DEBUG ESD RELATED PROBLEMS

STATE-OF-THE-ART ESD ANALYSIS
FINDS PROBLEMS AND CAUSES
EASY SOLUTIONS FOR DIFFICULT PROBLEMS

SOFICS
SOLUTIONS FOR ICS

ESD, LATCH-UP TESTING

- HBM & MM ANSI/ESDA and JEDEC
- Latch-up JEDEC
- TLP
  - Pulse width options: 75ns and 100ns
  - Rise time options: 200ps, 2ns, 10ns, 20ns
- VF-TLP
  - Pulse width options: 1ns, 2ns, 5ns and 10ns
  - Rise time options: 100ps, 200ps, 2ns
- DC leakage and IV tracing
- Solid state pulsing
- Thermo chuck for measurements up to 200°C
- Teseq NSG 438 ESD zap gun for IEC 61000-4-2

REDUCE TIME TO MARKET

Sofics helps customers identify the best full-chip ESD solution for their needs.

Combine public, customer-developed, and Sofics proprietary solutions as neccessary.

In spite of its low threshold for entry, this service leverages our extensive experience in providing product proven ESD solutions through 9 consecutive CMOS generations (0.5um down to 28nm) in all leading foundries

CONTACT US FOR MORE INFORMATION

SOFICS
SOLUTIONS FOR ICs

ESDdoctor@mail.sofics.com
http://www.sofics.com/products