ON-CHIP ESD SOLUTIONS FOR ADVANCED CMOS APPLICATIONS

IMPROVES IC/SOC PERFORMANCE
MEETS TOUGH ESD SPECIFICATIONS
REDUCES YOUR IC COST

SOFICS
Solutions For ICs

DESIGN WITHOUT CONSTRAINTS

- Low Parasitic capacitance for high speed or wireless applications
- Low leakage for analog interface protection
- Protect interfaces with most sensitive nodes like thin gates, core devices

REDUCE TIME TO MARKET

- Large library of standard ESD clamps available
- Customized EOS/ESD solutions can be delivered within a few days for almost any CMOS node
- Proven in more than 50 foundry and proprietary technologies

STRONGLY REDUCE IC COST

- Silicon and product proven ESD solutions help to reduce IC development cost
- Smaller silicon footprint help to reduce the manufacturing cost by 1% to 10%
- Compatible with the standard CMOS process flow. E.g. skip ESD implant layer and save >$40 per wafer

CONTACT US FOR MORE INFORMATION

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