



Data sheet

ESD clamps for 130nm, 350nm

On-chip ESD protection clamps for
TowerJazz 130nm, 350nm CMOS technology

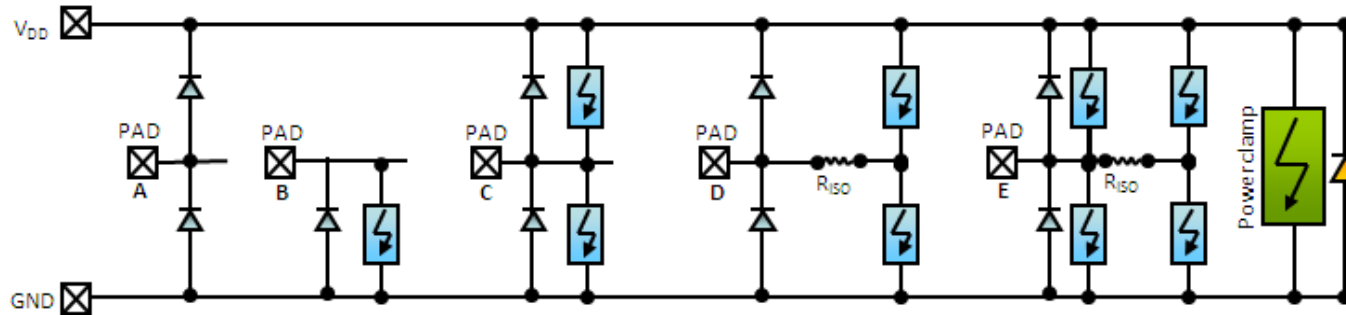
Sofics has verified its TakeCharge ESD protection clamps on technology nodes between 0.25um CMOS down to 28nm across various fabs and foundries. The ESD clamps are silicon and product proven in more than 1500 mass produced IC-products. The cells provide competitive advantage through improved yield, reduced silicon footprint and enable advanced multimedia and wireless interfaces like HDMI, USB 3.0, SATA, WIFI, GPS and Bluetooth.

The devices described in this document can be used for the protection of various voltage domains and interfaces in TowerJazz 130nm, 350nm CMOS technology.

ESD protection clamps for TowerJazz 130nm & 350nm CMOS technology

The following tables provide an overview of the Sofics ESD clamps verified on silicon. The cells can be easily adapted for other ESD protection levels and can be further customized to ensure compatibility with specific metal schemes and IO pitch. Cells for other voltage domains can be provided as well. In many cases devices verified in one foundry can be ported to another foundry. Please discuss your specific requirement with our sales person at bd@sofics.com.

The Sofics ESD cells cover all types of protection concepts and approaches as detailed in the figure below.



Different pad types available in the solution set from Sofics. For each power domain a power clamp is available. For the IO's several pad-types exist.

Process	Voltage domain	Clamp type Datasheet name	footprint	Leakage	Junction capacitance	ESD performance	Vt1	Info
TowerJazz 130nm	1.2V	power clamp DS-TJ130-PC1V2	<2000um ²	<50pA		>3 kV HBM V MM	3.3	
TowerJazz 130nm	1.2V	A clamp DS-TJ130-A1V2	<1000um ²	<1nA	<150	>3 kV HBM V MM	Depends on power clamp	Dual diode protection Low capacitive loading
TowerJazz 130nm	1.2V	B clamp DS-TJ130-B1V2	<2000um ²	<50pA		>3 kV HBM V MM	3.3	Overvoltage tolerant
TowerJazz 130nm	1.2V	C clamp DS-TJ130-C1V2	<3000um ²	<50pA	<150	>5 kV HBM >400 V MM	3.3	Full local protection
TowerJazz 130nm	1.2V	E clamp DS-TJ130-E1V2	<3000um ²	<10nA	<200	>4 kV HBM >200 V MM	Depends on driver	Full local protection

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Process	Voltage domain	Clamp type Datasheet name	footprint	Leakage	Junction capacitance	ESD performance	Vt1	Info
TowerJazz 130nm	3.3V	power clamp DS-TJ130-PC3V3	<3000um ²	<50pA		>5 kV HBM >250 V MM	9.6	
TowerJazz 130nm	3.3V	A clamp DS-TJ130-A3V3	<1000um ²	<1nA	<150	>3 kV HBM V MM	Depends on power clamp	Dual diode protection Low capacitive loading
TowerJazz 130nm	3.3V	B clamp DS-TJ130-B3V3	<3000um ²	<50pA		>5 kV HBM >250 V MM	9.6	Overtolerance tolerant
TowerJazz 130nm	3.3V	C clamp DS-TJ130-C3V3	<3500um ²	<50pA	<150	>3 kV HBM >300 V MM	9	Full local protection
TowerJazz 130nm	3.3V	E clamp DS-TJ130-E3V3	<3500um ²	<50pA	0	>5 kV HBM >400 V MM	Depends on driver	Full local protection
TowerJazz 350nm	4.5V	power clamp DS-TJ350-PC4V5	<5000um ²	<100pA	0	>8 kV HBM V MM	10.5	Circuit under Pad
TowerJazz 350nm	4.5V	power clamp DS-TJ350-PC4V5-RC	<7000um ²	<100pA	0	>8 kV HBM V MM	Depends on domain	Circuit under Pad
TowerJazz 350nm	4.5V	A clamp DS-TJ350-A4V5	<2000um ²	<100pA	<250	>8 kV HBM V MM	Depends on power clamp	Dual diode protection Circuit under Pad
TowerJazz 350nm	4.5V	D clamp DS-TJ350-D4V5	<4000um ²	<100pA	<560	>8 kV HBM V MM	Depends on power clamp	Dual diode protection & secondary protection Circuit under Pad
TowerJazz 350nm	4.5V	B clamp DS-TJ350-B4V5	<11000um ²	<500pA	<350	>8 kV HBM V MM	10.57	Circuit under Pad, Overtolerance tolerant, undervoltage tolerant
TowerJazz 350nm	4.5V	C clamp DS-TJ350-C4V5	<8000um ²	<5nA	<550	>8 kV HBM V MM	Depends on driver	Full local protection Circuit under Pad
TowerJazz 350nm	4.5V	C clamp DS-TJ350-C4V5-RC	<11000um ²	<1nA	<560	>8 kV HBM V MM	3	Full local protection Circuit under Pad

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About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
 - Enable unique requirements for Latch-up, ESD, EOS
 - Layout, metallization and aspect ratio customization
 - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

As is the case with many published ESD design solutions, the techniques and protection solutions described in this data sheet are protected by patents and patents pending and cannot be copied freely. PowerQubic, TakeCharge and Sofics are trademarks of Sofics BVBA.

Version

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