Data sheet

40V ESD protection

40V hebistor power clamp for TSMC 0.25um BCD technology

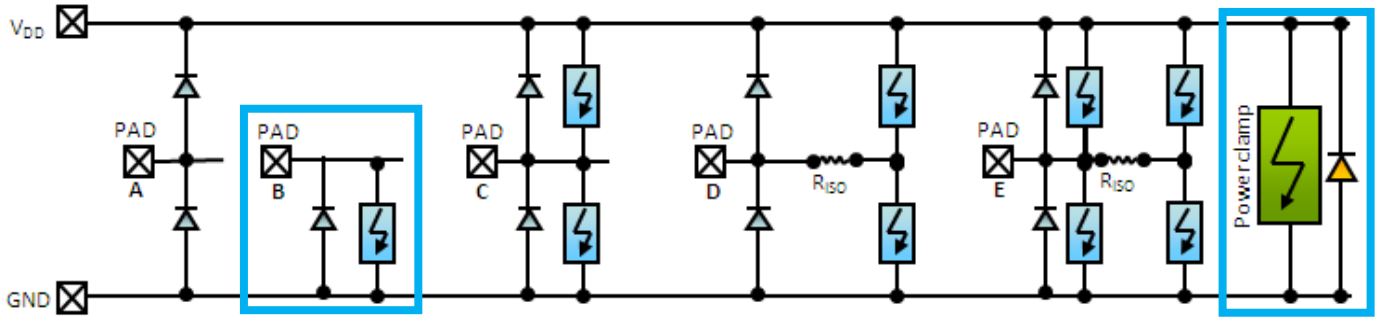
Sofics has verified its novel PowerQubic ESD protection clamps to TSMC 0.25um BCD 40V technology. The PowerQubic hebistor clamps are developed to protect a broad set of high voltage interfaces in BCD and high voltage CMOS. These cells provide competitive advantage through improved yield, reduced silicon footprint and interfacing with high voltage interfaces used in power management ICs, automotive applications and custom analog interfaces.

The ESD clamp described in this document protects all kinds of 40V interfaces in TSMC 0.25um BCD technology. It features a low leakage current. Thanks to the small silicon footprint it can be easily included into a broad set of IO's.

ESD protection clamp for 40V interfaces

Clamp type and usage

The Sofics ESD cells cover all types of protection concepts and approaches as detailed in the figure below. The ESD clamp cell described in this document is a **'Type B' solution** that can also be used as power clamp.



The ESD cell can be used for the protection of 40V interfaces.

Protection	40V	Comments
Core Protection	✓	
Input Protection	✗	Only 5V and 12V gates available in this BCD technology. Other clamps available for input protection
Output Protection	✓	
IO Protection	✗	
Over Voltage Tolerant IO (OVT)	✗	Over voltage tolerant clamp on request
Under Voltage Tolerant IO (UVT)	✗	Bi directional clamp on request
Inter Domain Protection	✗	

Features

- Efficient ESD protection
  - Different versions available for 2,4 and 8kV Human Body Model (HBM)
  - Different versions available for 100V, 200V and 400V Machine Model (MM)
- Leakage < 1 nA measured at 44V, room temperature
- Silicon footprint < 25.000um² (TLP-2A version)

Maximum ratings

Rating	Symbol	Value		Unit
		Min	Max	
Supply Voltage Range (DC)	V_{DD}	-0.5	44	V
Input/Output Voltage Range (DC)	V_{IO}	-0.5	44	V
Operating Temperature	T_{op}	-25	125	°C

Stresses exceeding these maximum ratings may damage the device. Functional operation above the recommended operating conditions is not implied. Extended exposure to stresses above the recommended operating conditions may affect device reliability.

The provided golden cell is designed for these maximum ratings/specifications. If the desired specification level differs, the golden cell has to be scaled up or down by using the Sofics implementation/scaling guidelines to remain a robust and effective ESD protection for the different specifications.

Electrical Characteristics

T_{amb} = 25°C unless stated otherwise

PAD to GND stress case

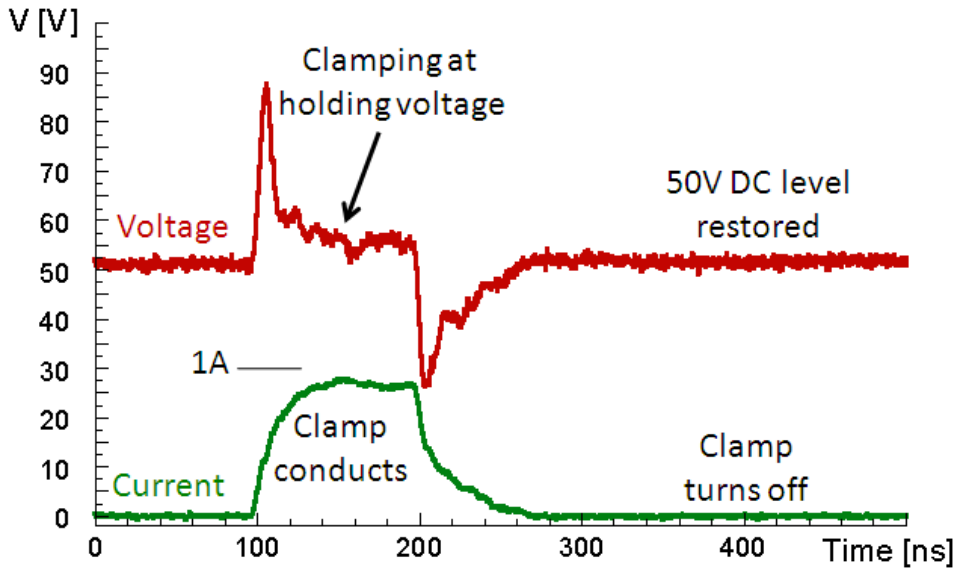
Parameter	Symbol	Typ.	Unit
Supply Voltage	V_{DD}	40	V
Trigger Voltage – TLP stress conditions	V_{t1}	44.5*	V
Breakdown Voltage – DC conditions, at 1uA	V_{bd_DC}	48	V
Holding Voltage – TLP like conditions – long pulse	V_h	51.6	V
Holding Voltage – DC conditions	V_h	>50	V
Breakdown Current – 2kV HBM version	I_{t2}	2.2	A
Breakdown Current – 4kV HBM version	I_{t2}	4.4	A
Breakdown Current – 8kV HBM version	I_{t2}	8.8	A
Breakdown Voltage	V_{t2}	<52	V

* Other trigger voltage possible with customized trigger circuit – does not affect clamping behavior

Other parameters

Parameter	Symbol	Typ.	Unit
Leakage current @ T_{amb} = 25 °C	I_{leak}	<1	nA
Leakage current @ T_{amb} = 125 °C, 2kV HBM version	I_{leak}	<50	nA
Leakage current @ T_{amb} = 125 °C, 4kV HBM version	I_{leak}	<75	nA
Leakage current @ T_{amb} = 125 °C, 8kV HBM version	I_{leak}	<125	nA
HBM – Human Body Model, 2kV HBM version		>2	kV
HBM – Human Body Model, 4kV HBM version		>4	kV
HBM – Human Body Model, 8kV HBM version		>8	kV
MM – Machine Model, 2kV HBM version		>100	V
MM – Machine Model, 4kV HBM version		>200	V
MM – Machine Model, 8kV HBM version		>400	V

Transient latch-up immunity test
1A TLP stress under powered conditions (50V DC bias)
No sustained latching after the ESD transient pulse disappears



Process, Area and integration

- Process: TSMC 0.25um BCD 40V
- Used Metals: 3 metals – (4 metals for TLP-8A version)
- Special needed Layer: N/A
- Area:
  - 2kV HBM version: 22.407 um²
  - 4kV HBM version: 29.017 um²
  - 8kV HBM version: 44.931 um²

LVS Net list – 2kV HBM version

```
R4 GND 8 NR r=20433.6
R8 1 11 NR r=5108.4
R9 GND 4 NR r=999.9
R10 11 5 NR r=999.9
R11 11 6 NR r=999.9
R12 VDD 7 NR r=999.9
R17 9 VDD NR r=5108.4
X18 7 8 4 4 LDDN l=7e-07 w=0.00067536 $[nld40_g5]
D30 8 18 zd_dio AREA=1.854e-11
D31 19 20 zd_dio AREA=1.854e-11
D32 20 21 zd_dio AREA=1.854e-11
D33 18 24 zd_dio AREA=1.854e-11
D34 25 19 zd_dio AREA=1.854e-11
D35 21 VDD zd_dio AREA=1.854e-11
D36 24 26 zd_dio AREA=1.854e-11
D37 26 25 zd_dio AREA=1.854e-11
D38 27 28 zd_dio AREA=1.854e-11
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About Sofics

ESD SOLUTIONS AT YOUR FINGERTIPS

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

Version

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