Data sheet

IO & ESD protection

1.8V & 3.3V capable general purpose digital IO pad based on 1.8V devices for TSMC 28nm CMOS technology

Sofics has verified its TakeCharge ESD protection clamps on TSMC 28nm CMOS HP and HPM technology. The technology is product proven in a broad range of applications across 9 CMOS generations. The cells provide competitive advantage through improved yield, reduced silicon footprint and enable advanced multimedia and wireless interfaces like HDMI, USB 3.0, SATA, WIFI, GPS and Bluetooth.

This CustomIO-IP enables the interface between a 28nm ASIC and legacy off chip components or data cards without extra cost of 2.5V/3.3V masks (if available). It provides a reliable, proven and low cost solution for true 3.3V signaling in deep submicron technologies.
The maximum voltage ratings and reliability are superior to overdriven 2.5V IOs in 28nm HP.
The IP is designed to reliably work under all start-up and power-up scenarios. It uses patented technology to minimize leakage under all conditions up to 125˚C. The device can withstand ESD events of over 2kV HBM and 200V MM, 500V CDM (ESD design by Sofics™).
The IP is qualified and characterized over corner lots, temperature, high temperature operating life, ESD and LU (IO design by ICSense™).

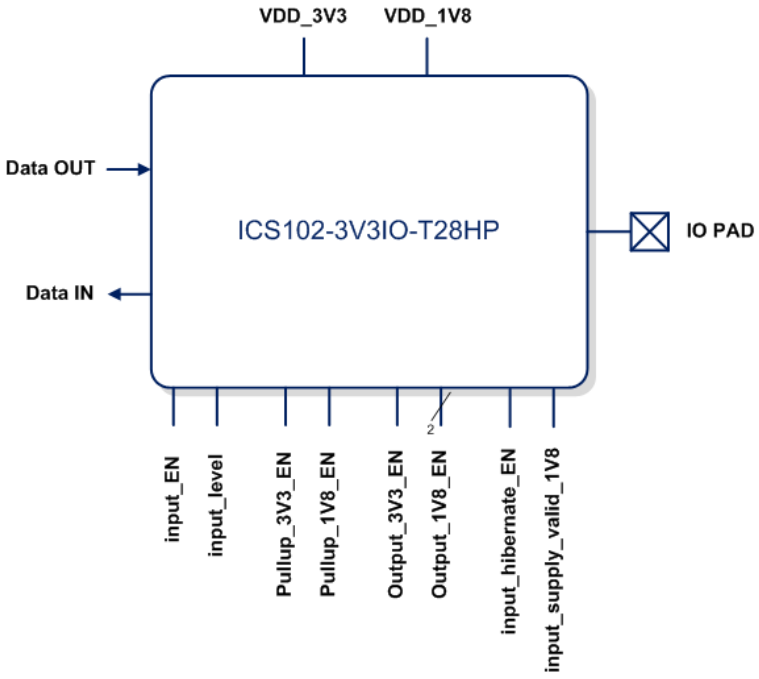
1.8V/3.3V capable general purpose digital IO pad based on 1.8V devices TSMC 28nm

Overview

This CustomIO-IP is complete 1.8V/3.3V capable general purpose digital IO pad. It converts 1.8V internal signaling to 3.3V or 1.8V level input/output while using only 1.8V devices in TSMC 28nm HP.

In addition to the IO driver cell(s), the supporting infrastructure is available in the IP: 3.3V power and ground pads; core power and ground pads; isolation cells to the ring. All is compatible with TSMC's tphn28hpgv18 IO ring. Supporting cells from the tphn28hpgv18 TSMC IO library can be used, subject to access to this library (not supplied by ICsense).

The IP is UHS50 compliant (50MHz DDR or 100MHz SDR modes maximum). Details can be found in the block diagram on page 3 or are available on request.



Technology	TSMC 28nm HP, 0.9V/1.8V
Features	3.3V IO, 50 MHz
	1.8V IO, 100 MHz
	Leakage below 6uA (125°C)
	ESD: 2kV HBM, 200V MM, 500V CDM
	TSMC padring compatible
	Max. Ratings: -0.3 .. 3.9V
	-40 .. 125°C
Deliverables	GDSII
	Abstract (LEF)
	CDL netlist for LVS
	.lib
	Verilog
	Documentation
	Integration guidelines
Status	Silicon proven

Applications

- SDXC interface
- SIM interface
- MMC interface
- Other 3.3V legacy ASIC-to-card/component interfaces

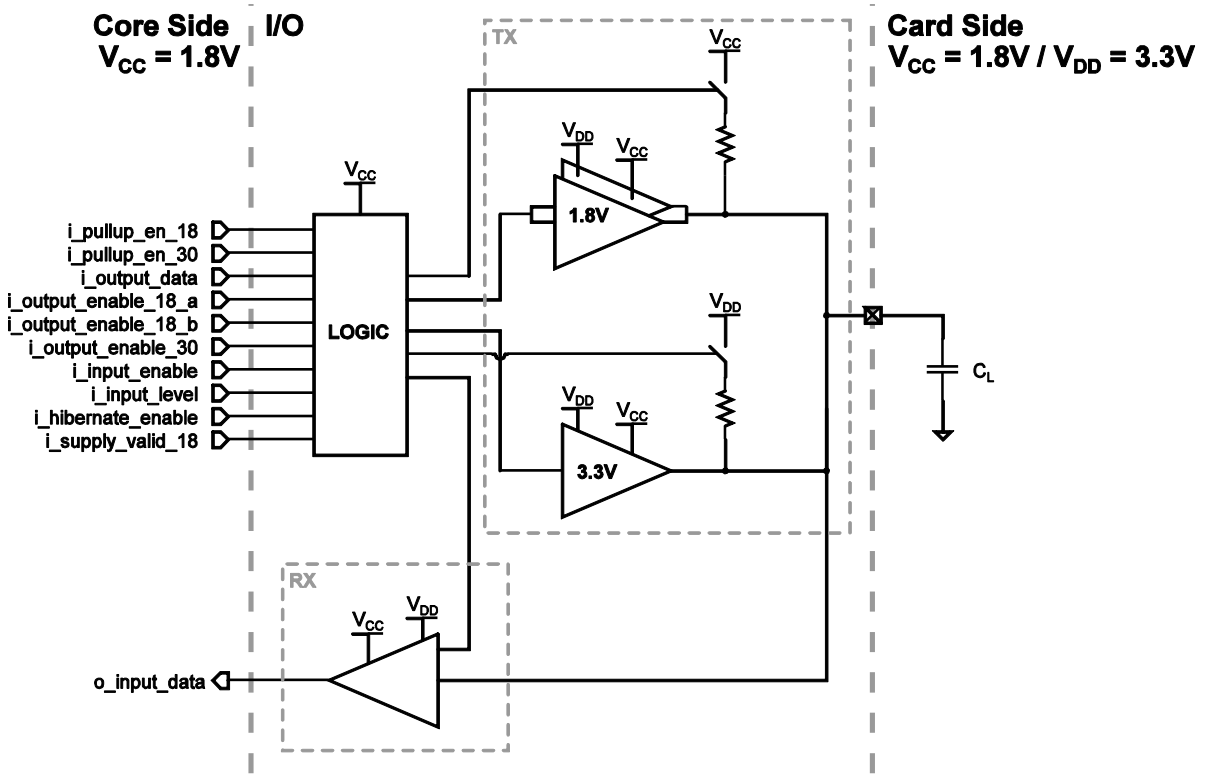
Maximum ratings

Rating	Symbol	Value		Unit
		Min	Max	
Supply Voltage Range (DC)	V_{DD}	-0.3	3.9	V
Max. Operating Temperature	T_{op}	-40	125	°C

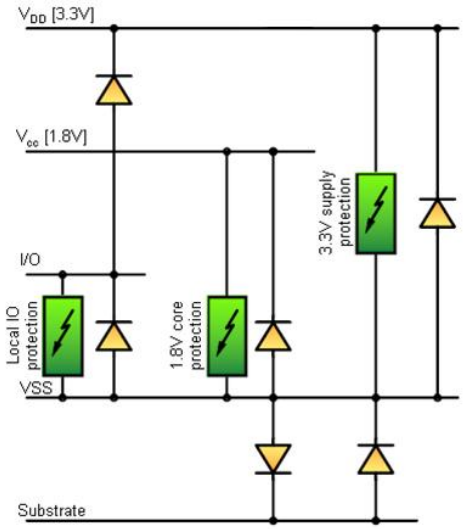
Stresses exceeding these maximum ratings may damage the device. Functional operation above the recommended operating conditions is not implied. Extended exposure to stresses above the recommended operating conditions may affect device reliability.

The provided golden cell is designed for these maximum ratings/specifications. If the desired specification level differs, the golden cell has to be scaled up or down by using the Sofics implementation/scaling guidelines to remain a robust and effective ESD protection for the different specifications.

Functional block diagram



ESD block diagram



Process

TSMC 28HP process:

- 1 poly
- M1, 5Mx,My,Mz,RDL metallization (circuits only up to M5)
- -40C to 125C junction temperature
- Deep N-well
- No CRT MOMS needed

The following devices are used:

- NCH_18 - I/O SVT NMOS
- NCH_NA18 - I/O native device
- PCH_18 - I/O SVT PMOS

About Sofics

ESD SOLUTIONS AT YOUR FINGERTIPS

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

About ICsense – our partner for CustomIO

ICsense is an ISO 9001:2000 certified IC design house offering analog, mixed-signal and high-voltage IC design services and ASIC turnkey solutions for the automotive, medical, industrial and consumer market. ICsense provides best-in-class IC design from consultancy and building block/IP design up to complete mixed-signal ASICs or SoCs. More information on www.icsense.com

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

As is the case with many published ESD design solutions, the techniques and protection solutions described in this data sheet are protected by patents and patents pending and cannot be copied freely. PowerQubic, TakeCharge, and Sofics are trademarks of Sofics BVBA.

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