



Data sheet

IO & ESD protection

1.8V & 3.3V capable general purpose digital IO pad based on 1.8V devices for TSMC 40nm CMOS technology

Sofics has verified its TakeCharge ESD protection clamps on TSMC 40nm CMOS G and LP technology. The devices are product proven in more than 25 mass produced 40nm products. The cells provide competitive advantage through improved yield, reduced silicon footprint and enable advanced multimedia and wireless interfaces like HDMI, USB 3.0, SATA, WIFI, GPS and Bluetooth.

The CustomIO-IP described in this document enables the interface between a 40nm ASIC and legacy off chip components or data cards without extra cost of 2.5V/3.3V masks (if available). It provides a reliable, proven and low cost solution for true 3.3V signaling in deep submicron technologies. The maximum voltage ratings and reliability are superior to overdriven 2.5V IOs in 40nm G/LP.

The IP is designed to reliably work under all start-up and power-up scenarios. It uses patented technology to minimize leakage under all conditions up to 125°C. The device can withstand ESD events of over 4kV HBM and 300V MM (ESD design by Sofics®). The IP is qualified and characterized over corner lots, temperature, high temperature operating life, ESD and LU (IO design by ICSense™).

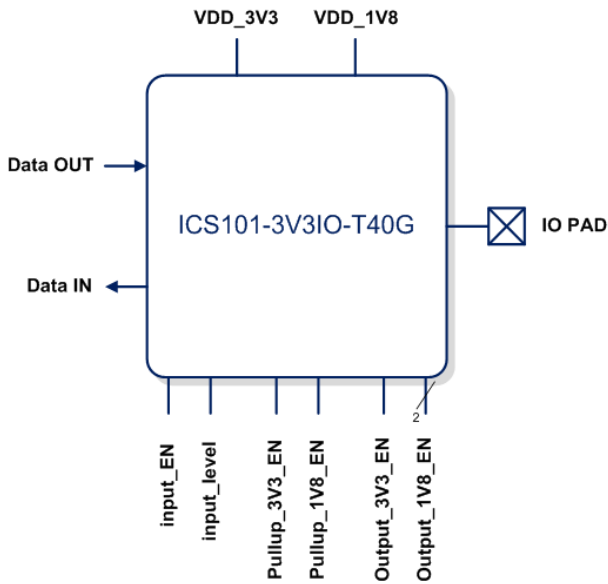
1.8V/3.3V capable general purpose digital IO pad based on 1.8V devices TSMC 40nm G, portable to LP

Overview

The CustomIO-IP is a complete 1.8V/3.3V capable general purpose digital IO pad. It converts 1.8V internal signaling to 3.3V or 1.8V level input/output while using only 1.8V devices in TSMC 40nm G.

In addition to the IO driver cell(s), the supporting infrastructure is available in the IP: 3.3V power and ground pads; core power and ground pads; isolation cells to the ring. All is compatible with TSMC's tpzn45gsgv18 IO ring. Supporting cells from the TSMC tpzn45gsgv18 IO library can be used, subject to access to this library (not supplied by Sofics).

The IP is UHS50 compliant (50MHz DDR or 100MHz SDR modes maximum). Details can be found in the block diagram on page 3 or are available on request.



Technology	TSMC 40nm G, 0.9/1.8V portable to LP, 1.1/1.8V
Features	3.3V IO, 50MHz
	1.8V IO, 100MHz
	Leakage below 5uA (125°C)
	4kV HBM, 300V MM
	TSMC pad ring compatible
Deliverables	GDSII
	Abstract (LEF)
	CDL net lists for LVS
	.lib
	<u>Verilog</u>
	Documentation
	Integration guidelines
Status	Silicon proven

Applications

- SDXC interface
- SIM interface
- MMC interface
- Other 3.3V legacy ASIC-to-card/component interfaces

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Maximum ratings

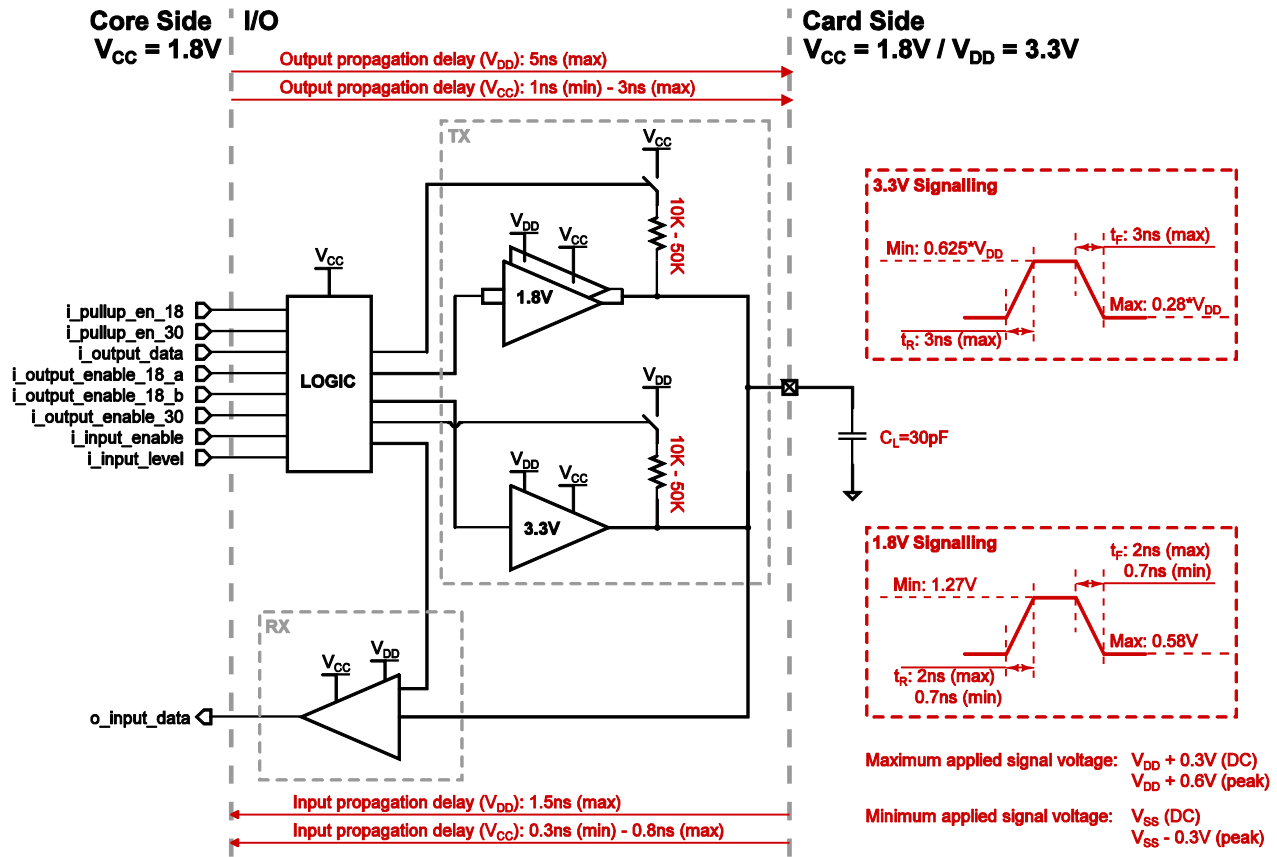
Rating	Symbol	Value		Unit
		Min	Max	
Supply Voltage Range (DC)	V_{DD}	-0.3	3.9	V
Max. Operating Temperature	T_{op}	-40	125	°C



Stresses exceeding these maximum ratings may damage the device. Functional operation above the recommended operating conditions is not implied. Extended exposure to stresses above the recommended operating conditions may affect device reliability.

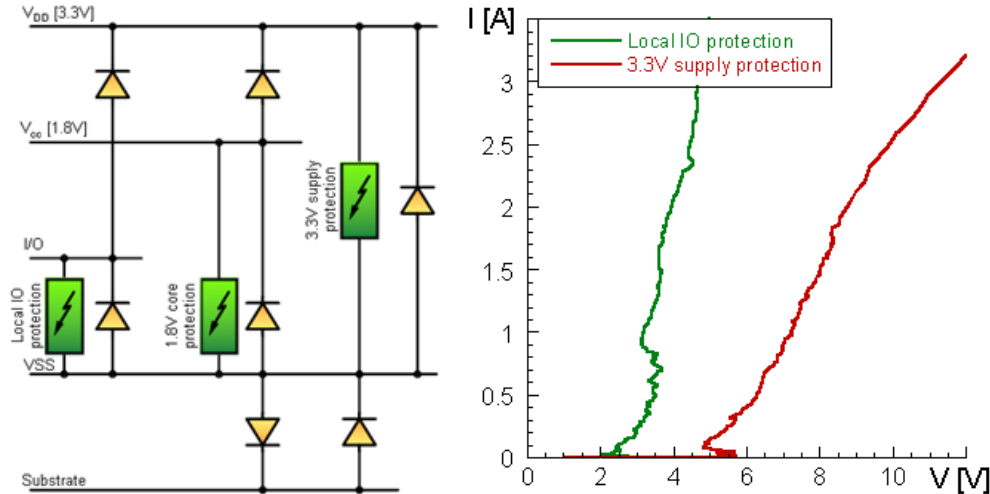
The provided golden cell is designed for these maximum ratings/specifications. If the desired specification level differs, the golden cell has to be scaled up or down by using the Sofics implementation/scaling guidelines to remain a robust and effective ESD protection for the different specifications.

Functional block diagram



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ESD block diagram and characterisation



Power supplies

The sequencing of the 1.8V and 3.0V supplies does not have to be guaranteed. The minimum rise and fall times on the supplies are given below:

Parameter	Min	Typ	Max	Unit	Comment
1.8V supply, rise time	40			us	
1.8V supply, fall time	100			us	
3.3V supply, rise time	30			us	
3.3V supply, fall time	200			us	

SDXC interface specifications

The interface is UHS50 compliant (50MHz DDR or 100MHz SDR modes maximum). Since the interface may be DDR, timing balance between rising and falling edges is present. The supply voltage to the pads is fixed at 3.0V to 3.3V nominal. The signalling level should be configurable between 3.0V and 1.8V nominal.

Bus Speed Mode	Max Bus speed (MB/s)	Max clock frequency (MHz)	Signal voltage (V)
SDR50	50	100	1.8
DDR50	50	50	1.8
SDR25	25	50	1.8
SDR12	12.5	25	1.8
High speed	25	50	3.3
Default speed	12.5	25	3.3

DC/AC parameters available on request and under NDA

SIM interface specifications

The SIM card interface includes two unidirectional signals for the reset and clock signals, and a bidirectional open-drain signal for the serial data stream. The open-drain pull-up resistor is included. Open drain operation is emulated using a combination of the data and enable inputs.

Signalling can be done at 3.0V or 1.8V levels. IO signal levels are referred to the selected signalling level. The open-drain pull-up resistor must be connected to the appropriate signalling level voltage.

DC/AC parameters available on request and under NDA

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Process

TSMC 40G process:

- 1 poly
- M1-7 (circuits only up to M3)
- -40C to 125C junction temperature
- Deep N-well
- EPI wafer (substrate resistivity 8-12 Ω -cm)

The following devices are used:

- NCH_18 - I/O SVT NMOS
- NCH_NA18 - I/O native device
- PCH_18 - I/O SVT PMOS

About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.



ESD SOLUTIONS AT YOUR FINGERTIPS

About ICsense – our partner for CustomIO

ICsense is an ISO 9001:2000 certified IC design house offering analog, mixed-signal and high-voltage IC design services and ASIC turnkey solutions for the automotive, medical, industrial and consumer market. ICsense provides best-in-class IC design from consultancy and building block/IP design up to complete mixed-signal ASICs or SoCs. More information on www.icsense.com

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
 - Enable unique requirements for Latch-up, ESD, EOS
 - Layout, metallization and aspect ratio customization
 - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

As is the case with many published ESD design solutions, the techniques and protection solutions described in this data sheet are protected by patents and patents pending and cannot be copied freely. PowerQubic, TakeCharge, and Sofics are trademarks of Sofics BVBA.

Version

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