



Data sheet

3.3V I/O protection

Dual diode protection

TSMC 40nm LP

Sofics has verified its TakeCharge ESD protection clamps on technology nodes between 0.25um CMOS down to 28nm across various fabs and foundries. The ESD clamps are silicon and product proven in more than 1500 mass produced IC-products. The cells provide competitive advantage through improved yield, reduced silicon footprint and enable advanced multimedia and wireless interfaces like HDMI, USB 3.0, SATA, WIFI, GPS and Bluetooth.

The ESD diodes described in this document can be used for the 3.3V interfaces in TSMC 40nm CMOS technology.

TSMC 40nm 3.3V I/O protection

Clamp type and usage

The Sofics ESD cells cover all types of protection concepts and approaches as detailed in the figure below. The ESD clamp cell described in this document is a type A clamp.



TSMC 40nm LP	3.3V	Comments
Core Protection		
Input Protection	YES	Needs efficient power clamp
Output Protection	YES	Needs efficient power clamp
I/O Protection	YES	Needs efficient power clamp
Over Voltage Tolerant I/O (OVT)		
Under Voltage Tolerant I/O (UVT)		
Inter Domain Protection		

Stress cases covered

PAD to VSS	Need separate power clamp	VSS to PAD	Diode down
VDD to PAD	Need separate power clamp	PAD to VDD	Diode up
VDD to VSS		VSS to VDD	

Connections in the cell

- Vdd, Vss, I/O

Features

- Efficient ESD protection
 - > 2.8 kV Human Body Model (HBM)
 - > 230 V Machine Model (MM)
- Leakage <100pA measured at 3.63V
- Silicon footprint <500um²

Maximum ratings

Rating	Symbol	Value		Unit
		Min	Max	
Supply Voltage Range (DC)	V_{DD}	-0.3	3.63	V
Input/Output Voltage Range (DC)	V_{IO}	-0.3	3.63	V
Operating Temperature	T_{op}	-25	125	°C
Burn-in Voltage (DC @ 125°C)		4.95		V



Stresses exceeding these maximum ratings may damage the device. Functional operation above the recommended operating conditions is not implied. Extended exposure to stresses above the recommended operating conditions may affect device reliability.

The provided golden cell is designed for these maximum ratings/specifications. If the desired specification level differs, the golden cell has to be scaled up or down by using the Sofics implementation/scaling guidelines to remain a robust and effective ESD protection for the different specifications.

Electrical Characteristics

$T_{amb} = 25^{\circ}\text{C}$ unless stated otherwise

Parameter	Symbol	Typ.	Unit
Trigger Voltage	V_{t1}	Depends on power clamp	V
Holding Voltage	V_h		V
Leakage current @ $T_{amb} = 25^{\circ}\text{C}$	I_{leak}	<100	pA
Leakage current @ $T_{amb} = 120^{\circ}\text{C}$	I_{leak}		
Total Capacitance Load, 0V bias	C_L	86.7	fF
Required (for ESD) resistance between bondpad and functional circuit	R_{iso}	0	Ohm
HBM – Human Body Model		2.8	kV
MM – Machine Model		230	V

Process, Area and integration

- Process: TSMC 40nm LP
- Used Metals: 4 metals – customization service available
- Special layers needed: N/A
- Area: 342.54 μm^2 (34.67 μm x 9.88 μm)

About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.



ESD SOLUTIONS AT YOUR FINGERTIPS

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
 - Enable unique requirements for Latch-up, ESD, EOS
 - Layout, metallization and aspect ratio customization
 - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

As is the case with many published ESD design solutions, the techniques and protection solutions described in this data sheet are protected by patents and patents pending and cannot be copied freely. PowerQubic, TakeCharge, and Sofics are trademarks of Sofics BVBA.

Version

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