Data sheet

1.8V I/O protection

Full local protection

High holding voltage

TSMC 65nm LP

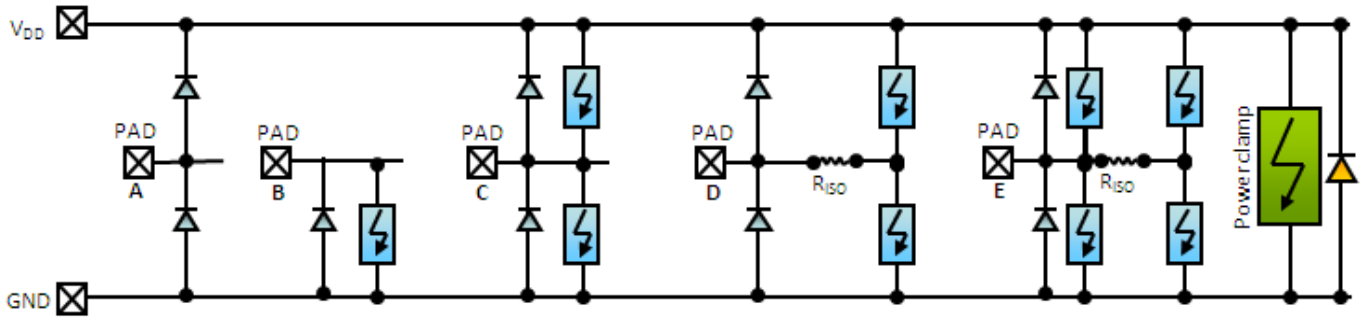
Sofics has verified its TakeCharge ESD protection clamps on technology nodes between 0.25um CMOS down to 28nm across various fabs and foundries. The ESD clamps are silicon and product proven in more than 1500 mass produced IC-products. The cells provide competitive advantage through improved yield, reduced silicon footprint and enable advanced multimedia and wireless interfaces like HDMI, USB 3.0, SATA, WIFI, GPS and Bluetooth.

The ESD clamp described in this document protects 1.8V interfaces in TSMC 65nm CMOS technology.

TSMC 65nm 1.8V I/O protection

Clamp type and usage

The Sofics ESD cells cover all types of protection concepts and approaches as detailed in the figure below. The ESD clamp cell described in this document is a type C clamp.



TSMC 65nm LP	1.8V	Comments
Core Protection		
Input Protection	YES	
Output Protection	YES	
I/O Protection	YES	
Over Voltage Tolerant I/O (OVT)		
Under Voltage Tolerant I/O (UVT)		
Inter Domain Protection		

Stress cases covered

PAD to VSS	Clamp	VSS to PAD	Diode down
VDD to PAD	Clamp	PAD to VDD	Diode up
VDD to VSS	Power clamp	VSS to VDD	Reverse diode

Connections in the cell

- Vdd, Vss, I/O

Features

- Efficient ESD protection
  - > 2 kV Human Body Model (HBM)
  - > 200 V Machine Model (MM)
- Leakage <50pA measured at 1.98V
- Silicon footprint <3000um²
- High holding voltage

Maximum ratings

Rating	Symbol	Value		Unit
		Min	Max	
Supply Voltage Range (DC)	V_{DD}	-0.3	1.98	V
Input/Output Voltage Range (DC)	V_{IO}	-0.3	1.98	V
Operating Temperature	T_{op}	-25	125	°C
Burn-in Voltage (DC @ 125°C)		2.7		V

Stresses exceeding these maximum ratings may damage the device. Functional operation above the recommended operating conditions is not implied. Extended exposure to stresses above the recommended operating conditions may affect device reliability.

The provided golden cell is designed for these maximum ratings/specifications. If the desired specification level differs, the golden cell has to be scaled up or down by using the Sofics implementation/scaling guidelines to remain a robust and effective ESD protection for the different specifications.

Electrical Characteristics

T_{amb} = 25°C unless stated otherwise

Parameter	Symbol	Typ.	Unit
Trigger Voltage	V_{t1}	4.0	V
Holding Voltage	V_h	2.9	V
Leakage current @ T_{amb} = 25 °C	I_{leak}	30	pA
Leakage current @ T_{amb} = 120 °C	I_{leak}	376	nA
Total Capacitance Load, 0V bias	C_L	120	fF
Required (for ESD) resistance between bondpad and functional circuit	R_{iso}	0	Ohm
HBM – Human Body Model		2	kV
MM – Machine Model		200	V

Process, Area and integration

- Process: TSMC 65nm LP
- Used Metals: 3 metals – customization service available
- Special layers needed: N/A
- Area: 2935.868 um² (33.8 um x 86.86 um)

About Sofics

ESD SOLUTIONS AT YOUR FINGERTIPS

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

Version

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