Data sheet

ESD clamps for 65nm

On-chip ESD protection clamps for TSMC 65nm CMOS technology

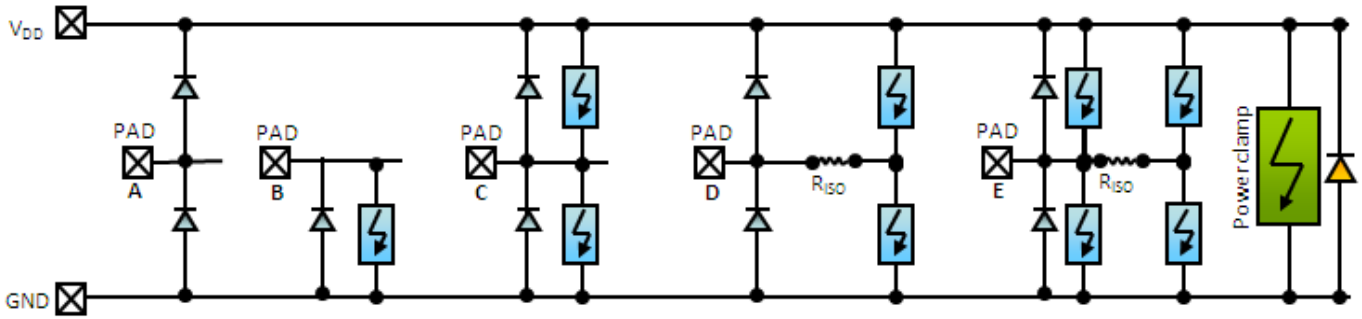
Sofics has verified its TakeCharge ESD protection clamps on technology nodes between 0.25um CMOS down to 28nm across various fabs and foundries. The ESD clamps are silicon and product proven in more than 1500 mass produced IC-products. The cells provide competitive advantage through improved yield, reduced silicon footprint and enable advanced multimedia and wireless interfaces like HDMI, USB 3.0, SATA, WIFI, GPS and Bluetooth.

The devices described in this document can be used for the protection of various voltage domains and interfaces in TSMC 65nm CMOS technology.

ESD protection clamps for TSMC 65nm CMOS technology

The following tables provide an overview of the Sofics ESD clamps verified on silicon. The cells can be easily adapted for other ESD protection levels and can be further customized to ensure compatibility with specific metal schemes and IO pitch. Cells for other voltage domains can be provided as well. In many cases devices verified in one foundry can be ported to another foundry. Please discuss your specific requirement with our sales person at bd@sofics.com.

The Sofics ESD cells cover all types of protection concepts and approaches as detailed in the figure below.



Different pad types available in the solution set from Sofics. For each power domain a power clamp is available. For the IO's several pad-types exist.

Process	Voltage domain	Clamp type Datasheet name	footprint	Leakage	Junction capacitance	ESD performance	Vt1	Info
TSMC 65nmG	1.0V	power clamp DS-TS65G-PC1V0	<700um²	<10nA	~60	3 kV HBM V MM	2.4	Circuit under Pad
TSMC 65nmG	1.0V	power clamp DS-TS65G-PC1V0-RC	<1400um²	<10nA	~60	2 kV HBM V MM	2.5	Circuit under Pad
TSMC 65nmG	1.0V	A clamp DS-TS65G-A1V0	<500um²	<1nA	<100	4 kV HBM V MM	Depends on power clamp	Dual diode protection Circuit under Pad
TSMC 65nmG	1.0V	B clamp DS-TS65G-B1V0	<700um²	<10nA	~60	3 kV HBM V MM	2.4	Overvoltage tolerant, Circuit under Pad

Process	Voltage domain	Clamp type Datasheet name	footprint	Leakage	Junction capacitance	ESD performance	Vt1	Info
TSMC 65nmG	1.0V	B clamp DS-TS65G-B1V0-RC	<1400um²	<10nA	~60	2 kV HBM V MM	2.5	Overvoltage tolerant, Circuit under Pad
TSMC 65nmG	1.0V	B clamp DS-TS65G-B1V0-E	<1000um²	<10nA	<100	2 kV HBM V MM	Depends on power clamp	Circuit under Pad
TSMC 65nmLP	1.2V	power clamp DS-TS65LP-PC1V2	<1500um²	<100pA	0	2 kV HBM 200 V MM	3.15	Circuit under Pad
TSMC 65nmLP	1.2V	power clamp DS-TS65LP-PC1V2-W2	<2400um²	<1nA	0	7 kV HBM V MM	3.15	Circuit under Pad
TSMC 65nmLP	1.2V	power clamp DS-TS65LP-PC1V2-RC	<1600um²	<50nA	0	4 kV HBM V MM	2.5	Circuit under Pad
TSMC 65nmLP	1.2V	A clamp DS-TS65LP-A1V2	<500um²	<1nA	<100	4 kV HBM V MM	Depends on power clamp	Dual diode protection Circuit under Pad
TSMC 65nmLP	1.2V	A clamp DS-TS65LP-A1V2-W2	<500um²	<500pA	220	4 kV HBM 400 V MM	Depends on power clamp	Dual diode protection Circuit under Pad
TSMC 65nmLP	1.2V	B clamp DS-TS65LP-B1V2	<1500um²	<100pA	0	2 kV HBM 200 V MM	3.15	Overvoltage tolerant, Circuit under Pad
TSMC 65nmLP	1.2V	B clamp DS-TS65LP-B1V2-W2	<2400um²	<1nA	0	7 kV HBM V MM	3.15	Overvoltage tolerant, Circuit under Pad
TSMC 65nmLP	1.2V	C clamp DS-TS65LP-C1V2	<2400um²	<50pA	120	2 kV HBM 200 V MM	2.3	Full local protection Circuit under Pad
TSMC 65nmLP	1.2V	C clamp DS-TS65LP-C1V2-HHV	<2400um²	<50pA	190	2 kV HBM 200 V MM	3.16	Full local protection High holding voltage, Circuit under Pad
TSMC 65nmLP	1.2V	C clamp DS-TS65LP-C1V2-OVT	<2500um²	<10pA	190	2 kV HBM 200 V MM	3.16	Full local protection Overvoltage tolerant, Circuit under Pad

Process	Voltage domain	Clamp type Datasheet name	footprint	Leakage	Junction capacitance	ESD performance	Vt1	Info
TSMC 65nmLP	1.8V	power clamp DS-TS65LP-PC1V8	<1900um²	<500pA	0	2 kV HBM 200 V MM	2.7	Circuit under Pad
TSMC 65nmLP	1.8V	A clamp DS-TS65LP-A1V8	<500um²	<1nA	<100	4 kV HBM V MM	Depends on power clamp	Dual diode protection Circuit under Pad
TSMC 65nmLP	1.8V	A clamp DS-TS65LP-A1V8-W2	<500um²	<500pA	220	4 kV HBM 400 V MM	Depends on power clamp	Dual diode protection Circuit under Pad
TSMC 65nmLP	1.8V	B clamp DS-TS65LP-B1V8	<1900um²	<500pA	0	2 kV HBM 200 V MM	2.7	Overvoltage tolerant, Circuit under Pad
TSMC 65nmLP	1.8V	C clamp DS-TS65LP-C1V8	<2600um²	<50pA	120	2 kV HBM 200 V MM	4.0	Full local protection Circuit under Pad
TSMC 65nmLP	1.8V	C clamp DS-TS65LP-C1V8-HHV	<3000um²	<50pA	120	2 kV HBM 200 V MM	4.0	Full local protection High holding voltage, Circuit under Pad
TSMC 65nmLP	1.8V	C clamp DS-TS65LP-C1V8-OVT	<2900um²	<500pA	0	2 kV HBM 200 V MM	4.0	Full local protection Overvoltage tolerant, Circuit under Pad
TSMC 65nmLP	2.5V	power clamp DS-TS65LP-PC2V5	<2200um²	<500pA	0	2 kV HBM 200 V MM	3.45	Circuit under Pad
TSMC 65nmLP	2.5V	A clamp DS-TS65LP-A2V5	<500um²	<1nA	<100	4 kV HBM V MM	Depends on power clamp	Dual diode protection Circuit under Pad
TSMC 65nmLP	2.5V	A clamp DS-TS65LP-A2V5-W2	<500um²	<500pA	220	4 kV HBM 400 V MM	Depends on power clamp	Dual diode protection Circuit under Pad
TSMC 65nmLP	2.5V	B clamp DS-TS65LP-B2V5	<2200um²	<500pA	0	2 kV HBM 200 V MM	3.45	Circuit under Pad
TSMC 65nmLP	2.5V	C clamp DS-TS65LP-C2V5	<2400um²	<50pA	115	2 kV HBM 200 V MM	4.94	Full local protection Circuit under Pad

Process	Voltage domain	Clamp type Datasheet name	footprint	Leakage	Junction capacitance	ESD performance	Vt1	Info
TSMC 65nmLP	2.5V	C clamp DS-TS65LP-C2V5-HHV	<3300um²	<100pA	287	2 kV HBM 200 V MM	3.33	Full local protection High holding voltage, Circuit under Pad
TSMC 65nmLP	2.5V	C clamp DS-TS65LP-C2V5-OVT	<3300um²	<500pA	287	2 kV HBM 200 V MM	5.5	Full local protection Overvoltage tolerant, Circuit under Pad
TSMC 65nmLP	3.3V	power clamp DS-TS65LP-PC3V3	<2500um²	<50pA	0	2 kV HBM 200 V MM	4.24	Circuit under Pad
TSMC 65nmLP	3.3V	A clamp DS-TS65LP-A3V3	<500um²	<1nA	<100	4 kV HBM V MM	Depends on power clamp	Dual diode protection Circuit under Pad
TSMC 65nmLP	3.3V	A clamp DS-TS65LP-A3V3-W2	<500um²	<500pA	220	4 kV HBM 400 V MM	Depends on power clamp	Dual diode protection Circuit under Pad
TSMC 65nmLP	3.3V	B clamp DS-TS65LP-B3V3	<2500um²	<50pA	0	2 kV HBM 200 V MM	4.24	Overvoltage tolerant, Circuit under Pad
TSMC 65nmLP	3.3V	C clamp DS-TS65LP-C3V3	<3300um²	<100pA	109	2 kV HBM 200 V MM	4.94	Full local protection Circuit under Pad
TSMC 65nmLP	3.3V	C clamp DS-TS65LP-C3V3-HHV	<3600um²	<50pA	281	2 kV HBM 200 V MM	3.33	Full local protection High holding voltage, Circuit under Pad
TSMC 65nmLP	3.3V	C clamp DS-TS65LP-C3V3-OVT	<3300um²	<500pA	0	2 kV HBM 200 V MM	5.5	Full local protection Overvoltage tolerant, Circuit under Pad

ESD SOLUTIONS AT YOUR FINGERTIPS

About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
    - Enable unique requirements for Latch-up, ESD, EOS
    - Layout, metallization and aspect ratio customization
    - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

As is the case with many published ESD design solutions, the techniques and protection solutions described in this data sheet are protected by patents and patents pending and cannot be copied freely. PowerQubic, TakeCharge and Sofics are trademarks of Sofics BVBA.

Version

August 2012

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