Conference paper

High Holding Current SCRs (HHI-SCR) for ESD Protection and Latch-up Immune IC Operation

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This paper presents a novel SCR for power line and local I/O ESD protection. The HHI-SCR exhibits a dual ESD clamp characteristic: low-current high-voltage clamping and high-current low-voltage clamping. These operation modes enable latch-up immune normal operation as well as superior full chip ESD protection. The minimum latch current is controlled by device design. The HHI-SCR is demonstrated in 0.10um-CMOS and in a 0.4um-BiCMOS technology. The design is highly area efficient.

High Holding Current SCRs (HHI-SCR)
for ESD Protection and Latch-up Immune IC Operation

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Abstract – This paper presents a novel SCR for power line and local I/O ESD protection. The HHI-SCR exhibits a dual ESD clamp characteristic: low-current high-voltage clamping and high-current low-voltage clamping. These operation modes enable latch-up immune normal operation as well as superior full chip ESD protection. The minimum latch current is controlled by device design. The HHI-SCR is demonstrated in 0.10um-CMOS and in a 0.4um-BiCMOS technology. The design is highly area efficient.

I. INTRODUCTİON

Silicon Controlled Rectifiers (SCRs) have long been used as on-chip ESD protection elements over a broad range of technologies because of their superior ESD behavior [1]-[5].

With SCRs extremely large failure currents, low dynamic on-resistances, and an ideal ESD performance width scaling can be accomplished as a result of a regenerative conduction mechanism with double-current injection (i.e. minority carrier injection into both wells). The excellent high current behavior of SCRs provide an area gain factor of 4 to 5 over silicide-blocked grounded-gate NMOS (GGNMOS) protection devices.

Decisively, the superior voltage clamping capabilities of SCRs make those devices indispensable protection elements in technologies, where the so-called ESD design window becomes extremely narrow. For example, significant future relevance of SCR-based protection elements is anticipated for sub-0.1um applications, where the NMOS holding voltage would exceed the dynamic breakdown voltage of ultra-thin gate oxides.

Another field of application are advanced BiCMOS technologies with extremely sensitive HBT emitter-base junctions. These sensitive elements require very low clamp voltages to be successfully protected.

Moreover, high-voltage technologies with often extremely ESD sensitive high-voltage NMOS transistors (caused by "strong" voltage snapback [6]) lack suitable power protection elements. Here, high-voltage SCR-type protection elements can be a feasible solution.

This paper presents a novel High-Holding Current SCR (HHI-SCR) device, which is directly derived from the Grounded-Gate NMOS triggered SCR (GGSCR) protection element [1].
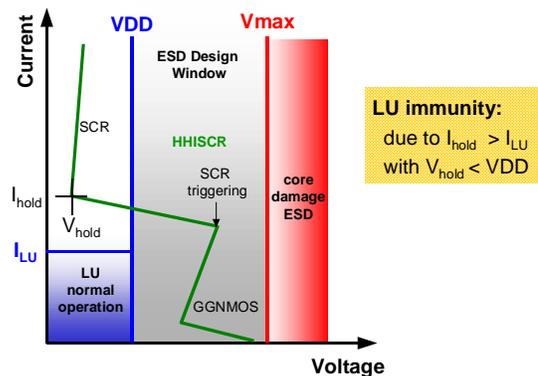

Figure 1 Generic HHI-SCR IV characteristic within the ESD Design Window defined by the supply voltage VDD and a maximum LU current I_{LU} for normal IC operation. The upper design margin is determined by the critical voltage at circuit failure, e.g. at transient oxide breakdown.

As depicted in Figure 1, the HHI-SCR employs an SCR with an increased holding current I_{hold} above a certain minimum LU current I_{LU}. Thus, LU-immune normal operation designs can be ensured, whereas the excellent SCR high current behavior for ESD protection application is preserved to a large extent.

II. STATE OF THE ART - GGSCR

In order to apply SCRs for ESD protection, the triggering voltage needs to be reduced below the critical node voltages within an IC, e.g. the transient gate oxide breakdown voltage. This can be achieved by connecting an external GGNMOS trigger element to the SCR between anode and gate node G1 as illustrated in the equivalent circuit in Figure 2. This specific implementation is referred to as a GGNMOS triggered SCR or briefly GGSCR [1].
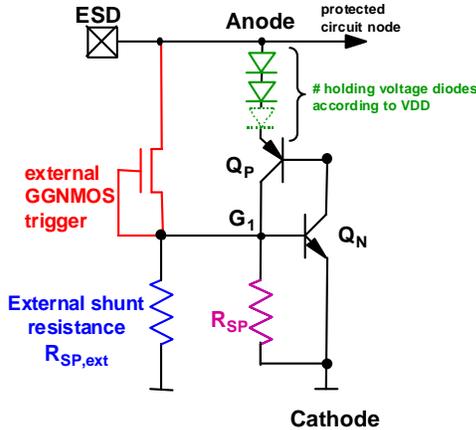

Figure 2 Schematic of an external GGNMOS triggered SCR (GGSCR) with external poly shunt resistor $R_{SP,ext}$ connected to the SCR gate G1 (P-well). Series diodes increase the holding voltage for LU immunity during normal operation.

During ESD stress conditions, the triggering voltage of the GGNMOS is reached leading to base (P-well) current injection into the NPN Q_N of the SCR. This triggers NPN bipolar operation, which provided the base drive for the SCR PNP transistor Q_P, since the Q_N collector corresponds to the Q_P base, and vise versa. As a result of this mutual bipolar base current injection, self-sustained, regenerative SCR "latch-up" (LU) is turned on. Once latch-up operation is initiated and maintained with a sufficient current / voltage source between anode and cathode, the trigger source can be "removed" without turning the SCR off. Due to the self-sustained operation mode, careful precautions need to be taken to guarantee latch-up immunity during normal operation, see for example [8] - [12]. Particularly, when using SCRs as power clamps, unintended triggering must be avoided for functional IC design according to IC latch-up (LU) specifications. But also for signal-integrity, local clamps at I/O pads need to be robust against temporary LU.

An external (poly) shunt resistor at G1 in the order of magnitude of approximately $R_{SP,ext} \approx 1k\Omega$ drains any leakage current of the trigger element during normal operation. The inherent resistance R_{SP} in parallel to $R_{SP,ext}$ represents the connection of the P-well to a P-Substrate. The higher substrate doping means a lower substrate resistance and thus shunt resistance.
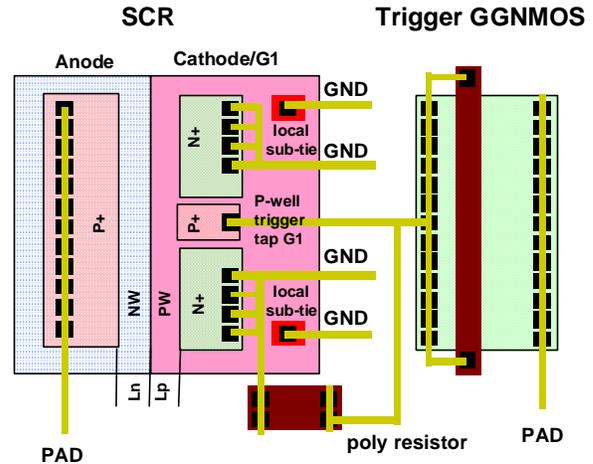

Figure 3 Layout sketch of the GGSCR showing the position of the P+ Anode, the N+ Cathode and the external trigger GGNMOS connected to the SCR (NPN) trigger tap G1. The position of the trigger tap close to the NPN base ensures efficient triggering of the SCR. No series diodes for V_{hold} increase are shown.

One feasible and successful approach for LU engineering uses series diodes, which are connected to the anode of the SCR, cf. Figure 2, to increase the holding voltage V_{hold} above the supply voltage VDD (plus a safety margin) [1]. However, this concept comes with several disadvantages and trade-offs:

- Diodes increase the dynamic clamping voltage. As a result, the typically excellent SCR voltage clamping capability is deteriorated.

- Diodes require the same width as the SCR, and, therefore, occupy significant silicon real estate.

- A large number of series diodes (>3) can result in high leakage currents due to an inherent parasitic PNP Darlington transistor to the substrate. Consideration of this issue is in particular important for high-temperature leakage specifications. Therefore, this technique cannot be applied for supply voltages VDD ≥ 5V, where more than three series diodes would be needed to increase V_{hold} above VDD.

A layout sketch of the GGSCR is shown in Figure 3. In this typical configuration, the N-well is left

floating, i.e. no Gate 2 tie is introduced to pull the N-well high.

III. NOVEL DESİGN - HHI-SCR

The generic IV characteristic of the HHI-SCR, which is shown in Figure 1, complies with the constraints of the ESD design window despite of a potentially low holding voltage below the supply voltage VDD.

In contrast to the V_{hold} engineering approach discussed above, this technique makes use of a higher SCR holding current I_{hold} above a maximum current I_{LU}, thus accomplishing a LU-immune design for IC operation.
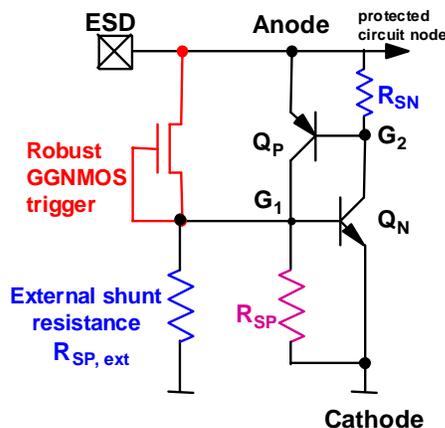

Figure 4 Equivalent circuit of HHI-SCR indicating the different elements as compared to the GGSCR in Figure 2.

The principle of the novel HHI-SCR device, cf. Figure 4, is derived from the GGSCR in Figure 2. Essentially, the novel device technique applies largely reduced P-well and N-well shunt resistances, R_{SP} and R_{SN}, respectively.

The GGSCR exhibits an extremely high effective N-well (floating) resistance due to quasi-isolation within a P-substrate, therefore relying on holding voltage increase above VDD for IC LU immunity. In contrast to the GGSCR, the N-well within the HHI-SCR is not left floating. Here, several (while only one is shown) N+ taps (G2) are inserted into the Nwell to tie the well high. These Nwell gate-ties are short-circuited with the anode by metal to minimize the shunt resistance R_{SN}. Then, in P-substrate technologies, R_{SN} is defined by the N-well geometry and doping profile, the position of the N-well-tie with respect to the PNP base, and the external N-well shunt resistance inserted between gate G2 and anode, which is negligible in case of a metal short.

In analogy, the P-well shunt resistance R_{SP} is determined by the P-well geometry and doping profile as well as the position of the Pwell-taps with regard to the NPN base. Moreover, in a P-substrate technology, the P-well has a significant shunt path into the substrate, such that R_{SP} also depends on the substrate properties. Finally, the external P-well shunt (or trigger) resistance $R_{SP,ext}$ between G1 and cathode influences the total resistance to ground.

By adjusting the external shunt resistance and applying effective SCR P-well/ N-well tie layout techniques, both (base) resistance values can be significantly reduced. Thus, both parasitic BJTs (forming the SCR) require more base current to reach the forward bias of the corresponding emitter-base junctions, which results in the regenerative SCR latch mode. Consequently, a higher triggering current $I_{t1,SCR}$ as well as holding current $I_{h,SCR}$ is required to trigger and to sustain the SCR on-state, respectively.
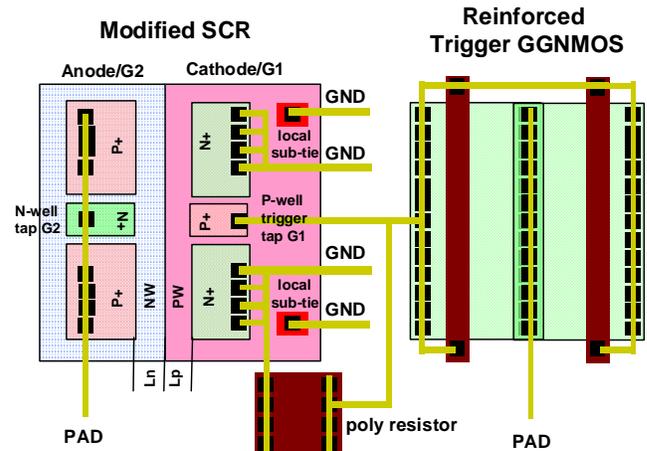

Figure 5 Layout of HHI-SCR containing reinforced GGNMOS trigger element, low-resistive and ESD robust poly resistor, and a modified SCR layout to reduce the effective shunt resistance of N-well and P-well, respectively.

To latch an SCR, the 'beta' product of the inherent NPN and PNP transistor current gains need to be in the order of unity, i.e. $\beta_n \cdot \beta_p \approx 1$ [13]. Since beta decreases with increasing transistor current (Webster Effect [13]), the HHI-SCR IV characteristic can also reveal an increased holding voltage.

III.a. External Shunt Resistance

The external shunt resistance connected to G1 (P-well) is formed by a poly resistor Rpol $\approx$ 1-10Ω of sufficient width, and thus of adequate ESD current capability. Due to a deliberately increased SCR triggering current, the GGNMOS element needs to

provide larger currents to turn on the SCR. In other words, for relatively low currents the GGNMOS protects the circuit whereas the SCR is not activated yet.

For a sufficient GGNMOS trigger current injection into the SCR (G1), the voltage across the external resistor (e.g. poly) needs to reach approximately 0.7V to forward bias the NPN base emitter junction. Consequently, the trigger device must be robust enough to provide at least $It1 \approx 0.7V/R_{SP,ext}$. Depending on the magnitude of the SCR triggering/holding current, reinforced multi-finger NMOS transistors (as indicated in Figure 5) are incorporated, which can survive these larger injection currents.

Particular compact configurations are possible applying advanced resistive ballast and multi-finger turn-on techniques [14].
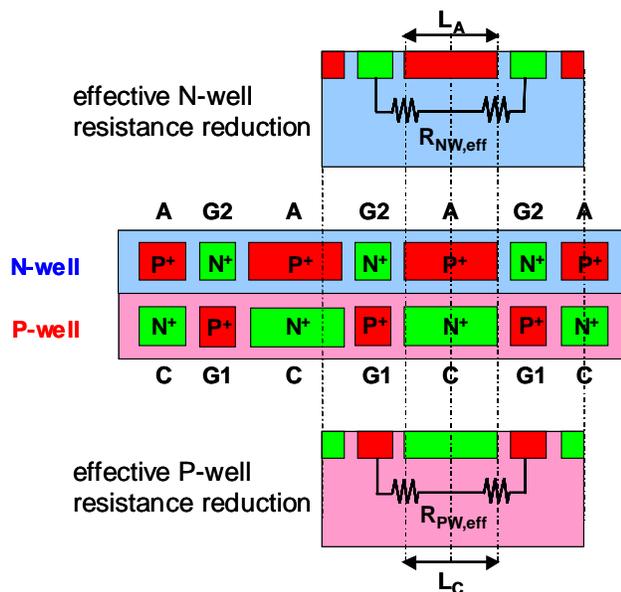

Figure 6 SCR layout technique to reduce the effective well resistances (SCR shunt resistance) and increase the SCR holding current.

III.b. Intrinsic Well Resistance

Figure 6 depicts a layout approach to reduce the inherent shunt resistance and thus to control the SCR holding and trigger current. Here, intermittent gate diffusion taps between cathode stripes (G1 in Pwell) and anode stripes (G2 in Nwell) are introduced. By interrupting the SCR cathode/anode, the effective well resistance with regard to the P+/N+ well-ties is reduced. Here, the P+ gates G1 do not only serve as well-ties to minimize the effective Pwell shunt

resistance, they also act as efficient GGNMOS trigger current injectors due to the proximity to the NPN base part of the SCR. The layout technique shown in Figure 6 reduces the effective well (or NPN/PNP bipolar base) resistances $R_{PW,eff}/R_{NW,eff}$: the shorter the length of the anode and cathode stripe, L_A and L_C, the lower $R_{NW,eff}$ and $R_{PW,eff}$, respectively, the higher the SCR holding current. Thus, changing the number of taps allows designing for the minimum required SCR injection current, i.e. holding current.

In other words, the LU immunity current-level can be controlled according to the product LU specification and / or signal current amplitude.

Note that continuous well-ties close to the anode and cathode do not provide an adequate low-resistive well connection because of the larger distance to the bipolar bases. On the other hand, these continuous ties can be introduced in addition to the intermittent well ties to further reduce the effective well and thus shunt resistances.

Once the structure enters full SCR operation under ESD stress conditions, mainly anode and cathode partitions contribute to the ESD current conduction. In this operation regime, both wells are strongly conductivity modulated, which results in the excellent ESD performance and low resistive clamping behavior.

IV. EXPERİMENTAL RESULTS

HHI-SCR devices were successfully implemented in a 0.10um-CMOS technology and in a 0.4um-BiCMOS technology.

The TLP analysis results were obtained with a Barth 4002 Transmission Line Pulse (TLP) tester with a square pulse duration of 100ns and default pulse rise time of 10ns.

IV.a. 0.1um-CMOS technology

The TLP measurement results of the HHI-SCR (W = 40um) are depicted in Figure 7 (top: TLP-IV characteristic and leakage current evolution, bottom: close-up).

The device reveals a trigger voltage of $Vt1 \approx 8.0V$, which corresponds approximately to Vt1 of the external GGNMOS trigger. At the triggering point, the voltage snaps back initially to the GGNMOS specific holding voltage $V_{hold1} \approx 5.9V$. This behavior is in contrast to the GGSCR characteristics, where

the SCR turns on instantly at minimum injection currents without any noticeable GGNMOS on-state. Due to the low external shunt resistance $R_{SP,ext}$, the initial ESD stress is dissipated by the GGNMOS up to a current level of approximately $I_{t1,SCR} = 100mA$. At this point, the SCR is triggered due to a sufficient voltage drop across $R_{SP,ext}$, thus feeding enough triggering current into the SCR.
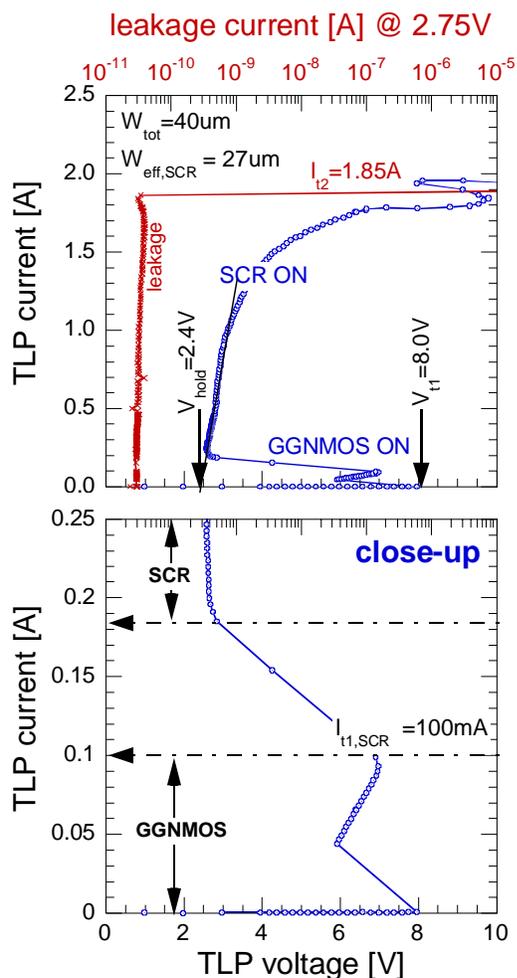

Figure 7 TLP-IV characteristic (top) and corresponding leakage current evolution of an HHI-SCR device (total width including taps W = 50um) in a 0.10um-CMOS technology. The close-up of triggering regime (bottom) with GGNMOS region and transition to SCR operation reveals a high SCR triggering current at approximately $I_{t1,SCR} = 100mA$.

At a current level of maximum 180mA, the SCR reaches its low-resistive on-state. Note that this current level Ih' does not represent the actual SCR holding current, but results from the load line of the 50Ohm-TLP tester: $(Vt1-Vh)/(It1-Ih')$
$= (7V-2.8V)/(100mA-180mA) = 52.5Ohm$.

Curve tracer measurements turning the SCR on and off in one cycle, cf. Figure 8, reveal the SCR holding current $I_{hold,SCR} \approx 68mA$ at the turn-off phase under DC conditions. This value is slightly smaller than the current at the onset of SCR triggering $I_{t1,SCR} \approx 70mA$ (turn-off / turn-on hysteresis). In comparison, the triggering current observed within the TLP IV curve was ca. 30mA higher (TLP: $I_{t1,SCR} \approx 100mA$). This reduction is caused by excessive self-heating within the SCR during static measurements. Apparently, also the SCR holding voltage is increased by approximately 1V to $V_{hold} \approx 2.4V$ due to a bipolar current gain decrease at high SCR trigger currents. This effect also supports LU safety.
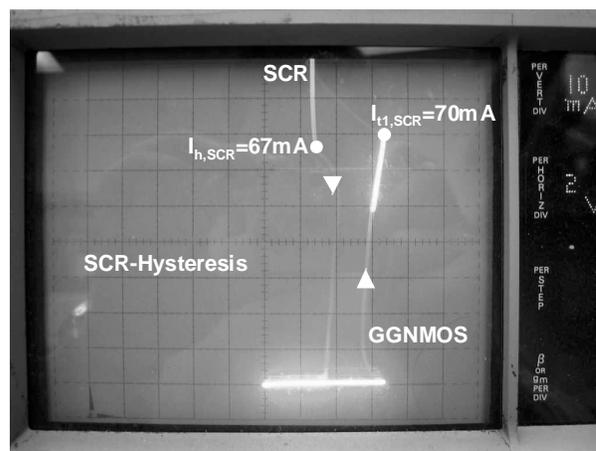

Figure 8 Curve tracer HHI-SCR IV characteristic showing the static turn-on / turn-off behavior including a slight SCR triggering-holding current hysteresis. The holding current at the lowest SCR IV point is approximately $I_{h,scr} = 67mA$.

For a number of applications in this technology, the higher holding current level is sufficient to exploit the structure as extremely area efficient power clamp. Moreover, it is suitable to be used as a LU-immune local I/O clamp, for example for PCI application, where otherwise area intensive series diodes would be required for SCR LU immunity because of the high signal current levels.

The device fails at a current level of approximately It2 =1.85A, which corresponds to a normalized ESD performance of roughly 42mA/um if the full HHI-SCR device width $W_{tot} = 40um$ is considered. Note, that the active SCR area (total effective anode or cathode width) is reduced by the intermittent well-ties, cf. Figure 6, therefore leading to a lowered normalized It2/um. Relating the ESD performance to the effective, total SCR anode/cathode width $W_{eff,SCR} = 27um$, results in a typical SCR

performance value of approximately 68mA/um.

The typical bending of the IV characteristic due to excessive self-heating before reaching It2 suggests an SCR failure mode at the contacts. The destructive pulse current level It2=1.85A is indicated by the sudden increase of the leakage current.

Due to the ideal width scaling of SCRs, the protection level according to the ESD product specification can be easily adjusted by increasing the total device width.

IV.b. 0.4um-BiCMOS

The HHI-SCR was also realized in a 0.4um-BiCMOS technology. Experimental results are shown in Figure 9 for three different variations of the number of trigger taps M = 2, 4, 10 in a symmetrical device configuration, cf. Figure 6. Note that the total anode/cathode width, i.e. effective SCR width, for all structures was kept constant. Moreover, two GGNMOS fingers W=2x50um were implemented into the HHISCR to trigger the SCR in conjunction with a voltage drop across a poly resistor at gate G1 of $R_{SP,ext}$ =2Ω.

Obviously, the SCR triggering current increases to a high levels of $I_{t1,SCR}$ = 395mA for M=10 trigger taps. This effect is accompanied by an increase of the holding voltage to approximately 2.5V, which also supports latch-up safe power protection operation.

For higher segmentation, i.e. smaller anode and cathode diffusion lengths, respectively, again different conduction modes can be distinguished: GGNMOS, SCR, GGNMOS/SCR. The latter region represents the typical current saturation regime of the SCR as clearly visible in the reference GGSCR IV curve. In the case of the HHISCR, however, sufficient voltage builds up across the SCR to re-trigger the GGNMOS. The joint current conduction leads to higher current failure levels with increasing M due to a reinforced trigger tap G1 as indicated by the leakage current evolution in Figure 9 (bottom).

The enhanced N+/Pwell diode for larger M increases efficiency of the trigger device as parallel current shunt. Since the total effective anode/cathode width is the same for all elements, a total increase of the HHISCR performance is observed with higher M.

HBM failure-levels of the HHI-SCR structures were all above 7kV. This corresponds to an HBM / TLP-It2 correlation factor of approximately 2 consistently observed in this technology.
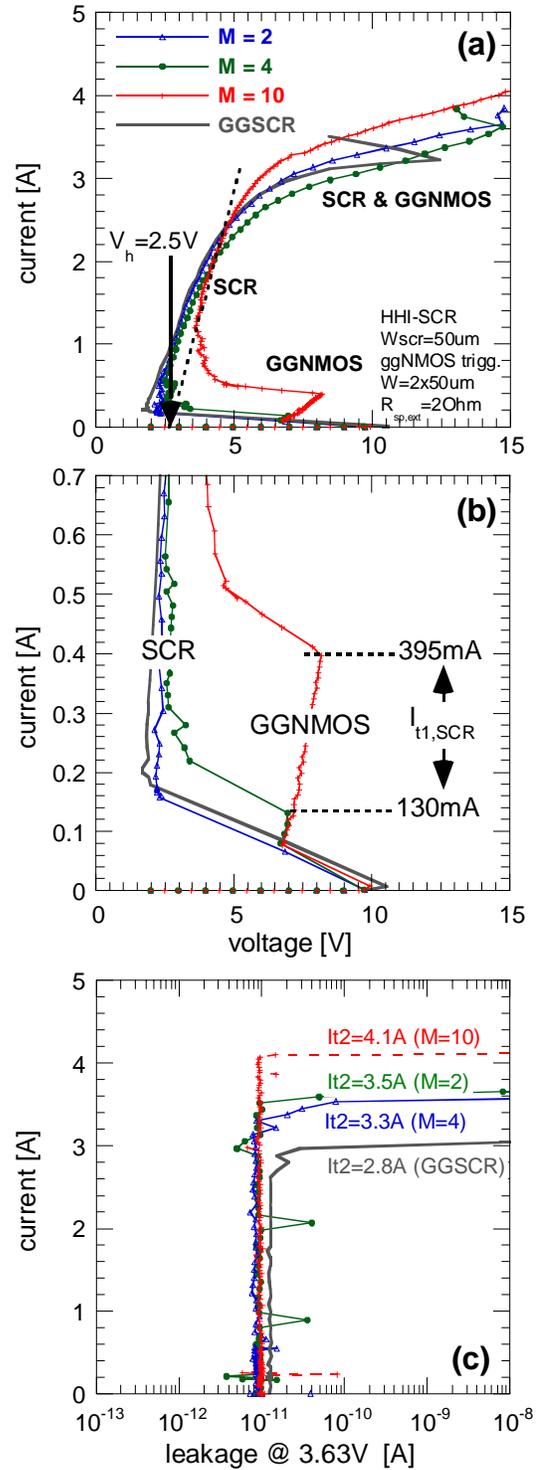

Figure 9 TLP-IV characteristic (a) / close-up (b) of three HHI-SCR variations / GGSCR reference device containing different number of well-ties M=2, 4, 10 in a symmetrical SCR configuration, cf. Figure 6. Leakage current evolution (c) indicating higher failure currents with more well-ties M.

The HHI-SCR reaches excellent values for the ESD performance per area: 3.5-4 V_{HBM}/um^2. This is a factor of 2-3 higher compared to standard GGNMOS power clamp solutions in this technology.

V. CONCLUSİONS

This paper introduces a novel SCR-type ESD protection design, the HHI-SCR, which was directly derived from the GGSCR (external GGNMOS triggered SCR) device.

Silicon proven results were obtained in a 0.10um - CMOS and a 0.4um-BiCMOStechnology.

In this structure, latch-up immunity is achieved during normal operation by increasing the holding current of the SCR to sufficiently high current levels.

The new HHI-SCR implementation comprises a number of advantages:

- In particular for applications, where the ESD design window becomes extremely narrow, this SCR-type protection allows exploiting the low-voltage clamping behavior typical for SCRs.

- The implementation is very area efficient, since no series diodes are required to increase the holding voltage above VDD. Device overhead introduced by additional well ties and reinforced trigger elements is less significant.

- A fast turn-on behavior of the SCR is ensured, since design rule minimum anode-cathode spacing can be preserved. This SCR turn-on time is relevant for the protection of thin gate oxides [1], [7]. Moreover, the trigger GGNMOS in parallel to the SCR provides a fast and efficient back-up in particular during fast ESD transients such as CDM.

- The HHI-SCR can be applied as power protection for higher supply voltages VDD > 3.3V and in particular for high-voltage applications, where the use of SCRs was not possible in the past due to an extremely high LU risk. Thus, an ESD solution can be provided for the high-voltage domain replacing the often very poor high–voltage GGNMOS-type protection clamps.

- The HHI-SCR is based on a modular approach, where an optimized design can be synthesized after analysis of the corresponding device parts. The specific behavior of all used components can be verified by separate test structures and the final device tailored regarding IC design specifications.

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About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include
- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
    - Enable unique requirements for Latch-up, ESD, EOS
    - Layout, metallization and aspect ratio customization
    - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

As is the case with many published ESD design solutions, the techniques and protection solutions described in this data sheet are protected by patents and patents pending and cannot be copied freely. PowerQubic, TakeCharge, and Sofics are trademarks of Sofics BVBA.

Version

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