Conference paper

Diode-Triggered SCR (DTSCR) for RF-ESD Protection of BiCMOS SiGe HBTs and CMOS Ultra-Thin Gate Oxides

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A novel Diode-Triggered SCR (DTSCR) ESD protection element is introduced for low-voltage application (signal, supply voltage ≤1.8V) and extremely narrow ESD design margins. Trigger voltage engineering in conjunction with fast and efficient SCR voltage clamping is applied for the protection of ultra-sensitive circuit nodes, such as SiGe HBT bases (e.g. f_{Tmax}=45GHz in BiCMOS-0.35u LNA input) and thin gate-oxides (e.g. tox=1.7nm in CMOS-0.09u input). SCR integration is possible based on CMOS devices or can alternatively be formed by high-speed SiGe HBT's.

Diode-Triggered SCR (DTSCR) for RF-ESD Protection of BiCMOS SiGe HBTs and CMOS Ultra-Thin Gate Oxides

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Abstract – A novel Diode-Triggered SCR (DTSCR) ESD protection element is introduced for low-voltage application (signal, supply voltage ≤ 1.8V) and extremely narrow ESD design margins. Trigger voltage engineering in conjunction with fast and efficient SCR voltage clamping is applied for the protection of ultra-sensitive circuit nodes, such as SiGe HBT bases (e.g. f_{Tmax}=45GHz in BiCMOS-0.35u LNA input) and thin gate-oxides (e.g. tox=1.7nm in CMOS-0.09u input). SCR integration is possible based on CMOS devices or can alternatively be formed by high-speed SiGe HBT's.

I. INTRODUCTION

Due to their excellent clamping capabilities (low holding voltage and low dynamic on-resistance), SCR's represent ideal ESD protection elements to operate within very narrow ESD design window applications, cf. Figure 1, where (GGNMOS) NPN bipolar-based protection is not feasible anymore. However, a suitable trigger element needs to be incorporated to latch the SCR sufficiently fast during ESD events and below the critical voltage limits of IC damage.

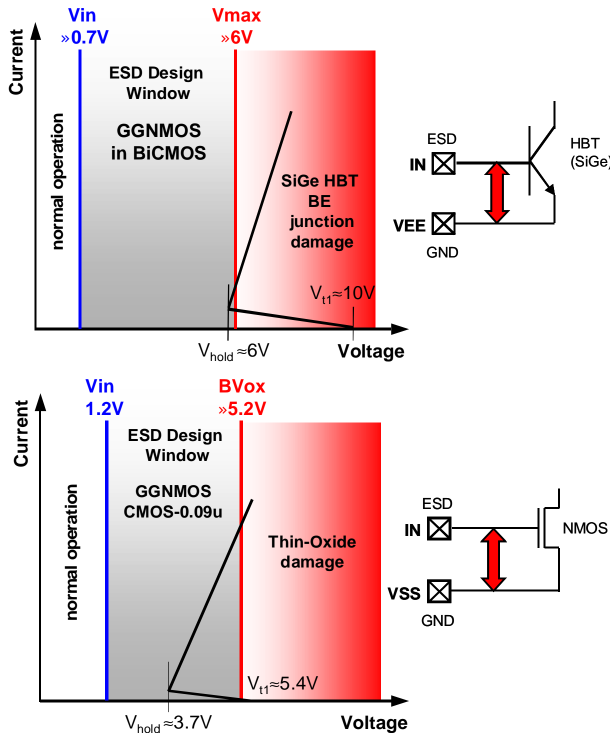

Figure 1 Narrow ESD design window IC applications. Top: SiGe HBT base protection in BiCMOS-0.35u: GGNMOS snapback trigger Vt1 and holding voltages Vhold are far above or too close to the damage level of the sensitive base-emitter junctions. Bottom: Ultra-Thin GOX input protection in CMOS-0.09u: GGNMOS trigger Vt1 and holding voltage Vhold are above / too close to the transient breakdown voltage of the ultra-thin gate oxide (tox=1.7nm).

This paper focuses on various implementations of a novel Diode Triggered SCR (DTSCR), which can be implemented based on CMOS or SiGe HBTs, respectively. In addition, two narrow design window applications will be discussed, which represent two common key issues for ESD protection design in advanced technologies: 1. SiGe HBT RF-ESD protection in BiCMOS, cf. Figure 1 (top). 2. Ultra-thin GOX protection in CMOS-0.09u, cf. Figure 1 (bottom).

II. DTSCR PROTECTION DESIGN

II.1. SCR Trigger Voltage Engineering

The DTSCR uses a trigger diode chain to latch the SCR during ESD stress conditions, when the diode string injects enough current into the SCR gates ("trigger taps") G1 or/and G2.

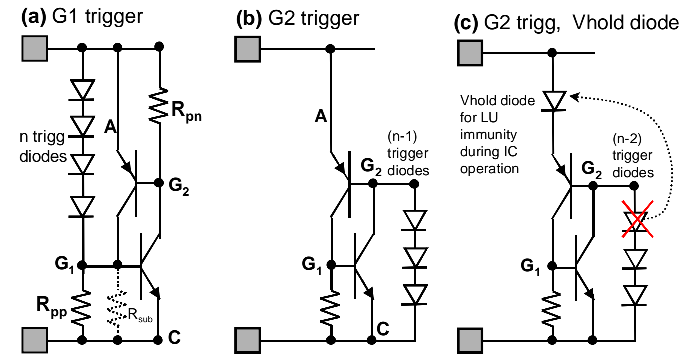

Figure 2 G1-triggered DTSCR (a): forward bias of SCR G1-Cathode junction. In CMOS-SCR an intrinsic connection to the substrate (Rsub) is present. G2-triggered DTSCR (b/c): forward bias of G2-Anode junction. Vhold diode for LU immunity allows removing one diode (c).

Triggering can either be accomplished by forward biasing the inherent SCR G1-Cathode junction, cf. **Figure 2** (a), or alternatively the G2-Anode diode, cf. **Figure 2** (b), or both simultaneously. The number of trigger diodes (n) must be chosen sufficiently high so that the chain does neither leak nor trigger the SCR during normal circuit operation. On the other hand, the SCR ESD trigger voltage is also defined by n. Obviously there is an important design trade-off between leakage during normal operation ("maximize n") and ESD

trigger voltage ("minimize n"). A reasonable design compromise can be achieved for low-voltage applications, where the supply or signal voltage does not exceed 1.8V.

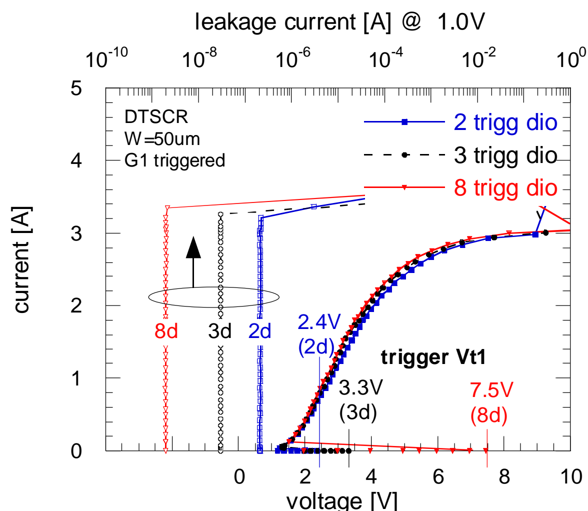

Figure 3 DTSCR Vt1 engineering: TLP-IV characteristic of DTSCR (CMOS-SCR) for three G1 trigger diode schemes: $Vt1 \approx (n+1) \cdot 0.8V$ (n trigger diodes + intrinsic SCR G1/Cdiode).

For CMOS-based SCRs, G2-triggered devices bear an important advantage: the SCR G2 (Nwell)-Anode diode can be exploited as a trigger diode within the trigger chain due to the isolation of the Nwell from the P-substrate. In contrast, in G1(Pwell)-triggered elements the diode chain sees an intrinsic Pwell-substrate connection with a leakage path to ground, cf. Rsub in **Figure 2** (a). As such, G2-triggering allows for the same diode-chain leakage during normal operation while using one trigger diode less, which is substituted by the inherent P+/Nwell (A/G2) SCR diode. Consequently, G2-triggered SCRs can be activated at an approximately 0.8V lower trigger voltage.

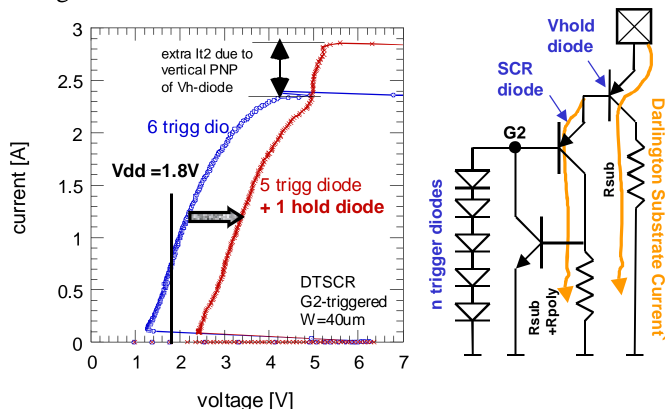

Figure 4 DTSCR latch-up engineering: TLP-IV characteristic of a G2-triggered DTSCR (CMOS-SCR) for 1.8V application with 6 trigger diodes / no holding diode compared to 5 trigger diodes / 1 holding diode. Result: approximately 1V difference in Vh, approximately same Vt1, but higher It2 with series diode due to parasitic darlington current into the substrate.

Figure 3 illustrates the Vt1 engineering technique by showing TLP-IV characteristics of various DTSCRs with different diode-chains. In this example, the SCR design is based on CMOS layers only as will be explained in the next paragraph. Alternatively, the SCR can be realized solely using SiGe bipolar device options. The implementation of both configurations is discussed in the next two chapters.

For higher VDD (e.g. if the DTSCR is used as a 1.8V supply clamp), a series diode is needed to increase the holding voltage Vhold above VDD to ensure latch-up immunity during normal operation [1], cf. **Figure 2** (c). This holding diode can also become part of the trigger chain in a G2-triggered scheme replacing one trigger diode.

Figure 4 shows the IV characteristics of two G2 triggered SCR demonstrating a holding voltage shift by approximately 1V to latch above VDD(=1.8V) using a series diode (P+/Nwell) to achieve latch-up immunity. The substitution of a trigger diode by a holding diode, does not alter the trigger voltage. Moreover, an increased maximum stress current can be observed when using a holding diode. This is due to the parasitic Darlington formed by the vertical PNPs in the device forming an additional ESD current path to GND.

An important option with a diode trigger chain, apart from triggering the SCR, is that the diodes can serve as an ESD backup path for slower SCRs by clipping possible transient trigger voltage overshoots during very fast ESD transients, such as CDM (Charged Device Model). Careful design of the trigger diodes and trigger current injection point (G1 or G2) is required to form a sufficiently strong initial ESD current path through the diodes until efficient SCR clamping sets in.

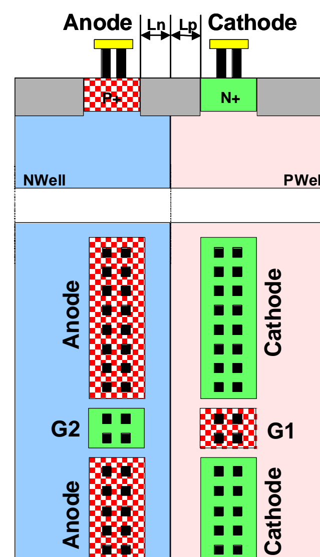

Figure 5 Cross-section / layout of a CMOS based SCR. The local G1/G2 trigger taps can be inserted between the interrupted cathode / anode diffusion, respectively [1]. In the DTSCR, a diode chain is applied to bias the wells through the gates G1/G2.

II.2. SCR integration in CMOS

Conventional CMOS design integrates SCRs purely based on CMOS layers [1], [2]. A schematic example layout and a cross-section of the SCR kernel including gate / trigger tap implementation are depicted in **Figure 5**.

II.3. SCR integration in SiGe HBT

A schematic layout and cross-section of a SiGe HBT based SCR are shown in **Figure 6**. Due to the vertical current flow from the SiGe HBT emitter to collector, the SCR will benefit from the high currents that can flow in a vertical bipolar

structure in contrast to lateral bipolar conduction in a lateral SCR. As demonstrated in **Figure 7**, the ESD performance in terms of maximum current It2 and HBM level drastically increases implementing more contact rows in anode and cathode, respectively, due to the reinforced vertical junction area.

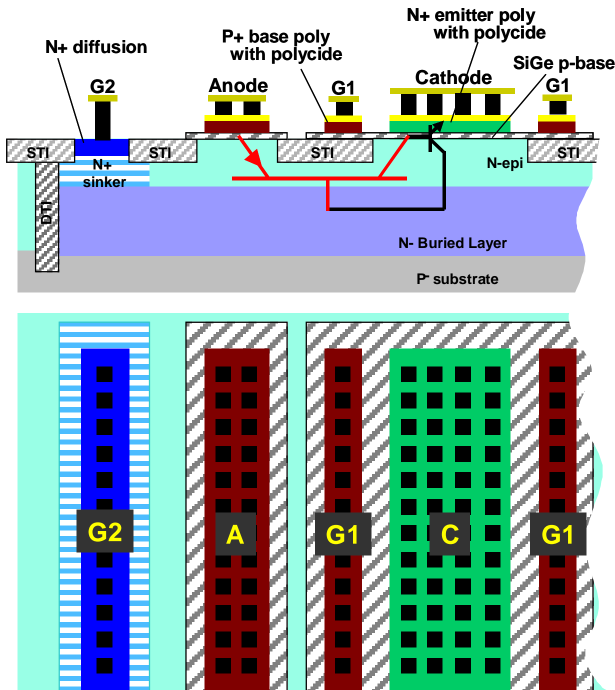

Figure 6 Cross-section and layout of SiGe-HBT based SCR (not shown: external diode-chain trigger scheme that can be integrated through G1, or G2, or G1 and G2). The symmetrical SCR device is formed by a vertical NPN HBT (emitter/SiGe-base/N-epi) in conjunction with a distributed PNP bipolar (Anode/N-epi/SiGe-base). Note: alternatively the same intermittent trigger taps as shown in Figure 4 could be used replacing the solid G1/G2 stripes.

Furthermore, the SCR holding voltage is relatively small (Vhold~1.1V) as compared to regular CMOS implementations reflecting the high transistor current gain of the SiGe HBT part of the SCR.

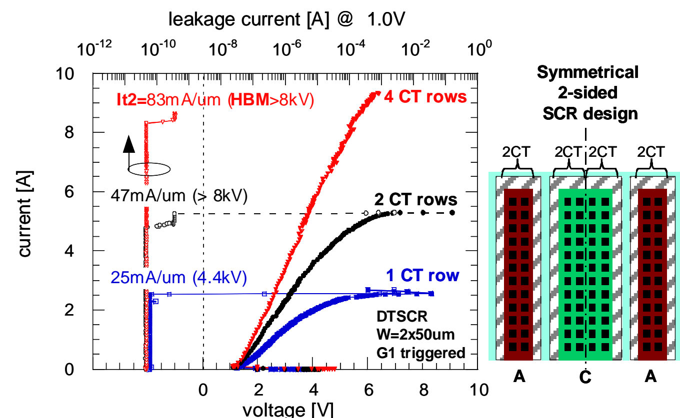

Figure 7 HBT-based DTSCR (W=2x50u; 2-sided) TLP-IV for three different variations of number of contact rows in anode and cathode, respectively. The performance boost with larger number of contact rows reflects the predominant vertical current flow in HBT based SCRs.

An interesting benefit of the described SiGe HBT-SCR is the fact that the SCR is fully isolated from the substrate. As a consequence, the gate G1 can be treated the same as G2 (see discussion above: G1-trigger vs. G2-trigger). This allows simultaneous G1/G2 triggering with identical diode chains on both gates. Dual-gate triggering enhances the SCR speed [3] and thus helps to avoid transient trigger voltage over-shoots during the device turn-on time.

Moreover, due to the complete device isolation from the substrate, DTSCRs can also be applied as local protection element between IO and supply. A further benefit is the device immunity to latch-up induced by substrate current injection.

III. DTSCR RF-ESD APPLICATION

III.1. Input SiGe HBT Base in BiCMOS-0.35u

SiGe HBT (f_{Tmax}=45GHz) emitter-base protection applying the conventional dual-diode protection approach in conjunction with an NMOS-triggered SCR power clamp, see **Figure 8,** is ineffective. Reason is the very low base-emitter failure voltage (~6V), which is already exceeded by the power-clamp trigger voltage as defined by the NMOS holding voltage (V_{hold}~6V). This situation is illustrated in the ESD design window in **Figure 1** (top).

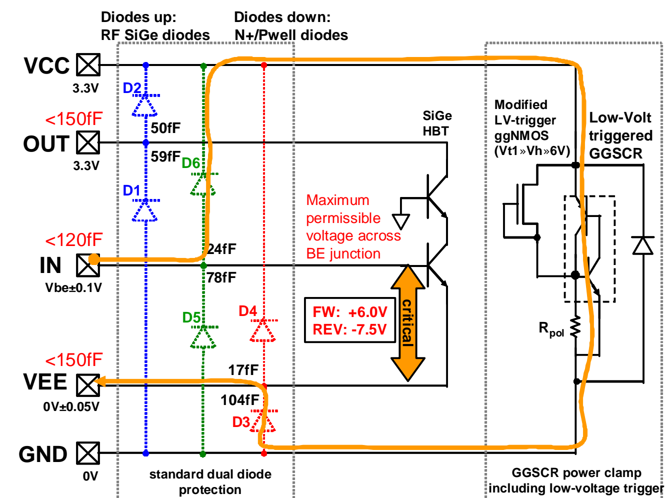

Figure 8 LNA including conventional dual-diode protection approach for output, input, and emitter pad. ESD protection scheme fulfills the capacitance specs at each pin (C(V) numbers calculated by SPICE parameters). Serious ESD issues occur since the NMOS-triggered power clamp has a higher Vt1 than failure voltage of forward biased SiGe HBT base-emitter (BE) junction. The most critical ESD current path is indicated.

Moreover, a direct local diode chain protection between Input and VEE (for both pins a capacitance spec is defined) compromises the RF performance because of a too high diode cathode capacitance (also increased by the forward bias).

Introducing a diode chain between Input and GND violates the ESD design window: for worst-case stress between IN and VEE, 4 width-limited RF diodes (high series R!) would compete with the parasitic HBT BE diode in forward conduction.

Local DTSCR protection as shown in **Figure 9** succeeds for three reasons: 1. By applying three small trigger diodes in series, the SCR Vt1 can be reduced sufficiently below the critical HBT failure voltage at 6V with an acceptably low input leakage during normal RF operation. 2. The SCR clamps the IN-VEE voltage below the HBT damage, thus enabling the challenging 200V-MM spec (roughly corresponds to 4kV-

HBM). 3. To meet the input RF capacitance spec Cin<120fF, the SCR-Nwell can be pulled high to VCC through G2, thus, reverse biasing the SCR Anode-Nwell junction minimizing the parasitic capacitance of the Anode at IN.

The TLP characteristic in **Figure 10** corroborates the functionality of the DTSCR ESD protection revealing the following IV regimes: HBT BE diode conduction, DTSCR triggering, joined HBT/DTSCR conduction (see inset including ESD current path for most critical stress case), HBT failure after input voltage exceeds the critical HBT failure limit of 6V.

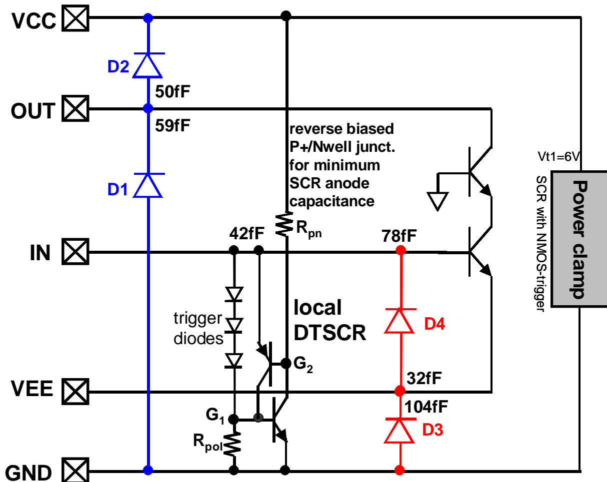

Figure 9 LNA including local DTSCR protection of HBT in conjunction with application of capacitance reduction scheme for the anode by reverse biasing the P+/Nwell junction. All pin combinations exceed ESD spec of 2kV-HBM and 200V-MM spec (latter corresponds to approx 4kV-HBM), whereas RF capacitance spec is also met.

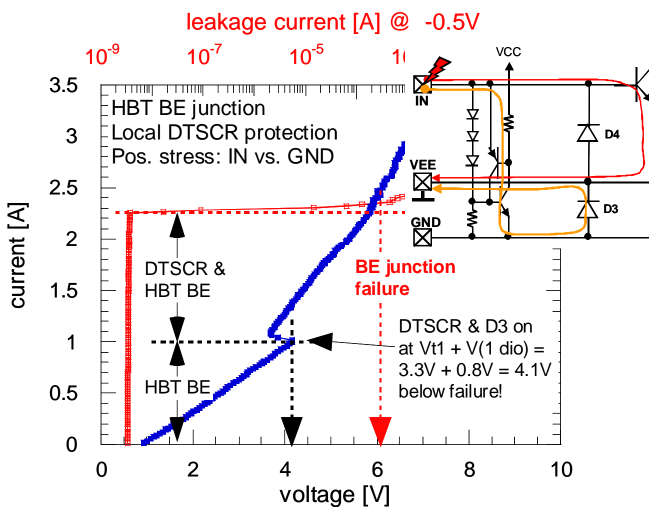

Figure 10 LNA TLP-IV characteristic: worst-case stress (positive on Input vs. VEE on ground) protected by local DTSCR, cf. **Figure 9**: the DTSCR triggers and clamps the voltage below HBT base damage. The ESD spec of 2kV-HBM and 200V-MM can easily be achieved within the RF capacitance constraints.

III.2. Input Ultra-Thin GOX in CMOS-0.09u

Figure 11 depicts the TLP-IV characteristics of two DTSCRs in a G1- and G2-triggered configuration, respectively. Both structures have the thinnest NMOS gate oxide (tox=1.7nm) as a protection monitor in parallel to emulate an RF IC input configuration, see figure inset. Note that the G2-trigger scheme essentially results in the same leakage current as compared to the G1-triggered SCR. However, the G2-triggered SCR reveals a lower trigger voltage Vt1, since one trigger diode less can be used as explained above. The leakage increase at It2 indicates gate-oxide failure occurring within the high-resistive roll-off regime of the SCR IV curve. So, almost the intrinsic failure current of the stand alone SCR is achieved. This experiment proves that the SCR can successfully protect a thin input gate oxide. The large margin of Vt1 and clamping voltage with regard to BVox provides a large IC ESD design window for ESD protection on IC level, where additional voltage drops occur in the ESD discharge path e.g. across bus resistance and diodes. The experiment with parallel gate monitor demonstrates that the DTSCR structure is able to protect ultra-thin gate oxides.

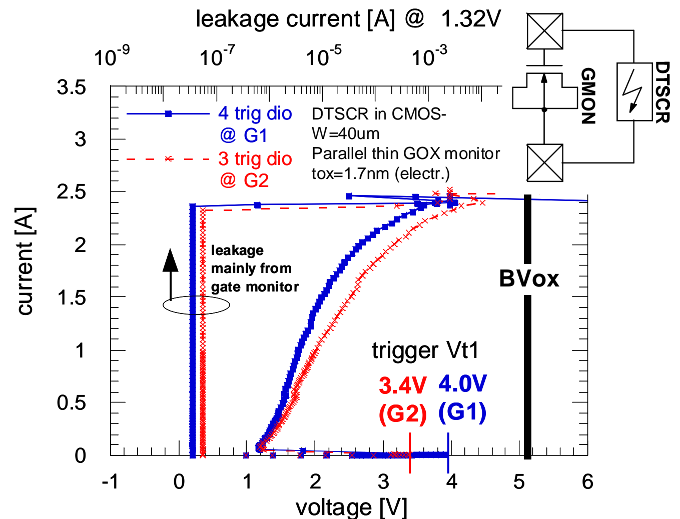

Figure 11 CMOS-0.09u: TLP-IV characteristic of DTSCR including a parallel gate-oxide (tox=1.7nm) monitor to emulate IC input protection. The thin GOX can be successfully protected!

IV. CONCLUSION

This paper presents a novel diode-chain triggered SCR ESD protection element for low voltage applications (signal, supply ≤ 1.8V). The DTSCR enables ESD protection design of ultra-sensitive IC nodes within extremely narrow ESD design windows, such as SiGe HBT emmitter-base junctions (advanced BiCMOS) or ultra-thin gate oxides (sub-0.25u CMOS). Conventional CMOS-integrated DTSCRs as well as SCR-based on high-speed SiGe HBT elements were successfully proven in product ICs.

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[2] M. Mergens, C. Russ, K. Verhaege, J. Armer, P. Jozwiak, R. Mohn. *High Holding Current SCR (HHI-SCR) for ESD Protection and Latch-up Immune IC Operation.* EOS/ESD 2002, pp. 10.

[3] K-C Hsu, M-D. Ker. *Double-Triggered SCR Devices for On-Chip ESD Protection in Sub-Quarter-Micron CMOS Processes.* EOS/ESD 2003, in press at time of submission.

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Notes

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Version

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