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This paper presents a novel active-source-pump (ASP) circuit technique to significantly lower the ESD sensitivity of ultrathin gate inputs in advanced sub-90nm CMOS technologies. As demonstrated by detailed experimental analysis, an ESD design window expansion of more than 100% can be achieved. This revives conventional ESD solutions for ultrasensitive input protection also enabling low-capacitance RF protection schemes with a high ESD design flexibility on IC-level. ASP IC application examples and the impact of ASP on normal RF operation performance are discussed.

Active-Source-Pump (ASP) Technique for ESD Design Window Expansion and Ultra-Thin Gate Oxide Protection in Sub-90nm Technologies

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I. Abstract

This paper presents a novel active-source-pump (ASP) circuit technique to significantly lower the ESD sensitivity of ultra-thin gate inputs in advanced sub-90nm CMOS technologies. As demonstrated by detailed experimental analysis, an ESD design window expansion of more than 100% can be achieved. This revives conventional ESD solutions for ultra-sensitive input protection also enabling low-capacitance RF protection schemes with a high ESD design flexibility on IC-level. ASP IC application examples and the impact of ASP on normal RF operation performance are discussed.

II. Introduction

With further downscaling of feature size in advanced CMOS technologies, thin and ultra-thin gate oxide (GOX) protection becomes increasingly challenging [1]-[3]. This critical trend is corroborated in Figure 1, which depicts experimental Transmission Line Pulse (TLP: 100ns square pulse width) results for technologies down to 75nm.

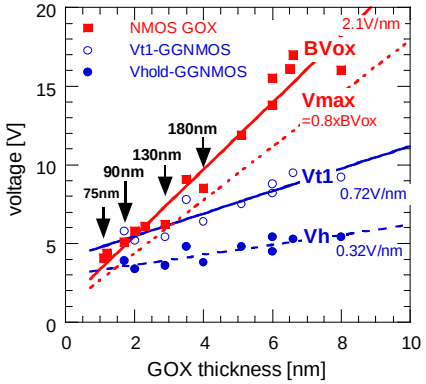

Figure 1 Transient GOX breakdown and GGNMOS TLP parameters (trigger Vt1 and holding voltage Vhold) as a function of physical GOX thickness in various CMOS technologies (0.18u - 0.075u). Technology advancement results in a dramatically narrowed ESD design window Vmax.

The plot shows a rapid decay of the transient gate oxide (GOX) breakdown voltage BVox as a function of the physical GOX thickness (here NMOS GOX with area <40u^2). As a consequence of the fast BVox decrease, the ESD design window, cf. Figure 2, for the protection of a thin GOX input on IC-level is dramatically narrowing down. The upper limit V_{max}, which is used for IC ESD protection design, is derived from BVox by subtracting a certain safety margin (typically about 20% as also depicted in the plot). Then, the V_{max} level must be experimentally verified by endurance TLP tests (~1000 repetitive TLP pulses at V_{max}) with continuous leakage current monitoring and check of potential MOS characteristic degradation comparing fresh vs. stressed device. Typical ESD design window margins V_{max}-VDD (supply) range only between 2.5V to 3.5V for inputs containing ultra-thin gate oxides in sub-90nm technologies.

Grounded-Gate NMOS (GGNMOS) transistors are most widely applied for ESD protection design. Figure 1 shows the decisive ESD clamp parameters of such a device as a function of technologies advancement: the inherent parasitic NPN snapback trigger voltage Vt1 and holding voltage Vhold, cf. schematic IV curve in Figure 2, come extremely close to the transient BVox and eventually exceed V_{max}! As a result of these insufficient GGNMOS clamping capabilities, pure (parasitic) bipolar protection of ultra-thin GOXs is not feasible anymore for advanced sub-90nm technologies.

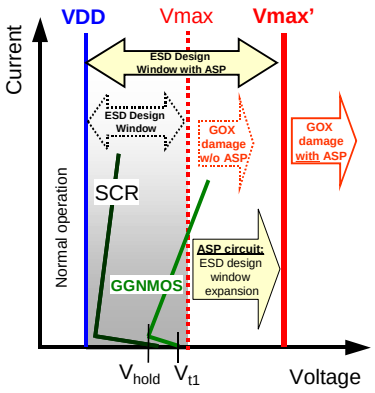

Figure 2 Schematic ESD Design Window including typical SCR / GGNMOS protection IV curve. The ASP ESD design window expansion is indicated.

This fact has a direct negative impact on high-speed IO cell design applying the thin-GOX transistors as output driver: the common concept of self-protecting MOS drivers also protecting the input GOX does not function anymore because of input damage. Moreover, even for excellent SCR voltage clamps (cf. schematic IV curve in Figure 2) optimized for ultra-thin GOX protection [2], the narrow ESD design window poses extreme challenges as will be discussed below.

For the first time, this paper presents an innovative circuit technique called active-source-pumping (ASP), which allows coping with these protection challenges by potentially expanding the effective ESD design window (cf. Figure 2: V_{max}'>V_{max}) by up to more than 100% for ultra-thin GOX. In the next section TLP breakdown analysis results for ultra-thin GOXs in a 90nm-CMOS technology are provided. Next, the novel ASP circuits will be introduced including a detailed explanation of the corresponding experimental data evidencing the largely relaxed ESD boundaries. A separate section is devoted to application examples and a brief discussion on the DC/AC impact of the ASP ESD circuit on normal operation performance.

III. Ultra-thin GOX TLP Analysis

An interesting finding in advanced CMOS technologies is the experimental fact that the transient gate-to-bulk oxide breakdown can occur at drastically higher voltage levels as compared to the gate-to-source/drain breakdown. As illustrated by the TLP data in Figure 3, the source-side stress reveals the characteristically low damage level of approximately BVox(G-S)~5V, whereas the gate-bulk breakdown appears at more than a factor of two higher values BVox(G-B)>12V. This effect was verified for many samples on different dies/wafers with the worst-case breakdown characteristic indicated in the plot (BVox(GB)~12V). Not depicted is the leakage current, which was monitored after each stress event remaining constant up to the point, where the IV characteristic notably changes and the BVox is indicated. Similarly pronounced differences regarding difference in BVox to source vs. bulk were observed in other technologies as well.

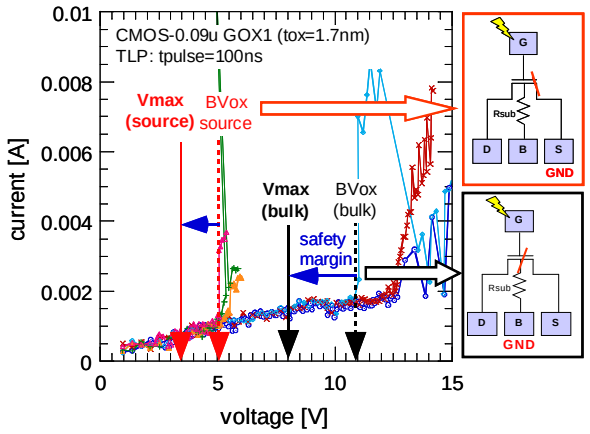

Figure 3 Transient GOX (tox=1.7nm, W/L=20u/0.5u) breakdown for gate-bulk TLP stress (left) and gate-source TLP stress (right) in CMOS-90nm. BVox to bulk is significantly higher than to source.

Device simulation results presented in [4] can explain the different TLP breakdown shown in Figure 3, which is caused by the higher electrical field that exists at the gate edge.

For ESD IC design, we can conclude that to protect advanced thin gate oxides a predominant focus must be put on limitation of the most critical gate-source ESD voltage. But note that two important conditions must be fulfilled first: 1. a particularly large safety margin for V_{max}(GB) of more than 30% regarding BVox(GB) should be introduced as indicated in Figure 3 to account for potential BVox fluctuation e.g. due to extrinsic GOX breakdown. Secondly, the resulting V_{max} definition must be experimentally verified for multiple samples with no degradation after TLP endurance stress tests as discussed above.

IV. Active-Source-Pump ASP Schemes

Figure 4 (left) illustrates the general ASP concept for a simple input inverter including generic placeholders for main IO ESD protection elements (e.g. diodes or local clamps). The ASP scheme consists of source-pump devices inserted between the IO line and the internal source node of the inverter MOS transistors in series with a source resistor Rs. This source resistor can either be formed by the (silicide-blocked) source junction diffusion or by separate (diffusion or poly) resistor. The maximum permissible Rs (~10-50Ω) would depend on the specific IC application not compromising normal IC operation as will be discussed below.

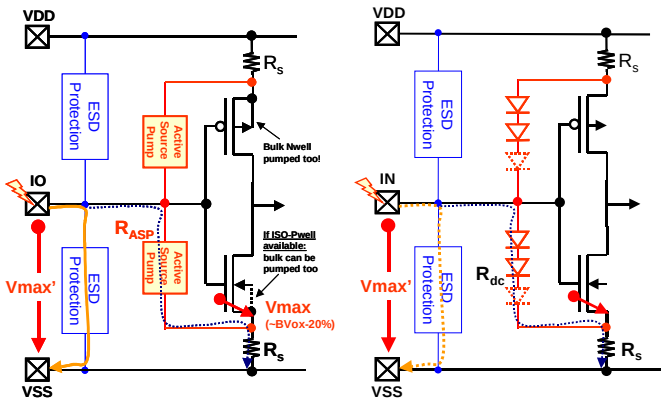

Figure 4 Generic scheme illustrating the active-source-pump technique also being used to pump the bulk (left). Specific implementation of active source-pump scheme applying diode chains in conjunction with source resistors for the NMOS and PMOS in an input inverter stage (right). Note that the orientation of the diodes is defined for the worst-case stress polarity.

To limit the effective voltage at the gate during ESD stress conditions, the ASP technique lifts the source potential of the endangered MOS transistor. This is achieved by activating the ASP circuit at a certain voltage level well below the maximum allowed voltage across the thin GOX V_{max} (definition of V_{max} see above). Note that different critical stress cases must be distinguished, which are often represented by positive ESD on IO vs. VSS for the NMOS and positive ESD on VDD vs. IO for the PMOS, respectively. The ASP must trigger the source biasing mechanism for exactly these stress events. Once the ASP is turned on, the circuit starts to inject minor amounts of ESD current into the source resistor R_S as indicated for IO vs. VSS stress in Figure 4. In this case, it is a also assumed that the main ESD current is conducted thru the protection device between the same pins. Due to the voltage drop across R_S, the NMOS source potential V_S rises. This reduces the total ESD voltage across the endangered gate-source oxide $V_{GS}=V_{IN}-V_S$, which often represents the most sensitive IC part, cf. Figure 3. Due to the source bias, a higher total transient gate bias $V_G=V_{max}$' can be tolerated before the low ESD voltage limit V_{max} directly across the GOX is reached. The ASP on-resistance R_{ASP} and the source resistor R_S act as a voltage divider, which results in an analytical expression for the increased ESD design margin

$$V_{max}' = (1 + R_S / R_{ASP}) \cdot V_{max}$$

Assuming an ASP design with $R_S = R_{ASP}$, a 100% increase of the ESD design window, i.e. $V_{max}' = 2 \cdot V_{max}$ can be achieved.

Important to mention is that **the ASP scheme can also be applied to simultaneously pump the MOS bulk**. In the PMOS this is easily achievable by connecting the "isolated" Nwell to Rs instead of directly to VDD. This is always recommended not needing to rely on the BVox bulk effect

described in the previous section. For the NMOS transistor, the use of deep-Nwell is advisable to enable efficient ESD potential increase within the now substrate-isolated Pwell. Advantageous is the fact that many RF technologies with ultra-high-speed (thin GOX input!) applications have the deep-Nwell available for noise isolation purposes anyway.

A specific ASP design example is presented in Figure 4 (right) employing a diode chain as ASP circuit. Such a design is applicable in low-voltage domains (e.g. Vin=VDD≤1.2V) where 3 diodes can sufficiently limit the normal operation leakage current to acceptably low values. Note that these diodes can be relatively small in size thus having only very limited parasitic capacitance (order of magnitude ~15fF). During ESD stress conditions, the diodes would need to provide a high enough current (~100mA) to produce a substantial voltage drop across the source resistor R_S ~ 10-50Ω. Note that a resistance R_S increase with higher ESD current will enhance the ASP function as explained below.

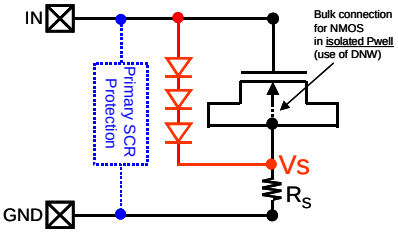

Figure 5 Ultra-thin GOX input emulation test-structure implemented in a 90nm-CMOS technology including ASP diode chain scheme in conjunction with source resistors.

V. Experimental ASP Input Analysis

Figure 5 represents a dual-pad input emulation structure for ASP test-chip implementation. These test elements allow for a detailed experimental analysis of the thin GOX ESD design window expansion and ASP circuit optimization. The device contains a NMOS input transistor with its gate connected to one pad (IN), whereas the shorted drain and source are hooked up thru a "source" resistor R_S to the second pad (GND). The R_S poly resistor width was dimensioned large enough to support at least 100mA in ESD current. In case of an isolated Pwell (use of deep Nwell), also the bulk is connected to R_S instead of directly to GND. This allows reducing the effective gate-bulk voltage simultaneously to gate-source. The ASP diode chain is inserted between IN and the shorted drain-source node. Additional test elements can contain a main ESD clamp between the two terminals to simulate a fully protected gate oxide including ASP scheme.

Figure 6 depicts the TLP analysis results (positive pulse polarity for IN vs. GND) for the test structure in Figure 5 containing a source resistor of R_S=10Ω (top) and R_S=25Ω in regular Pwell / isolated Pwell (DNW), respectively (bottom). Obviously for voltages below approximately 3V, no significant amount of current can flow thru the diode chain in series with R_S. At higher ESD bias the diodes start to conduct resulting in a pumping of the source/drain node and thus in a reduced V_{GS}=V_{GD}. At elevated currents, the linear IV curve regime bends into an IV roll-off that is characteristically for poly resistors under high current conditions. This roll-off leads to an effective R_S increase and generally does not degrade the resistor below a certain current limit. Due to a more efficient voltage divider (higher ratio R_{ASP}/R_S) a larger V_{max}' and thus a further relaxed design window is supported according to the formula above. In case of R_S=10Ω (bottom plot), the upper ESD design margin limit can be increased to approximately V_{max}'=6V as indicated by a constant leakage current evolution up to the point where the poly resistor is blown open as shown by a rapid leakage drop and voltage increase. The initial leakage current increase before poly open could indicate that the GOX is damaged firstly. These results corresponds to a significant 50% increase of the original most critical ESD design margin V_{max}=4V in Figure 3. The measurement results were verified for slow (TR=10ns) and fast TLP rise times (TR=200ps), respectively, hence ensuring that ASP reacts fast enough also for very fast ESD transients such as CDM.

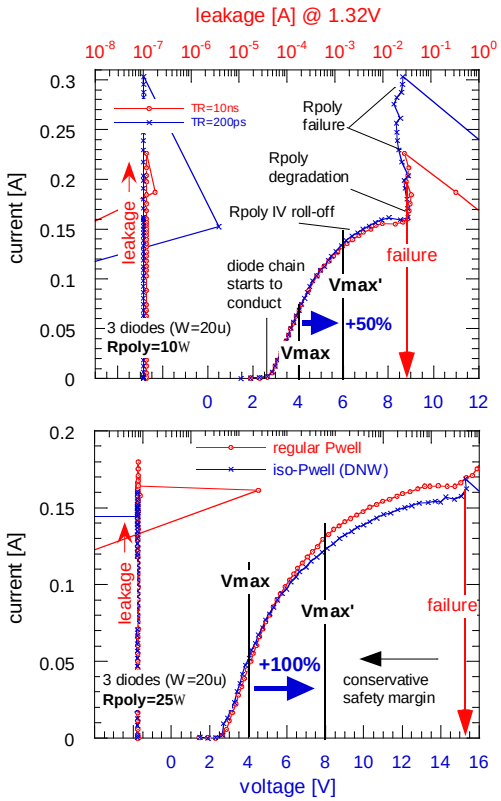

Figure 6 TLP-IV characteristic (90nm-CMOS) including leakage current evolution for the input emulation structure in Figure 5 applying a R_S=10Ω (top) and R_S=25Ω (bottom). A design window expansion of (more than) 40% (top) / 100% (bottom) including conservative safety margins can be achieved.

The bottom diagram in Figure 6 reveals a V_{max}'=8V for R_S=25Ω, which is equivalent to a 100% push-out of the critical ESD design limit V_{max}. In addition to the regular Pwell NMOS, also a structure variation containing an isolated Pwell connected to R_S was investigated. The same ESD design increase can be achieved. Note that in both cases discussed above a very conservative safety margin definition for the extracted V_{max}' was considered concerning the damage level.

VI. ASP IC IO Application Examples

As outlined in the introduction, protecting an ultra-thin GOX within an RF input is extremely challenging. Since local ESD clamps are not acceptable for many RF-IO designs due to a too high load capacitance, diode concepts (e.g. dual-diode protection, cf. Figure 7 (right)) with minimum capacitance are required. Moreover, secondary clamps applying an input gate resistor to separate secondary from primary elements will also compromise RF performance due to detrimental gate delay and RF speed loss.

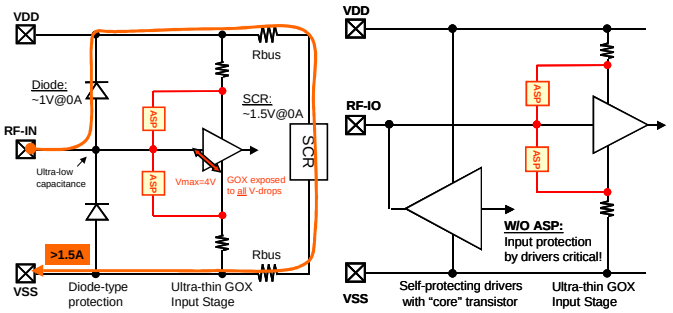

Figure 7 Two ASP application examples: RF input applying diode-type protection (left). Self-protecting driver transistor concept for RF-IO (right).

For worst-case ESD stress conditions RF-IN vs. VSS in Figure 7 (right), the VDD diode, the power protection clamp (here: SCR!) and the bus resistance are involved in the ESD current path. All the resulting voltage drops are exposed to the ultra-sensitive GOX of the NMOS. Considering the diode cut-in voltage ~1V and the SCR holding voltage ~1.5V (meaning at ~1V+1.5V=2.5V these elements in series start to conduct ESD current!), there is only ~4V-2.5V=1.5V margin left to shunt for instance 1.5A in stress current (~2kV-HBM). Consequently, less than 1Ω total resistance would be permissible for R_{SCR} plus R_{diode} plus R_{BUS} to successfully protect the input – practically impossible! The ASP V_{max} expansion can boost the maximum permissible resistance thereby enabling ultra-low capacitance RF input protection.

Another important area of ASP applications is related to high-speed IO design applying the most sensitive core transistor for self-protecting MOS drivers and input transistor, cf. Figure 7 (right). The ASP scheme can revive conventional MOS drivers for self- as well as ultra-thin GOX input protection.

Normal operation interference of the ASP circuit within the input stage (neglecting minor ASP capacitance) is caused by a source de-biasing effect due to the $I_{DS}RS$ voltage drop. This leads to a slight shift in the operation point, i.e. a smaller effective gate-source voltage. A rough estimation of the impact for an NMOS width of W=10u, a positive gate bias of $V_{IN}=V_G=1.2V$, and a source resistor $R_S=10–25\Omega$, provides a source de-biasing value of V_S~0.5mA/um·W·R_S = 0.05-0.125V. The maximum de-biasing of ~10% would roughly result in a 20% I_{DS} reduction. The lowered performance can easily be compensated by an increase of the inverter MOS widths by roughly 20%. As also confirmed by SPICE simulation, the DC switch points can be closely matched by minor width tweaks. Within a feasibility study, small signal SPICE simulation of an RF inverter stage allowed quantifying the AC impact of a source resistor R_S. Compared to a reference inverter without any external R_S an almost identical frequency response up to 10 GHz was observed. The bandwidth was reduced by less than 2% only.

As shown in Figure 8, alternatively to the R_S resistor in the conventional ASP scheme, a second MOS transistor can be exploited as frequently present in for instance cascode NMOS transistors of LVDS inputs.

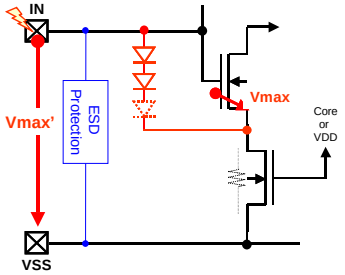

Figure 8 Typical cascoded NMOS configuration including ASP diode chain for source pumping of the jeopardized upper NMOS.

Generally, the normal operation interference of the ASP circuit should be considered well in advance for complex RF applications during the actual IO design phase. Embedding the ASP scheme into a comprehensive "RF-ESD co-design" concept allows simultaneously trading-off and optimizing ESD /RF performance. In addition, the introduction of additional elements e.g. to bridge R_S for ultra-high frequency signals can be efficiently explored.

VII. Conclusions

This paper presents a novel active-source-pump (ASP) circuit technique, which can extensively expand the ESD design window by 50% to up to more than 100% for ultra-thin GOX protection in advanced sub-90nm technologies. This significant advancement is achieved by minor ESD current injection into a source / bulk resistor effectively reducing the gate-source/gate-bulk ESD voltage. ASP has proven in particular useful in RF-IOs to allow for conventional MOS driver self-/input protection as well as in RF-inputs to enable low-capacitance solutions. Other input schemes containing a thin-GOX can also be equipped with the ASP circuit. Normal operation RF interference can be compensated in many applications by minor input width adjustments. Embedding the ASP scheme into a comprehensive "RF-ESD co-design" concept for advanced RF applications allows eliminating many potential issues.

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Notes

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