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Conference paper Advanced SCR ESD Protection Circuits for CMOS / SOI Nanotechnologies

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This paper reviews the application of SCR-based ESD protection circuits in advanced CMOS/SOI technologies. The devices are integrated in a flexible modular circuit design technique allowing for independent optimization of key characteristics. The IC application focus is on sensitive IOs, i.e. (ultra-) thin GOX input protection and robust output driver design using SCRs. Moreover, SCR transfer and integration into advanced SOI technologies is discussed. RF ESD principles are considered as well.

Advanced SCR ESD Protection Circuits for CMOS / SOI Nanotechnologies

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Abstract - This paper reviews the application of SCR-based ESD protection circuits in advanced CMOS/SOI technologies. The devices are integrated in a flexible modular circuit design technique allowing for independent optimization of key characteristics. The IC application focus is on sensitive IOs, i.e. (ultra-)thin GOX input protection and robust output driver design using SCRs. Moreover, SCR transfer and integration into advanced SOI technologies is discussed. RF ESD princinples are considered as well.

I. Introduction: ESD Design Challenges

This chapter introduces the characteristic ESD protection design challenges in advanced Nanotechnologies with a particular focus also on RF applications. Embedded into this context are the corresponding ESD solutions to be presented in this paper.

I.1. Narrow ESD Design Windows due to Ultra-thin GOX

With further downscaling of feature size in advanced CMOS technologies, protection of thin and ultra-thin gate oxides (GOX, tox < 2nm) becomes increasingly challenging [1]-[4]. This critical trend is corroborated in Figure 1 showing Transmission Line Pulse (TLP: 100ns square pulse) results for CMOS technologies down to 65nm [3].

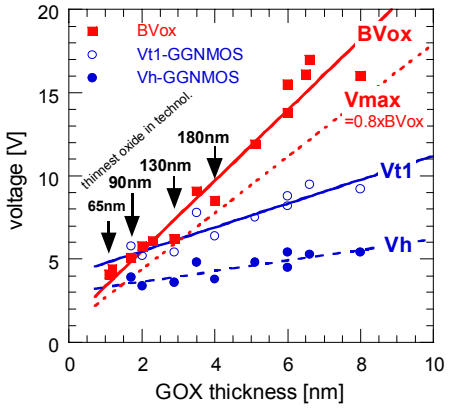

Figure 1 Transient breakdown of NMOS GOX (area <40u^2) and corresponding GGNMOS trigger voltage Vt1 and holding voltage Vh as a function of physical GOX thickness in various CMOS technologies (0.18u - 0.065u). Technology advancement results in a continuous narrowing of the ESD design window for input protection.

The plot depicts a rapid decay of the transient GOX breakdown voltage BVox as a function of the physical GOX thickness. As a result of the strong BVox decrease, the ESD design window for input GOX protection, cf. Figure 2 (left), is dramatically narrowing down in advanced technologies. The upper limit V_{max} (considered for ESD design on IC level) is derived from BVox by subtracting a safety margin of typically about 20%, to account for the typical statistical spread due to process fluctuation and potential MOS parameter drift before hard damage. Typical design window widths V_{max}-VDD range between 2.5V to 3.5V for ultra-thin gate inputs in sub-90nm CMOS technologies.

Grounded-Gate NMOS (GGNMOS) transistors are most widely applied for ESD protection design. Figure 1 also illustrates the evolution of the critical GGNMOS snapback parameters (i.e. parasitic NPN trigger voltage Vt1 and holding voltage Vh indicated in Figure 2) with technologies advancement. Apparently, both these values come close to or even exceed BVox and V_{max}. As a consequence of the insufficient GGNMOS voltage clamping capability in these very advanced technologies, pure (parasitic) bipolar protection of ultra-thin GOXs is not feasible anymore.

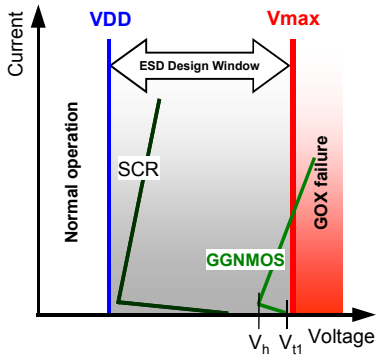

Figure 2 Schematic ESD Design Window including typical GGNMOS and SCR TLP-IV curves indicating NPN triggering Vt1 and holding voltage Vh.

As schematically indicated in Figure 2, SCRs exhibit a superior clamping behavior as compared to NMOS- or bipolar based devices due to the typically low holding voltage and on-resistance achievable with small silicon area. Different SCR circuits will be presented in this paper such *as Grounded-Gate NMOS triggered SCRs (GGSCRs) and Diode-chain triggered SCR (DTSCR). Latter elements* are capable to protect ultra-thin gate oxides due to a sufficient transient voltage clamping. One section will summarize design measures to enhance SCR trigger speed, which is a crucial prerequisite to protect these highly sensitive nodes.

I.2. RF ESD Protection Design

Among other requirements, such as minimum RF noise, high-speed interfaces require very low capacitive ESD devices. Therefore, frequently diode protection schemes replace high capacitive local protection solutions. Figure 3 shows a generic example of a dual-diode configuration connected to an ultra-thin GOX input inverter. For worst-case ESD stress conditions (positive on RF-IN vs. VSS on GND), the VDD diode, the power clamp, and the bus resistance Rbus are

involved in the ESD current path. As a result, the sensitive GOX of the NMOS is exposed to the sum of ESD voltage drops. The following calculations demonstrate why excellent power clamps are necessary to enable GOX protection (without any secondary-type clamping as discussed below).

According to Figure 1, a thin GOX in a 90nm technology reveals a maximum ESD voltage rating of roughly Vmax~4V. Due to the diode cut-in voltage of Vd0~1V and the holding voltage of the GGNMOS power clamp Vh~3.0V, the protection solution in Figure 3 is already situated outside of the ESD design window without conducting any significant ESD current. To escape the 'zero' ESD robustness, more efficient ESD voltage clamps are required. One option is the application of SCRs, which start to conduct a considerable amount of ESD current at approximately Vh~1.5V. An SCR power clamp allows a rough margin of Vmax - Vd0 – Vh=(4V-1V-1.5V) = 1.5V to shunt the stress current. For a ~2kV-HBM ESD spec (corresponding to a 1.3A peak current), a total resistance of only 1.5V/1.3A=1.2Ω is permissible for $R_{SCR} + R_{diode} + R_{BUS}$ within the discharge path, also indicating the importance of low protection on-resistance.

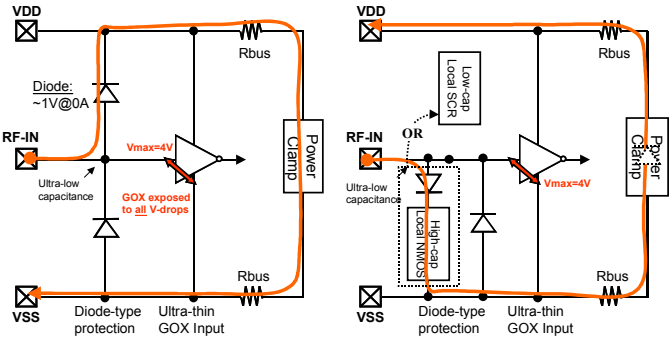

Figure 3 Generic RF input applying a low-capacitance dual-diode ESD protection concept. The yellow line indicates the discharge path for worst-case ESD stress conditions.

This limitation can require larger protection elements paying a penalty in terms of area consumption and RF capacitance. On IC-level a higher power clamp repetition rate may be needed for effective bus resistance Rbus reduction.

If no diode to VDD is allowed (e.g. failsafe or over-voltage tolerant IO, cf. Figure 3 (right)), the high capacitance of a local NMOS clamp must be isolated from the RF pin by a series RF diode. Consequently, the situation is even more critical (2 diodes + NMOS + Rbus) for worst-case stress RFIN-VDD. A local SCR with low anode junction capacitance saves the isolation diode plus offers a much better voltage clamping.

Pi-type protection schemes are commonly used to act as ESD voltage dividers for input protection [10], thus limiting the ESD voltage seen by the sensitive node, in other words, increasing the effective ESD design window for the specific pins. In these schemes input series resistors must separate secondary from primary protection elements. These isolation resistors can significantly compromise speed performance in high-end RF applications due to detrimental gate delay and added RF noise. A scheme called *Active Source Pump (ASP)* [3] also allows for an effective ESD design window expansion, however, in a different voltage divider configuration, which is more compatible with many RF design applications. As a result, a higher ESD design flexibility on IC-level can be achieved for these critical application types.

I.3. Sensitive Drivers

Designing robust output cells, two methods can be applied: either output drivers can be made ESD self-protective or additional ESD protection is added in parallel to the driver. The concept of self-protective drivers is frequently applied in microelectronic ICs. The most straightforward design approach for robust MOS multi-finger transistors uses ballast resistance in each device finger, e.g. by blocking part of the silicide in drain/source junctions or by applying poly-resistor [5] and active area ballasting [16]. These ballasting techniques allow for uniform current flow and stable, linearly scalable ESD performance. In addition to finger ballast implementation, the total gate width must be increased proportional to the desired ESD level. As a result, large drivers significantly increase the IO cells height resulting in considerable area consumption in pad-limited IC's. Other output design methods with fully silicided drivers make use of proprietary transient gate/bulk biasing schemes to enable transistor robustness as for instance presented in [5], [7]. In particular in EPI technologies above described design approaches for MOS robustness are challenging and can fail. More ESD limitations are inherent to advanced SOI technologies with thin Si films (<150nm) as demonstrated in section I.4.

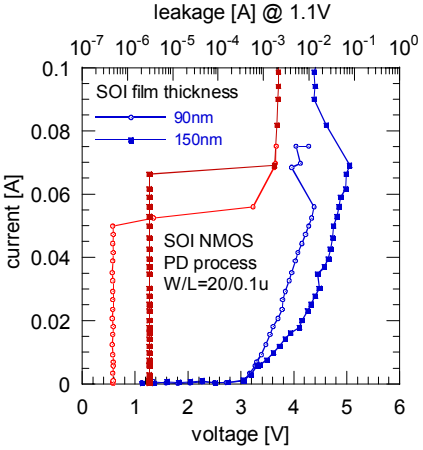

Figure 4 NMOS TLP data in an advanced partially depleted SOI CMOS technology demonstrating a low ESD base performance of It2~2.5mA for a 90nm film thickness.

To address the described challenges above, more area efficient parallel protection devices such as SCRs seem to be the most appealing solution. However, this protection scheme bears a severe potential competitive triggering risk by turning on the sensitive parasitic bipolar inherent to the fully-silicided MOS driver instead of the parallel ESD device. To make

things worse, the quasi-floating driver gate generally reduces the trigger voltage of the parasitic bipolar ultimately to the low holding voltage. Thus, the weak transistor is often preferably triggered and damaged. To cope with the trigger competition, output decoupling resistors between ESD device and driver can be applied but are often not feasible in view of drive performance.

Section IV.3 discusses a safe concept to build ESD robust and relatively small drivers by introducing parallel SCR elements in a self-aligned trigger fashion with no risk of the above described trigger competition.

I.4. SOI Technologies

Due to the thin silicon film and thermal insulating properties of the buried oxide, ESD devices in SOI have a significantly lower performance of 2-3mA/um than devices in a bulk process, cf. Figure 4. This very low base performance makes self-protecting drivers economically not practical anymore.

Moreover, SOI devices reveal a significantly higher on resistance resulting in a poor ESD voltage clamping and therefore a protection incompatibility for ultra-thin GOX (Vmax=4V in Figure 4). The low base performance and poor clamping would imply a severe area penalty on product level.

II. SCR Roadmap

Thyristors or Silicon Controlled Rectifiers (SCR) have been widele used in industry as on-chip ESD protection due to their current shunting and voltage clamping capabilities [8]-**Error! Reference source not found.**.

- High ESD failure current per anode-cathode perimeter (TLP failure current It2~45-70mA/µm) and large HBM performance per area (up to $10V_{HBM}/\mu m^2$ [14])
- Low holding voltage Vh~1-1.5V
- Low dynamic on-resistance Ron~20-50Ω µm

Therefore, these elements represent an excellent solution type to cope with ESD design challenges in advanced technologies as reviewed above.

Applicability of SCRs		> 0.5	0.5	0.35	0.25	0.18	0.13	0.09	0.07
MLSCR	n+ trigger diff. (LOCOS)	OK		not possible					
LVTSCR	integrated GGNMOS trigger	OK				problematic			
GGSCR	NMOS-triggered	expected			OK (VDD: 1.8V-3.3V)				
DTSCR	Diode-Chain Triggered	not required					OK (VDD<1.8V)		
RCSCR	RC-MOS Triggered	not required					OK (VDD<1.8V)		

Table 1 SCR roadmap for selected elements

Table 1 gives a brief SCR history starting with the MLSCR [10] and the LVTSCR [9], which used to provide popular and successful ESD protection concepts down to the quarter-micron regime. However, due to trigger (speed) issues the LVTSCR became problematic in sub-0.18u-CMOS domain demanding for alternative solutions [4].

Different SCR protection elements were designed to protect specific IC circuit nodes in different voltage domains. Those were realized by a modular design concept as will be discussed in the following.

III. Modular SCR Design Technique

To exploit thyristors for ESD protection purposes, two crucial design aspects need to be considered: firstly, the trigger voltage must be engineered according to the specific technology and product application. Secondly, it is of utmost importance to guarantee latch-up immunity during normal circuit operation. This section explains the general design concepts used for different applications to achieve these goals.

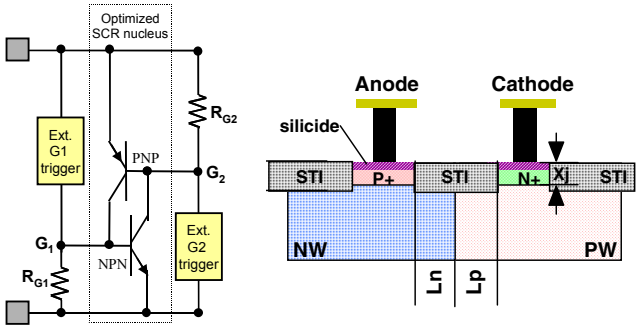

Figure 5 Generic SCR schematic (left) using an optimized SCR core (cross-section right) in conjunction with adapted ESD trigger circuits for specific ESD protection applications according to the technology node.

The so-called "modular design approach" separates the SCR kernel from the SCR trigger element as well as shunt resistors RG1 and RG2 connected to the SCR gates G1 and G2, respectively, as depicted in the generic schematic in Figure 5 (left). This design concept yields the advantage that both device components can be controlled and optimized independently: the SCR for turn-on speed, current capability and voltage clamping; the trigger element for low-voltage turn-on, fast trigger speed, and its application as back-up device coping with fast ESD transients such as CDM (cf. section V). Moreover, as will be discussed in conjunction with SCR latch-up immunity, the discrete gate resistors can be tuned independently to control the SCR trigger/holding current and to prevent false triggering during normal operation.

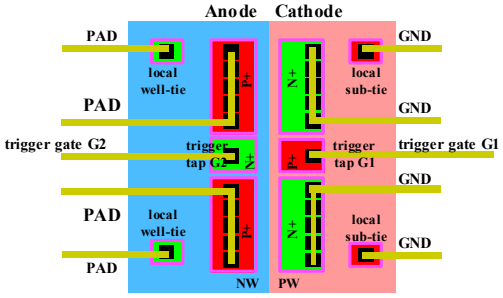

Figure 6 Layout of SCR kernel used with different triggering schemes to be connected to the trigger gates G1 or/and G2.

During ESD stress conditions first the external trigger element is turned on. As a result the Pwell (Nwell) at G1 (G2) is pulled high (low) thus injecting holes (electrons) into the base of the parasitic NPN (PNP). This eventually latches the SCR into a low-resistive and robust operating state. Trigger speed enhancement can be achieved by simultaneous current

injection into both SCR wells [8]. When the device enters the typical ESD high current regime, the SCR wells are swamped with minority carriers leading to a strong conductivity modulation and thus transforming the SCR into a low resistive p+-intrinsic-N+ (PIN) diode.

Figure 5 (right) depicts a cross-section of the active SCR segment. Due to the possibility of a minimum design rule geometry for the anode-cathode spacing Ln+Lp enabled by the modular design approach, smallest possible base lengths for both the PNP and NPN sub-structures can be implemented. Therefore, the intrinsic SCR speed is maximized.

The top view in Figure 6 indicates how the G1 and G2 trigger taps are integrated into the SCR layout: the anode (cathode) is interrupted by N+ (P+) trigger tap(s) to insert the trigger gate G2 (G1). Thru these well taps, the external trigger device can inject current directly into the bipolar base close to the corresponding SCR PNP emitter (NPN emitter).

IV. SCR Trigger Voltage Engineering

This chapter presents different SCR trigger techniques realized by the modular SCR design technique for different areas of application (i.e. supply / IO voltages).

IV.1. NMOS Triggered SCR (e.g. GGSCR)

A GGNMOS triggered SCR (GGSCR) is schematically represented in Figure 7 (left). A GGNMOS transistor is used as an external trigger device between anode and G1 replacing the generic box in Figure 5. To avoid premature failure of the trigger NMOS, drain and source regions are often silicide-blocked for robustness. For speed reasons the gate length is best kept at minimum.

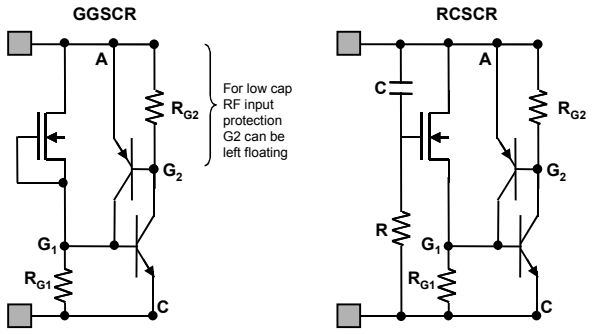

Figure 7 GGSCR schematic (left). Example of Vt1 reduction RC scheme for NMOS or MOS current based triggering RC-SCR (right).

Alternatively, the same trigger NMOS can be connected between PNP base (SCR gate G2) and cathode C as presented in Figure 11 for driver protection.

The pulsed IV-characteristic and the DC leakage current evolution are plotted in Figure 8. All pulsed I-V and DC leakage data presented were measured with a Barth 4002 Transmission Line Pulse (TLP) tester (pulse duration of 100ns). As can be seen in the plot, the GGSCR triggers at the external GGNMOS Vt1=7.8V leading to an instant snapback to the characteristic SCR holding voltage Vh=1.2V. The IV curve continues to the linear high current regime with a typical low on-resistance of Ron=0.7Ω (for W=50um) while the DC leakage current stays constant below 50pA. The destructive pulse current level It2=3.3A is indicated by the sudden increase of the leakage current after the typical roll-off of the IV-characteristic. This increase of the device resistivity is related to excessive self-heating of the contacts in anode and cathode. Therefore, a typical failure mode observed in well-designed SCRs is melted contacts.

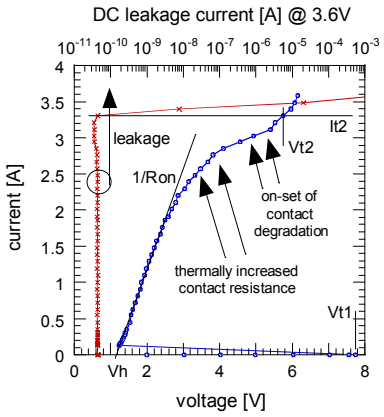

Figure 8 IV-characteristic (Y-axis vs. X1-axis) and leakage evolution (X2-axis vs. Y-axis) of a GGSCR (W=50um).

As discussed in section I.1, the trigger and holding voltage of NMOS devices come close or even exceed the transient breakdown voltage of ultra-thin GOX (tox ~ 2nm) in advanced CMOS technologies. Consequently, the GGNMOS SCR trigger technique is not applicable anymore for thin GOX protection.

Another slightly modified alternative low voltage trigger scheme, cf. Figure 7 (right), appropriate for thin GOX protection can directly be derived from the GGSCR schematic. By increasing the gate width of the trigger NMOS and by applying a transient RC gate-biasing scheme, the SCR can be latched by sufficient MOS current injection into G1 during an ESD event. This is achieved by supplying a transient gate bias to the NMOS during ESD in a similar way BIGFET clamps work. Advantages of this method are a potentially low Vt1~1.5V and a fast triggering mechanism. Moreover, a relatively small RC element is required only to latch the SCR during less than RC<10ns. The next section presents an alternative non-transient trigger technique allowing for ultra-thin GOX protection.

IV.2. Diode Chain Triggered SCR (DTSCR)

The DTSCR uses a diode chain trigger to latch the SCR during ESD stress conditions at sufficient trigger current injection into the gates G1 or G2 of the SCR.

Turn-on can either be accomplished by forward biasing the inherent SCR G1 - Cathode junction, cf. Figure 9 (a), or alternatively the G2 - Anode diode, cf. Figure 9 (b), or both simultaneously. The number of trigger diodes (n) must be chosen sufficiently high such that the chain does neither leak nor trigger the SCR during normal circuit operation. Conversely, the SCR ESD trigger voltage is increasing with n.

A reasonable design trade-off between low leakage during normal operation ("maximize n") and low ESD trigger voltage ("minimize n") can be achieved for low-voltage applications with supply or signal voltage smaller than 1.8V. The trigger voltage can be tuned sufficiently below the transient BVox and V_{max}: Vt1 ~ (n+1) 0.8V < V_{max}, cf. Figure 10. With n=2 trigger diodes e.g. in a G2 scheme we would obtain Vt1 ~ 2.4V. Applying the DTSCR as a power-clamp, the SCR holding voltage must be increased above VDD as one option to achieve latch-up immunity, cf. section VI.1. In this case a trigger diode can be moved from the trigger chain to the SCR anode, cf Figure 9 (c), with the benefit of an increased Vhold while Vt1 remains unchanged.

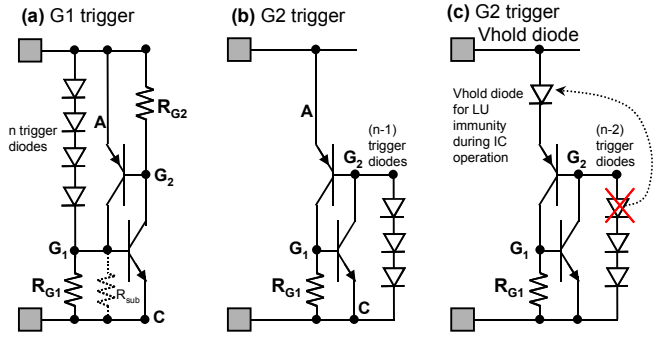

Figure 9 G1-triggered DTSCR (a): forward bias of SCR G1-Cathode junction. In CMOS-SCR an intrinsic connection to the substrate (Rsub) is present. G2-triggered DTSCR (b/c): forward bias of G2-Anode junction. Vh diode for LU immunity replaces trigger diode (c).

Figure 10 plots the TLP-IV characteristics of two DTSCRs in a G1- and G2-triggered configuration, respectively. Both structures have the thinnest NMOS gate oxide (tox=1.7nm) as a monitor in parallel to emulate an RF IC input. Note that the G2-trigger scheme essentially results in the same leakage current as compared to the G1-triggered SCR. However, the G2-triggered SCR reveals a lower trigger voltage Vt1, since one trigger diode less can be used as explained in [18].

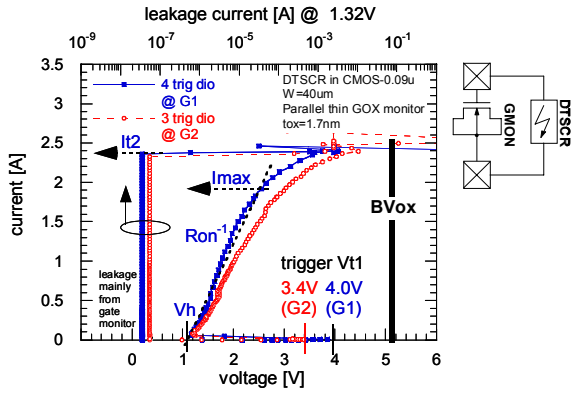

Figure 10 CMOS-0.09u: TLP-IV characteristic of DTSCR including a parallel gate-oxide (tox=1.7nm) monitor to emulate IC input protection. The thin GOX can be successfully protected.

The leakage increase at It2 indicates that the gate-oxide fails within the higher resistive roll-off regime of the SCR IV curve. This means that almost the intrinsic failure current of the stand-alone SCR is reached, which proves that the DTSCR can successfully protect an ultra-thin input gate oxide. Moreover, the margin of Vt1 and the clamping voltage with regard to transient BVox provides ESD design flexibility for protection integration on IC level, cf. introduction.

IV.3. Self-aligned SCR Triggering for Driver Protection

The risk of competitive triggering between driver bipolar parasitics (e.g. the NMOS NPN) and parallel SCR protection, cf. section I.3, is solved by applying a similar trigger concept as for the GGSCR. Again a MOS based trigger element - the drivers itself - is exploited as demonstrated for an NMOS in Figure 11. Instead of connecting the trigger between anode and G1 as in Figure 7, it is inserted between G2 and ground for SCR PNP triggering during ESD. Here, the NMOS NPN having a minimum ESD robustness is allowed to turn on first and conduct the initial ESD stress current I_{dr}. An output resistor between pad = SCR anode and output drain = SCR G1 can now produce the voltage drop of R_{out} I_{dr} ~ 0.8V to sufficiently forward bias the SCR PNP emitter and eventually latch the SCR. As soon as the SCR clamps the voltage the NMOS NPN extinguishes and is protected.

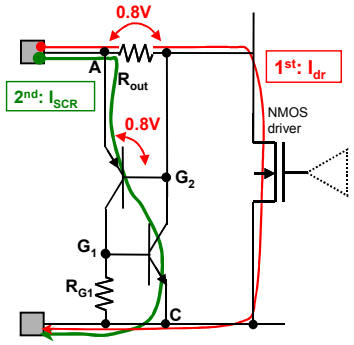

Figure 11 Principle of a self-aligned SCR trigger scheme with NMOS driver in G2 trigger configuration. G2 output resistor Rout builds up the turn-on voltage of roughly Rout·Idr~0.8V.

Figure 12 shows experimental TLP data for the configuration in Figure 11. Initially the voltage snaps back to the characteristic NMOS NPN holding voltage. When the NMOS driver conducts sufficient ESD current reaching the trigger condition R_{out}·I_{dr}~0.8V, the SCR is turned on by the forward biased anode-G2 junction.

The inset illustrates the trigger point for different Rout values. From this figure it can be seen that the SCR trigger current scales inversely proportional to Rout as expected. Larger deviations from the nominal resistance behavior at low Rout are due to thermal resistance increase reducing It1.

The self-aligned trigger concept allows for relatively small Rout < 10 Ohm, which is a critical parameter in many output drive applications. Moreover, the driver itself can be dimensioned relatively small in size due to the fact that it needs to conduct only a small amount of ESD current. Note that the MOS drive current is typically an order of magnitude lower preventing false SCR triggering during normal drive operation by Rout voltage drops.

Another SCR trigger technique, predisposing the element for

turn-on under ESD stress conditions ("ESD-on SCR") can be applied alternatively for driver protection as described in [16].

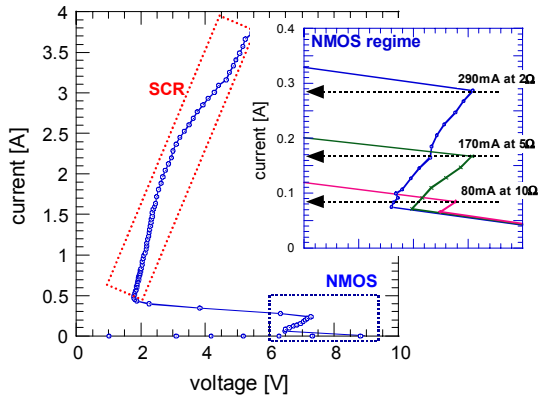

Figure 12 TLP-IV data of self-aligned driver triggered SCR in 0.18-CMOS EPI technology. Inset: Scaling of SCR trigger current is inversely proportional to Rout.

V. SCR Trigger Speed Engineering

Another topic in particular relevant for input protection of ultra-thin gate oxides (tox<2.0nm) covers potential SCR trigger speed issues and dangerous transient trigger voltage overshoots [4], [19]. Speed enhanced implementation concepts can be realized by several (combined) techniques:

- The trigger speed of the SCR core device can be optimized by introducing a minimum anode-cathode spacing. This compact design can easily be achieved by applying modular design approach, cf. section III, instead of integrating the trigger [9], [10].
- The SCR trigger voltage needs to be significantly reduced below the transient oxide breakdown. An example implementation is a diode chain triggered SCR (DTSCR) or RC-NMOS Triggered SCR (RC-SCR) described above.
- A trigger back-up in parallel to the SCR can be introduced for example by increasing the size of the trigger devices as well as the SCR gates G1, G2 [19]. A reinforced diode-chain (including the inherent SCR diodes) for instance provides a fast and low-resistive ESD current path for the first (few) nano-seconds of the ESD stress clipping the initial voltage trigger peak. Here, also the parasitic Darlington supports initial current conduction to provide sufficient time for the slower SCR to respond.
- Simultaneous dual-gate triggering, cf. generic scheme in Figure 5, is also a powerful option to reduce the SCR turn-on time [8]. The trigger schemes discussed in this paper can easily be incorporated in a dual-gate injection configuration to accomplish a fast trigger behavior and high ultra-thin GOX protection levels.
- Isolation of the wells in a triple-well or SOI CMOS technology confines the injected trigger current and allows a more efficient biasing of the bipolar bases, which are part of the SCR substructures [21]. This allows for a faster turn-on.

VI. SCR Latch-up Immunity Engineering

To make SCRs useful ESD protection devices, latch-up by false triggering during normal circuit operation must be avoided. Two different design paths can be followed as discussed in the next two sections.

VI.1. SCR Holding Voltage Increase

The most intuitive technique is to increase the minimum SCR holding voltage above the maximum operating voltage of the IC plus adding a safety margin (e.g. VDD + 10%).

By introducing series diodes to the SCR anode, as demonstrated in the inset of Figure 13, Vh can be increased by an average of approximately 1V per diode rather than the expected diode built-in voltage of 0.7V. This beneficial effect can be attributed to the SCR trigger current in the order of magnitude of ~1-10mA, which drives the Vh diodes into the ohmic high current regime. By the holding diode technique, the device can be made compatible to 1.8V (1d), 2.5 (2d) or 3.3V (2-3d) supply voltages. The SCR series elements do not affect the device performance (It2). Moreover, there is no significant impact on the leakage current when using up to 2 diodes. However, one has to be careful due to the parasitic vertical PNP Darlington into the substrate inherent to the P+/Nwell diode chain. The increase of the on-resistance by series diodes having the same width as the SCR is found to be almost negligible due this parallel Darlington current path.

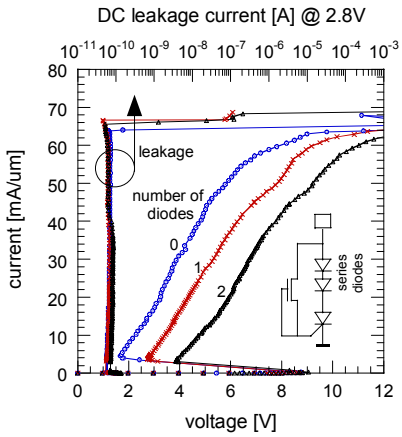

Figure 13 SCR latch control through insertion of series diodes.

VI.2. SCR Holding/Trigger Current Increase

The second technique for LU safe designs is related to an increase of the SCR trigger and holding current, cf. High-Holding Current SCR (HHISCR) [18]. As illustrated in Figure 14, the HHISCR employs an SCR with an increased trigger/holding current. Thus, LU-immune normal operation designs can be ensured while the excellent SCR protection capabilities are preserved to a large extent.

The technique is based on two design approaches: The *external shunt resistors connected to the SCR gates (wells) are significantly reduced*. For the GGSCR in a G1 trigger configuration, cf. Figure 7, the G2-Nwell ties are shorted to the anode by metal, i.e. R_{G2}~0Ohm. The resistor at the SCR trigger gate, G1 in Figure 7, is used to tune the trigger current

by applying a relatively low-resistive poly resistor $R_{G1} \approx 1\text{-}10\Omega$. The resulting higher trigger current $It1 \approx 0.8V/R_{G1}$ (roughly 0.8V needed for well current injection) must be supplied by a reinforced trigger element (e.g. multi-finger GGNMOS in Figure 7). The higher trigger current enhances the LU robustness of the SCR significantly. Another beneficial effect occurs due to the reinforced GGNMOS which supports node protection during ultra-fast CDM serving as a trigger back-up for the SCR, cf. section V.

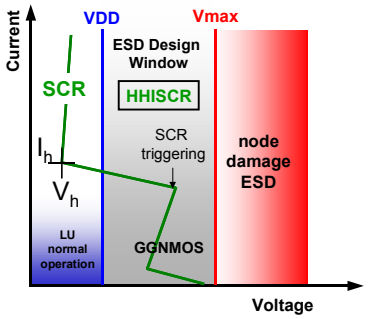

Figure 14 Generic HHISCR IV characteristic within the ESD Design Window defined by the supply voltage VDD and a maximum LU current I_{LU} for normal IC operation. The upper design margin is determined by the critical voltage at circuit failure, e.g. at transient oxide breakdown.

Figure 15 demonstrates a *special SCR layout technique* to reduce the inherent SCR well resistance on top of minimizing the external shunt resistance as described above. Here, intermittent gate diffusion taps between cathode stripes (G1 in Pwell) and anode stripes (G2 in Nwell) are inserted. By interrupting the SCR cathode/anode, the effective well resistance $R_{PW,eff}$ / $R_{NW,eff}$ with regard to the well-ties can be decreased leading to a lowered effective base resistance of the bipolar substructures. This effect increases the SCR holding current and makes the device less prone to LU triggering by substrate currents.

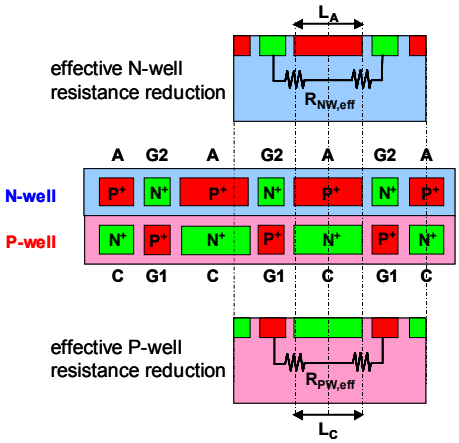

Figure 15 SCR layout technique to reduce the effective well resistances (SCR shunt resistance) and increase the SCR holding current.

The TLP measurement results of the HHI-SCR (W = 40um) are depicted in Figure 16. The device reveals a GGNMOS trigger voltage of $Vt1 \approx 8.0V$. At the triggering point, the voltage snaps back to the GGNMOS specific holding voltage $V_{h1} \approx 5.9V$. This behavior is in stark contrast to the GGSCR characteristics, cf. Figure 8, where the SCR turns on instantly at minimum injection currents without any noticeable intermediate state. Due to the low external shunt resistance R_{G1}, the initial ESD stress is dissipated by the GGNMOS up to a current level of approximately $I_{t1,SCR} = 100mA$ where the SCR turns on. Note that the current Ih' = 180mA does not represent the actual SCR holding current, but results from the 50Ohm-loadline of the TLP tester: (Vt1-Vh) / (It1-Ih') = (7V-2.8V)/(100mA-180mA) = 52.5Ohm. Curve tracer measurements turning the SCR on and off in one cycle, reveal the actual SCR holding current $I_{hold,SCR} \approx 68mA$ [18]. This value is only slightly smaller than It1 and can guarantee LU immunity in many IC applications. HHISCR are also applied in HV technologies [16], [18].

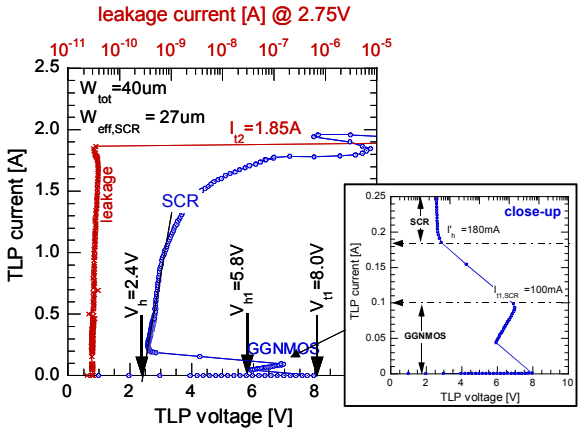

Figure 16 TLP-IV characteristic and corresponding leakage current evolution of an HHI-SCR device (total width including taps W = 50um, 0.10um-CMOS). Close-up of triggering regime (inset): GGNMOS trigger region and transition to SCR operation.

VII. SCR Integration into CMOS SOI

The modular design concepts for trigger and latch-up engineering presented above for CMOS bulk technologies can also be applied for SOI SCRs creating GGSCR, DTSCR etc. However, the actual SOI integration of the SCR core device poses some challenges. Due to the isolation of the 'wells' by STI or PTI (partial trench isolation leaving only a minimum gap ~20nm) any SCR operation in a standard SOI process is disabled. This issue can be solved by introducing a 'STI or PTI block' approach as a non-standard design method to create a four layer NPNP structure in the full silicon film, thus maximizing the effective cross-section for a lateral ESD current path between SCR anode and cathode. Figure 17 depicts a layout top view and cross-section of such a SOI SCR core. To block STI formation, the whole SCR area is defined as active region. Inserting small G2/G1 trigger taps by anode/cathode segmentation is often necessary in advanced SOI CMOS processes replacing trigger implantations behind anode and cathode. Latter are not feasible because source/drain implants or their depletion region reach down to the BOX. Another important design detail must be thoroughly considered: since the active region covers the whole SCR,

silicide would short out all junctions. Therefore, silicide-block (SB) must be thoroughly applied for instance between anode and cathode or around the trigger taps.

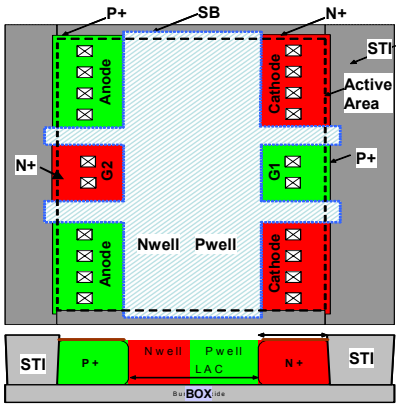

Figure 17 Layout top view and cross section of the SCR core in SOI

Figure 18 represents the TLP-IV plot of a double sided DTSCR in a 65nm SOI technology with a film thickness of tsoi=90nm. The It2 performance of about 10.5mA/um is about 4 times larger than the corresponding NMOS NPN performance of 2.5mA/um in this technology, cf. Figure 16. Besides reaching the physical limit for current performance achievable in the thin SOI film, the plot demonstrates the ESD protection capability of thin GOX (tox=1.3nm) in parallel to the SCR also for fast TLP rise times (TR=200ps).

Advantageous in SOI is the fact that no precautions need to be taken to prevent substrate current triggered latch-up.

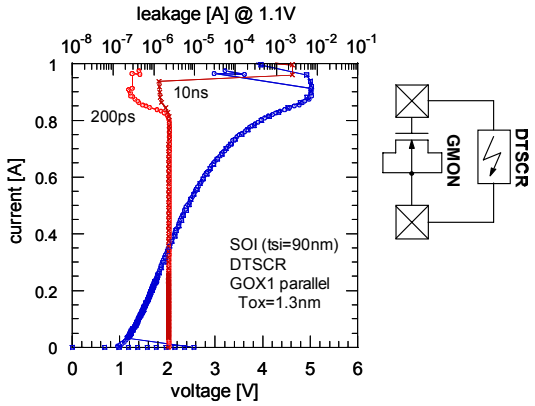

Figure 18. TLP-IV characteristic of DTSCR in 65nm SOI CMOS. The ESD protection capability with parallel gate monitor is demonstrated for slow and fast TLP rise times.

VIII. Conclusions

The paper discusses the application of advanced SCR circuits for a complete ESD protection design methodology in IC products covering all supply voltage domains and full IO protection. The modular circuit design technique separates SCR core, trigger, and latch-up engineering thus independently allowing optimal design parameters for fast, efficient and reliable SCR operation. Different SCR devices realized by this concept are presented covering the protection of core transistors including ultra-thin GOX inputs as well as area efficient driver design in a self-aligned SCR trigger approach. Two techniques to achieve normal operation latch-up immunity of the SCR are discussed. The first approach is based on holding voltage increase by adding series elements. The second concept relies on trigger/holding current increase. SCR integration into SOI technologies is enabled by blocking STI formation between the ESD current conduction paths while using the same modular circuit technique as in bulk CMOS for SCR engineering. SCR also offer low capacitance ESD protection solutions for high-speed interfaces.

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  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
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Notes

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