Conference paper

Current detection trigger scheme for SCR based ESD protection of Output drivers in CMOS technologies avoiding competitive triggering

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Current detection trigger scheme for SCR based ESD protection of Output drivers in CMOS technologies avoiding competitive triggering

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Abstract - A local protection scheme for output drivers is presented, solving the competitive triggering issue using only a very small series (~10 Ohm) resistance. This novel solution uses an SCR that is triggered by current flowing through the driver in ESD mode.

I. Introduction

When designing an ESD protection for output pins, one of two methods can be applied: (A) either the output drivers are made self-protective to allow ESD current through the drivers or (B) an isolation resistor is added to increase the pad potential and redirect the main ESD current either through the parallel local clamp or through the power clamp.

A. Self-protective MOS drivers

For self-protective MOS drivers the layout needs to be altered to obtain a driver that is robust enough to conduct all the ESD current. Therefore, the total gate width is increased, proportional to the desired ESD level. Further, ballasting is typically added at the drain side.

The added resistance serves two purposes:

- Micro-ballasting: due to the larger resistance, the current distribution within one finger is improved.
- Macro-ballasting: the additional voltage drop over the resistor will make sure all fingers trigger.

For micro-ballasting the requirement for the resistance value is less strict than for macro-ballasting. In the latter case the resistance value should be at least

$$R_{bal} + R_{on} > (Vt1 - Vh) / It2 \qquad \text{(EQ-1)}$$

where It2 is maximum ESD current conducted by one finger, Ron is the intrinsic resistance of one finger in parasitic bipolar mode, and Rbal is the added

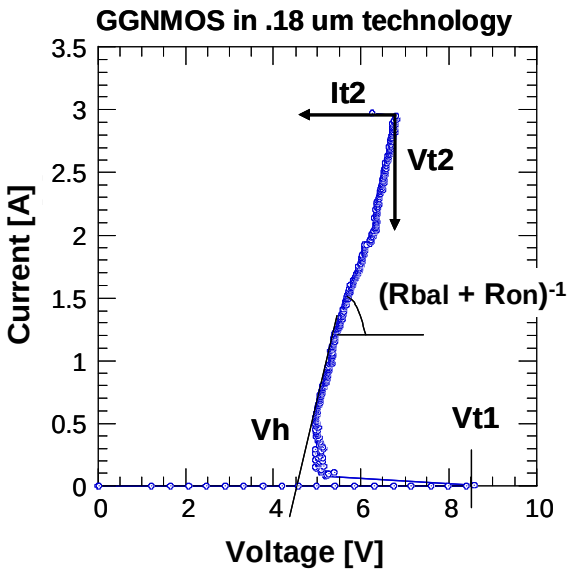

Figure 1: GGNMOS device in .18um technology, showing the parameters of EQ-1.

ballasting resistance for one finger. (Figure 1).At the failing point of one finger, the voltage over the device should be higher than the triggering voltage Vt1 of the other fingers. This is necessary to ensure all fingers are turned on during ESD. Ballast can be added through the use of silicide blocked junctions,

well ballast or back-end ballasting (BEB) techniques [1-4].

The major drawback of this self-protective approach is the high area cost: each driver has to be strong enough to take all the ESD stress current; assuming a 200V MM (~ 3A TLP) specification and a typical NMOS It2 = 6mA/um, the driver has to be at least 500 um wide. Perpendicular to the gate width, the pitch is also increased by introducing ballasting.

Different techniques exist to enhance uniform triggering through all fingers of MOS drivers by bulk pump schemes or increased bulk coupling [5-9]. Moreover, in many technologies self protective drivers are not feasible due to multi finger triggering issues. This is in general the case for technologies with a deep snapback, where EQ-1 can not be met. Also, a low correlation factor between HBM and TLP data for self-protective drivers is often seen. (e.g. Table 1).

Because of these difficulties, making the drivers self-protective is often not an attractive solution.

B. Isolation resistor

In the other approach, an isolation resistor is added to trigger an ESD protection parallel to the driver. This can either be an added local clamp (Figure 2) or a powerclamp. In both cases the main issue to solve is competitive triggering between the two current paths: NMOS driver versus the ESD clamp

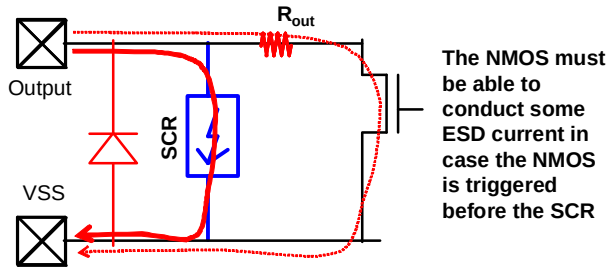

Figure 2: Local SCR clamp in parallel to the output driver: Carefull design of the output resistance is required to avoid competitive triggering issues. The resistance limits the current through the driver and builds up voltage required to trigger the SCR. The SCR conducts the main ESD current.

A first possibility to solve this issue is to create an ESD clamp which triggers at a sufficiently low voltage, i.e. lower than the holding voltage of the NMOS driver, yet still high enough not to endanger normal operation. In many cases this is very difficult, if not impossible. Two other solutions exist for the competitive triggering issue:

- Limit the ESD current through the driver by adding a large series resistance (>50 Ohm) in the output pad between the protection structure and the driver.
- Increase the Vt1 trigger voltage of the driver by keep-off circuits or gate/bulk bias-schemes [10-11]

Both solutions have a big implication on normal operation.

To avoid the drawbacks of these methods, a novel SCR based solution is presented, called a Resistor Trigger Silicon Controlled Rectifier (RTSCR). The next paragraph explains the mechanism of the device. The third paragraph shows measurement results obtained in 0.6um, 0.3um, 0.18um (EPI) and 0.13um (EPI) CMOS technologies.

II. RTSCR principle

The basic idea behind the RTSCR is to detect ESD by monitoring the current flow into the driver. When this current exceeds a predefined level, the chip is diagnosed to suffer from ESD stress. This condition automatically triggers the protection device. Three elements are required:

- A current monitor, that discriminates between ESD current and normal operation current.
- A protection device which shunts the main ESD current, and that reacts to the current monitor.
- A normal operation circuit element which conducts the first, limited ESD current.

For output protection this solution is highly preferable. In the RTSCR solution the current monitor is implemented as a resistor. The resistor is placed in parallel with the Anode - G2 junction of an SCR. The voltage across this resistor exceeds a critical level in case of ESD, while staying at low levels during normal operation.

The schematic is shown in Figure 3. Three devices can be distinguished:

- The NMOS driver. The width of this device is determined by normal operation conditions, and the gate width is therefore typically not altered by the ESD protection strategy. This NMOS driver conducts the ESD current for the first nanosecond(s) and needs appropriate ballasting to prevent failure due to this current. If the driver cannot be made robust to survive any ESD current, the RTSCR schematic cannot be used. For these technologies, other solutions are needed [12].

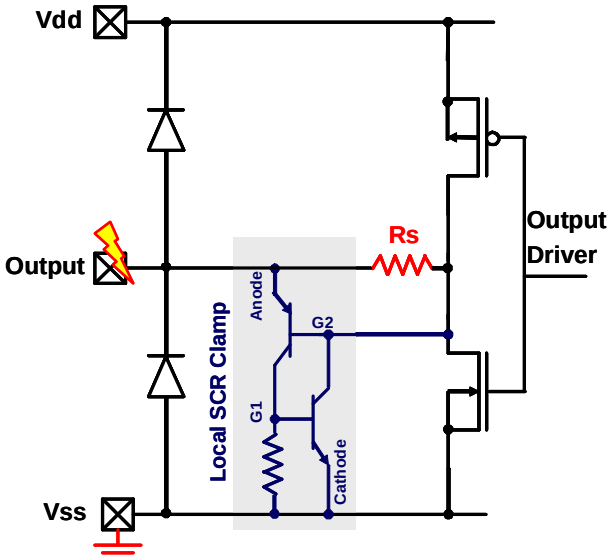

Figure 3: Schematic of the RTSCR protection device for an NMOS output driver. The SCR is triggered in a low ohmic conduction state at a fixed current level, through the NMOS. The current level is determined by the Rs resistance.

- The SCR. This device stays off during normal operation. During ESD it conducts the main current. Therefore its layout can be freely determined by the ESD engineer.
- The resistor Rs. The resistance will act as the ESD detection circuit. Its value is determined by both normal operation and ESD considerations.

Key to the design of the RTSCR is the value of the Rs resistor. Apart from the obvious condition that Rs cannot compromise normal operation driver performance (and thus defines an absolute maximum resistance value), there are two conditions to be met:

- During normal operation the amount of current in the output pad is determined by the MOS operation of the driver. This current is typically around 0.5 mA per um NMOS gate width. The maximum value of the Rs resistor is determined by this current such that the voltage drop for maximum drive current ($I_{driver,\ max}$) is limited to about 300 mV, keeping the parallel SCR local clamp off.
- In ESD conditions, however the same driver can take much more current in parasitic bipolar mode ($I_{t2,driver}$ > 5mA/um). Therefore, the voltage drop over the series resistor Rs is much larger. The minimum value of the resistance Rs can then be calculated such that >800 mV bias is generated over the anode-G2 diode junction of the SCR, turning on the local protection element.

The range of possible Rs values is determined by the ESD strength of the driver compared to its normal operation current conduction capability. In normal operation, the current through the driver is determined by its MOS drive operation, i.e. ~ 0.5mA/um. In ESD mode, typical values of 5-10 mA/um are achieved. The typical factor of 10 leaves enough design margin to calculate an optimal value of Rs. In conclusion, if no other requirements for normal driver operation are posed, the value for the series resitance can be determined from:

$$\frac{0.3V}{I_{drive,\max}} \geq R_s \geq \frac{0.8V}{I_{t2,driver}} \qquad \text{(EQ 2)}$$

Alternatively, the current level specified by the latch up test can be used instead of $I_{drive,\ max}$.

As stated before, in some technologies multi finger triggering can not be achieved. In worst case conditions, only one finger triggers. In this case, $I_{t2,driver} = I_{t2,\ driver\ finger}$. in EQ2. Sufficiently wide finger widths are required for a feasible design window for Rs. Due to current uniformity issues, finger width should be limited < 100 um in most technologies.

Please note that for high temperature applications, the voltage needed over the anode-G2 junctions to trigger the SCR decreases, while the resistance value of Rs increases. Therefore the trigger current will decrease. This can be solved by adding another small diode, which doubles the trigger current. (Figure 4).

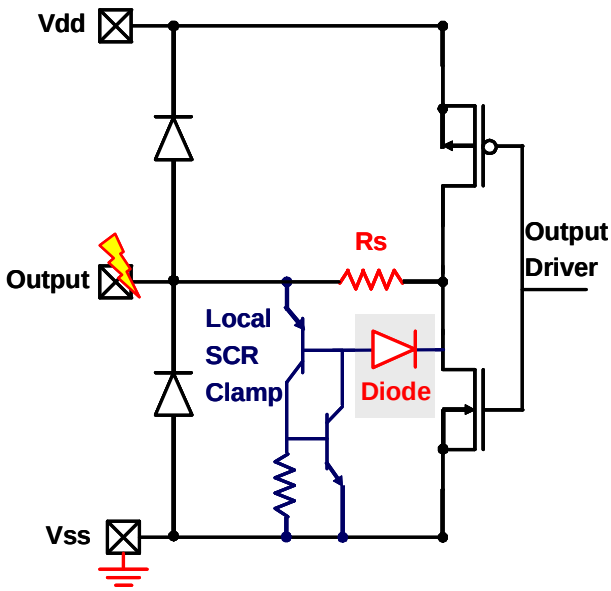

Figure 4: Diode added to increase trigger current.

III. Measurement results

The measurements are performed using a Barth Electronics Inc. TLP system with a fixed pulse width of 100ns. Devices from four CMOS technologies were measured:

- 0.6um 5V
- 0.3um 3.3-13.5V;
- 0.18um EPI TSMC 3.3V
- 0.13um EPI TSMC 3.3V

Figure 5 shows the basic principle for an NMOS of W= 4x34um in a 0.6um technology. It2 of this driver is ~5mA/um. At low current levels, the NMOS is conducting in the parasitic bipolar mode. For ESD current below 250mA the voltage drop over the isolation resistance (value ~2 Ohm) is too low to forward bias the Anode-G2 junction. The SCR is triggered for current levels above 250mA. The inset of the figure depicts a close-up of the triggering of the NMOS and SCR.

In Figure 6 an SCR (70um wide) is triggered at different current levels for three values of the resistance. The NMOS driver (180um wide) has a gate length of 6um, about 3 times the minimum design rule value for a transistor with this particular implant. The It2 of the driver was only ~500mA. The

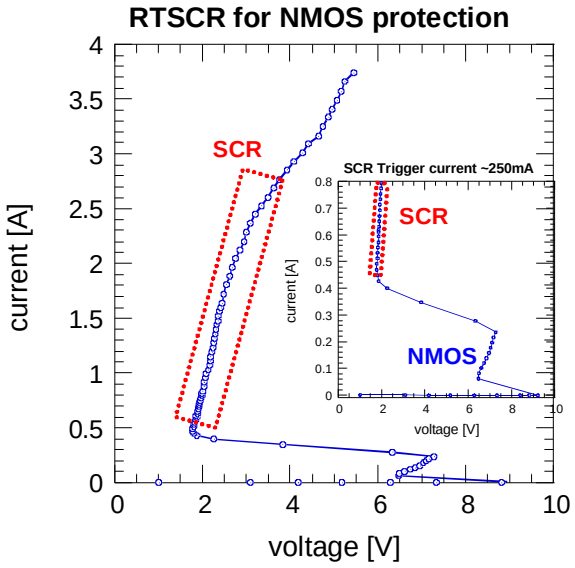

Figure 5: RTSCR measurement in a 0.6um 5V CMOS technology. Resistance value Rs=2 Ohm. The SCR (width=30um) conducts the main ESD current. ESD currents below 250mA are handled by the NMOS driver.

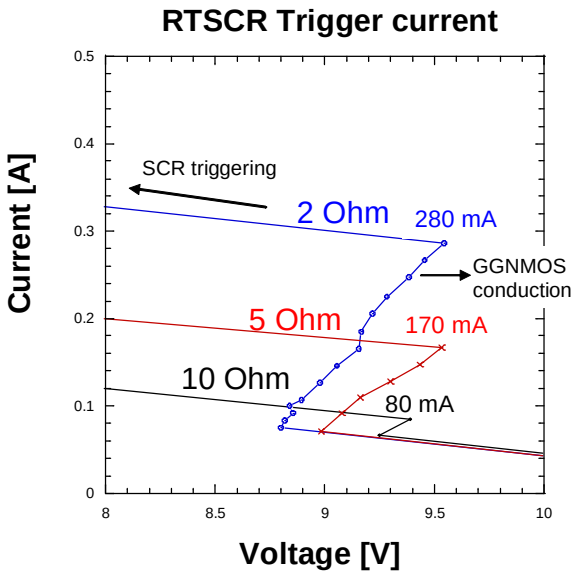

Figure 6: RTSCR measurement close up for 3 values of the resistance in 0.6um technology. The SCR trigger current is shown to increase with decreasing resistance values.

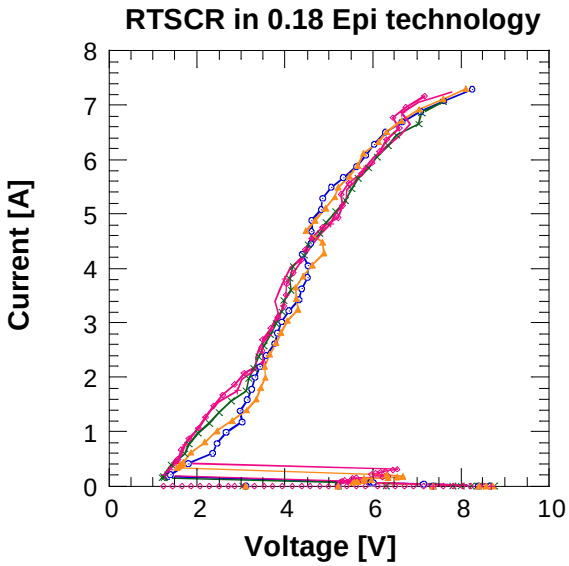

Figure 7: RTSCR measurement results in a 0.18um EPI TSMC technology for different values of R and different NMOS drivers (width and DCGS variations). The resistance and driver influence the SCR trigger behaviour, as was shown in Figure 6, but the high current regime is the same for all implementations (W_{SCR} = 2 x 50)

maximum drive current during normal operation is defined as 20 uA. Three different variations of Rs are shown. Even for the largest value, 10 Ohm, there is no danger of triggering the SCR in normal operation, unless the maximum driver current exceeds ~70mA.A high It2 (~100mA/um) for all implementations was found (not shown in the figure). As expected, this SCR failure current is independent of the value Rs. The Vt1 of the NMOS does not change with the value of Rs either, since at the time of triggering, no current is flowing. The Vt1 of the SCR can easily be calculated as Vh, NMOS + 1V, and is independent of Rs.In Figure 6, one can clearly see that the trigger current of the SCR decreases with increasing Rs. Analytically, Rs*It1~800 mV. For the Rs = 2 Ohm case, this calculation deviates slightly (280mA*2Ohm ~ 560 mV), because of the lower accuracy for the low ohmic resistors. These measurements clearly show that the Rs resistance can be used to tune the current level at which triggering of the protection device occurs. Figure 7 summarizes TLP results of the same concept applied in 0.18um TSMC technology on EPI. Different values for the resistance Rs and different NMOS driver implementations are shown together. The It2 current level for the SCR is always above 7A and HBM above 8kV. All the different driver implementations are protected by the SCR protection. The different driver implementations included 1.2V and 3.3V drivers and width variations.

In Figure 8 the IV curves of two RTSCRs (2x40um wide) are shown in a 0.13um EPI technology using 2 values for Rs. There is one major difference in implementation as compared to the RTSCR in the 0.18um technology depicted in Figure 7: for the 0.13um structures, the gate of the NMOS was coupled high. This can be seen in the measurements from the fact that there is no snapback in the MOS conduction regime. (Figure 9) The voltage at the gate of the driver does not affect the triggering principle of the RTSCR.

The higher perfomance of the SCR in 0.18 EPI (~70mA/um) as compared to 0.13 EPI (~50mA/um) is attributed to the different contact sizes in both technologies. The same difference in performance was also observed for other SCR implementations (GGSCRs, DTSCRs, …) not shown in these figures. In Figure 10, a measurement is plotted for an RTSCR protecting a PMOS driver in a 0.3 um HV technology. The protection schematic is depicted in Figure 11. The It2 of the RTSCR (not shown here) is higher than 80 mA/um. The voltage over G2-Anode at the SCR trigger point is roughly 300mA*2Ohm ~ 0.6V, which complies with the above explained trigger mechanism.

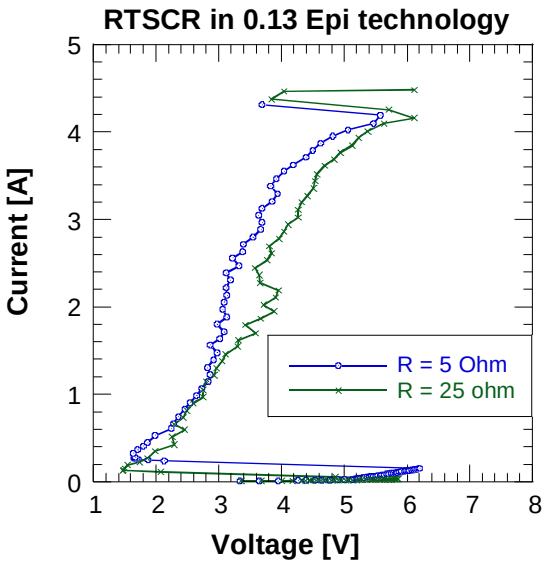

Figure 8: RTSCR in 0.13um technology. The gate of the driver is coupled high, such that no snapback is seen in the NMOS conduction regime.(see Figure 9)

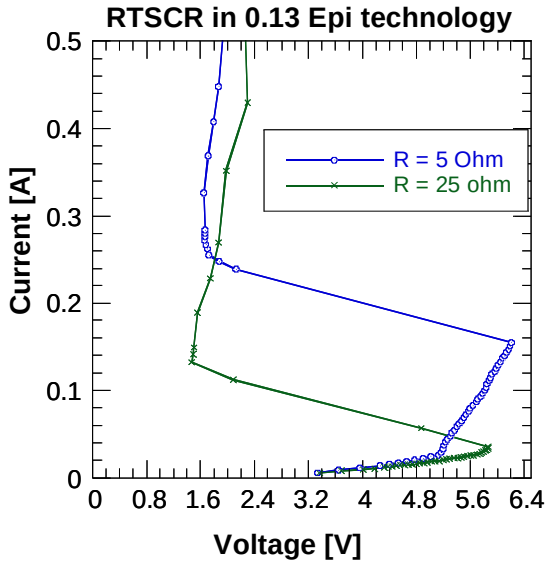

Figure 9: Zoom of triggering behaviour of RTSCR in 0.13um technology (Figure 8)

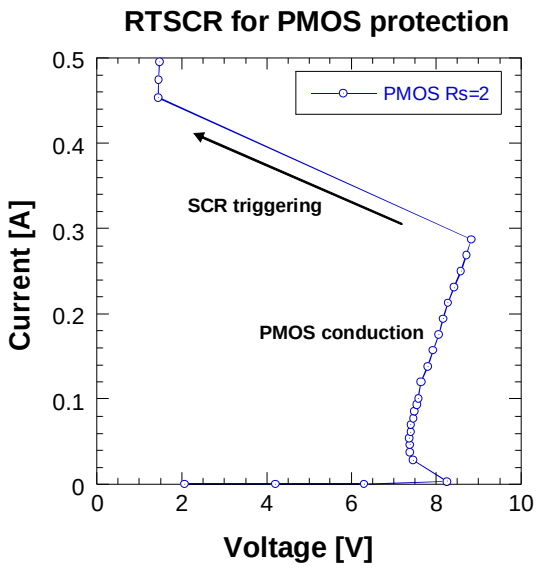

Figure 10: RTSCR protection for a PMOS driver in a 0.3um HV technology. A trigger current of 300 mA for an Rs of 2 Ohm is shown.

One of the key advantages of the RTSCR is that it solves much of the HBM-TLP correlation issues typically seen for self protective MOS devices. In the 0.6um and 0.18um technologies, low correlation between the HBM failure values and the TLP failure levels are found for ggNMOS devices. Going into the different possible reasons for this lack of correlation [13-17] would be beyond the scope of this paper, but it should be noted that the RTSCR devices in these technologies did not exhibit the same weakness to HBM stresses, as can be seen from Table 1. Although the ggNMOS devices fail at HBM levels below 1.5kV for different ballasting techniques, all RTSCRs can protect the drivers up to high HBM levels (> 8 kV, the maximum level of the used tester).

Conclusions

In this paper a novel protection concept is presented, to improve ESD protection for output drivers. High protection levels are achieved, with only a minimal impact on normal operation. Measurements from four CMOS technologies are used to show the analytical alterable trigger current, and the high It2 level. The technique is applicable both for NMOS and PMOS output drivers. The main advantage of this concept is a much smaller Si area (down to 30%) required for implementing ESD protection of output drivers, depending on the drive strength for normal operation and the maximum resistance value allowed.

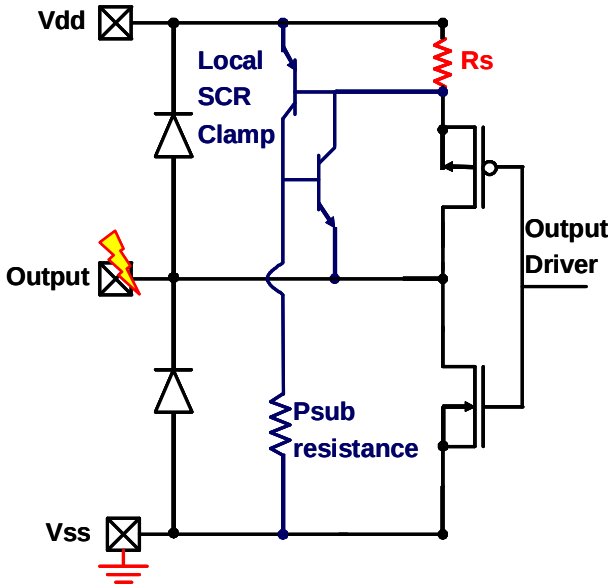

Figure 11: RTSCR principle used for protection of a PMOS driver for ESD stress from Vdd (+) to output (GND).

Technology	ggNMOS size [um]	GGNMOS TLP [A]	GGNMOS HBM [kV]	SCR size [um]	RTSCR TLP [A]	RTSCR HBM [kV]
0.6 um CMOS	8x50	3.5	1.3	70	7.2	> 8
0.18 um EPI	20x20	2.9	0.7-1.2	2 x 40	6.0	> 8

Table 1: HBM and TLP data for ggNMOS devices (left side of the table) in 0.6 and 0.18um technologies. A low correlation factor between HBM and TLP is found. The same MOS devices can be protected using the RTSCR technique to values above 8kV (right side).

Acknowledgement

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Notes

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