Conference paper

SCR based ESD protection in nanometer SOI technologies

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I. Introduction

As the CMOS technology roadmap reaches the nanometer nodes, efficient ESD protection design is becoming increasingly difficult. The protection of the thin gate oxide in particular is faced with a number of challenges. First of all, with the steady decrease in breakdown voltage of the gate oxide (BV) (Figure 1), constraints for the ESD protection element are becoming more severe.

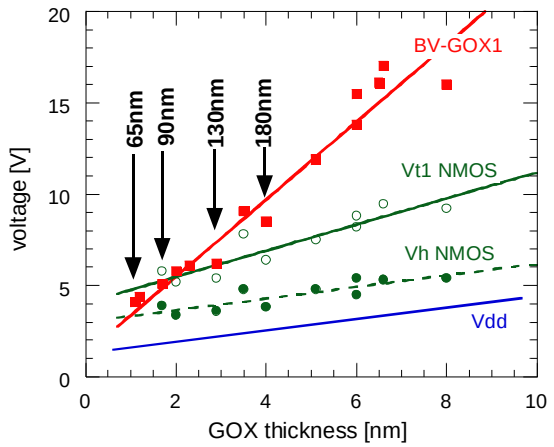

Figure 1. Evolution of the BV of the GOX1 in comparison to the trigger voltage (Vt1) and the holding voltage (Vh) of an NMOS in Bulk CMOS technologies down to the 65nm node.

Secondly, Figure 1 also shows the trend for the holding voltage (Vh) of the gate grounded NMOS, long considered the workhorse for efficient protection. It is clear that this voltage Vh is not decreasing accordingly. Since Vh constitutes the lowest possible voltage in the ESD on state (not considering the voltage drop due to the on resistance), the margin for protection design is vanishing for increasingly advanced technologies. Therefore the application of the NMOS in nanometer CMOS is very limited [1]. Moreover, with the introduction of advanced technologies like SOI (Silicon On Insulator), other challenges have arisen. Due to the thin silicon film and insulating properties of the buried oxide, ESD devices in SOI are expected to have a significantly lower performance than devices in a Bulk process [2-4]. Figure 2 depicts measured TLP failure currents of basic devices in various technology nodes for both bulk and SOI.

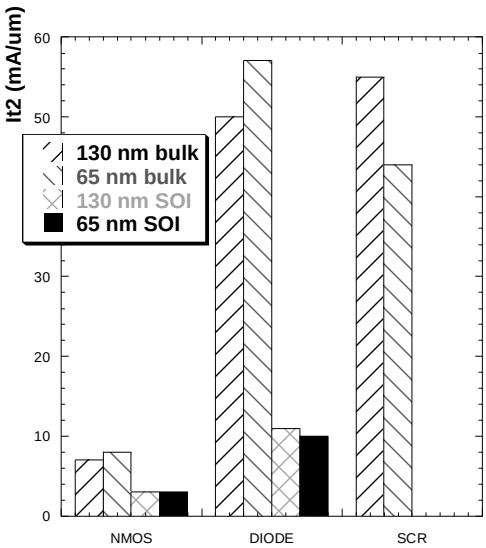

Figure 2. TLP It2 study for diode (STI blocked), NMOS and SCR devices in various CMOS technologies (Bulk and SOI). A typical factor of about 4 is found between bulk and SOI and between MOS (bipolar mode) and diodes within the same technology node.

Ron [Ωμm]	Diode	MOS	SCR
130 nm BULK	90	400	60
90 nm BULK	51	466	60
65 nm BULK	40	120	26
130 nm SOI	100	1056	
65 nm SOI	150	565	

Table 1. Ron comparison for diode, NMOS and SCR in various CMOS technologies (values are in Ωμm).

From these measurements, bulk devices have about 4 times higher ESD performance as compared to SOI.

Table 1 shows that SOI devices have a significantly higher on resistance due to the thin Si-film. Note the increased sheet resistance of SOI diodes due the decreased film thickness in 65nm SOI. This data implies a severe penalty on the consumed silicon area, rendering a snapback MOS based solution less attractive and strengthening the need to look for a novel approach.

In this paper we present an SCR based solution for ESD protection in SOI. Section II explains motivation to look for an SCR solution in these technologies. Section III addresses the challenges in making a functional SOI SCR. The actual design of the proposed device is presented in section IV. Finally, section V presents experimental data in different SOI technologies. This data is derived from three different SOI technologies:

- 130nm Partially Depleted (PD) SOI (2nm gate oxide)
- 65nm Partially Depleted (PD) SOI (1.3nm gate oxide)
- 65nm Body Slightly Tied (BST) SOI (1.3nm gate oxide)

In Partially Depleted SOI the STI goes all the way down to Buried Oxide, but the bulk of the MOS devices is not completely depleted. In Body Slightly Tied SOI the STI does not reach the Buried Oxide, leaving a high resistive connection underneath the STI.

II. Motivation

Figure 2 shows that diodes (bulk and SOI) have a consistently 4-5 times higher performance compared to MOS devices. Further, SCR devices and diodes exhibit the same performance for the different bulk technology nodes. Should this still hold true for SOI, SCR devices would be able to reach an It2 4 times larger than that of an NMOS. Furthermore, an SCR usually has a holding voltage of around 1.2V. This low holding voltage would return much needed margin for efficient ESD design. Moreover, in SOI fewer precautions need to be taken to prevent false triggering due to stray substrate currents reaching the SCR device because the isolation oxide (STI/BOX) prevents any carriers from reaching the active region of the device. Even if the STI does not touch the BOX, the current path underneath the STI is usually so resistive that there is no need for additional guard bands. Finally, the possibility of isolating both the NWell and the PWell allows better control of the well resistances RG1 and RG2 and well potentials (Figure 3). This offers straightforward circuit techniques to ensure multifinger operation. The actual implementation of an SCR device in SOI however poses also a number of challenges which are summarized in the next section.

III. Challenges

An SCR (Figure 3) basically comprises an integrated PNP and NPN transistor in a latch configuration. In Bulk, the PPLUS anode, the NWell and the PWell form the vertical PNP transistor and the NPLUS cathode, the PWell and the NWell form the lateral NPN. RG1 and RG2 are the well resistances. In SOI, due to the isolation of the wells and the buried oxide there is no longer a vertical PNP transistor available, seemingly preventing SCR action. Another consequence of these isolated wells is the lack of a NWell/PWell junction because of the separation by BOX and STI. One way to mitigate this problem is placing a gate across this junction between the anode and the cathode of the SCR. This however creates severe leakage concerns.

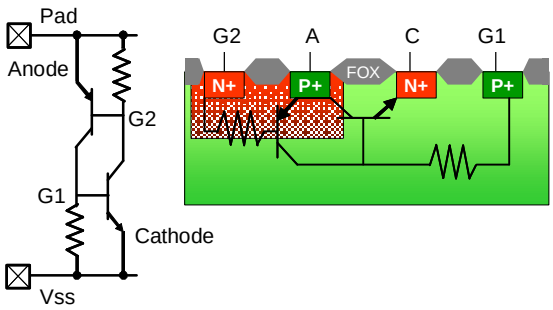

Figure 3. Schematic and typical cross-section of an SCR in a bulk technology showing the vertical PNP and lateral NPN.

By placing a gate over the junction, there will always be a MOS channel present between pad and ground. Either through the open PMOS formed by the part of the gate over the NWell if the gate is tied low or through the open NMOS formed by the part of the gate over the PWell if the gate is tied high as can be

seen in Figure 4. Clearly another way to prevent the formation of STI between the wells is needed. A third challenge constitutes the triggering of the device. Relying on well to well breakdown to trigger the SCR is not possible, since the voltage built up over the device would be too high to effectively protect the thin gate oxide.

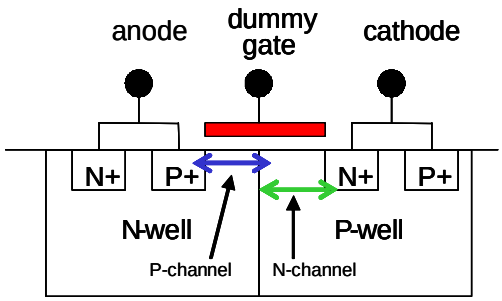

Figure 4. Formation of MOS channels in a poly spaced SCR. Placing a gate over the well-well junction creates parasitic MOS devices of which at least one is always in conduction. The PMOS is on if the gate is tied low, the NMOS is on if the gate is tied high.

Triggering implantations in the junction are also not a viable solution, because the implants typically reach down to the BOX and this blocks the SCR action. This paper introduces a layout approach which makes SCR action in SOI possible. In Section V experimental data will be provided to support this.

IV. Actual design and layout

The actual SCR layout is made up of three crucial steps:

1. create the Nwell/Pwell junction by blocking the STI
2. introduce trigger means by segmentation of the anode and cathode.
3. avoid a short circuit by applying silicide blocking

Figure 5 and 6 show the top view and cross-section of this device with two Anode/Cathode segments.

To block the formation of STI, the whole SCR area is defined as active region. Next, the segmentation approach is necessary because, as already mentioned in the previous section, the implants in some SOI processes go all the way down to the BOX. Even if they don't reach the BOX completely, the connection underneath them is very resistive. This implies that the standard SCR layout for Bulk CMOS with trigger implantations behind the anode and cathode respectively is not applicable in SOI. Placing small G2/G1 trigger taps interrupting respectively the anode and cathode, provides the necessary current path to the base of the PNP/NPN. This way the vertical PNP is replaced with a lateral device. One important issue remains however. Since the active region covers the whole SCR, silicide will cover all the junctions, shorting them. The overlay of a correct pattern of silicide block prevents this (Figure 5). To trigger this device, an external trigger element feeds current to the G1 and the G2 taps.

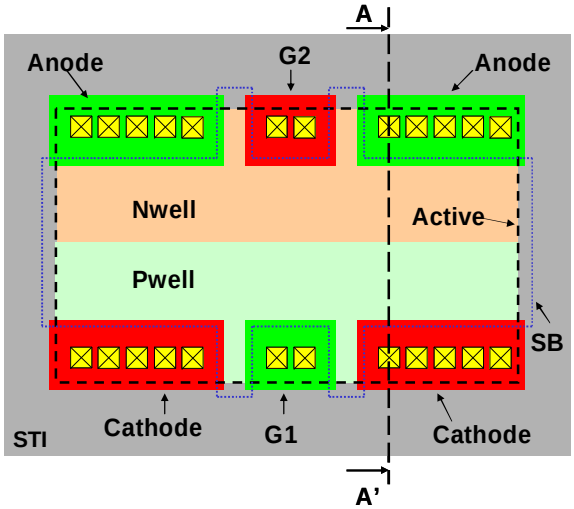

Figure 5. Top view (layout) of the SOI SCR implementation.

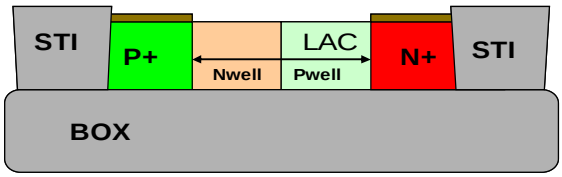

Figure 6. Cross-section A-A' of the SOI SCR implementation (LAC represents the spacing between the anode and the cathode regions).

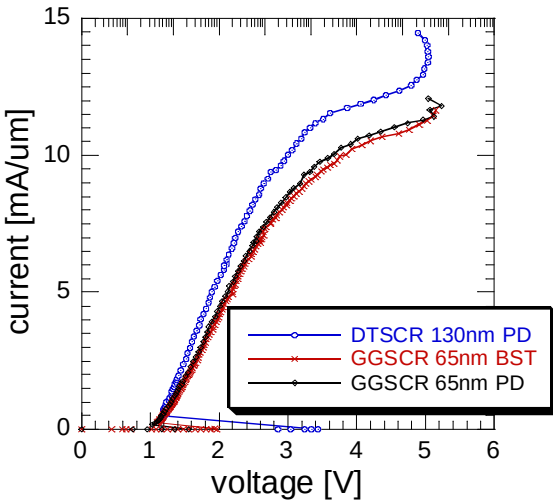

Figure 7. SCR conduction in two 65 nm SOI processes. and in a 130 nm The current is plotted relative to the device width.

V. Experimental data

This section presents experimental results of this device in 65nm and 130nm SOI and compare them to the corresponding bulk devices. The focus is on the DTSCR or Diode Triggered SCR (which uses diodes as external trigger devices) [1] and the GGSCR [5] (which relies on a GGNMOS as external trigger element. The SCR body is the same for both implementations.

Figure 7 presents normalized TLP data from 3 different technologies with a pulse width of 100ns and a rise time of 10ns: 130nm Partially Depleted (PD), 65nm Partially Depleted (PD), and 65nm Body slightly tied (BST). Both SCRs in the 65nm process have a total width of 80um and have a normalized It2=10.5 mA/um. In the 130nm process, the total SCR width is 100um, normalized It2=14mA/um. Table 2 presents a comparison of typical It2 values for different devices both in bulk as in SOI technologies. This table illustrates the fact that SCRs have a similar performance as diodes. The It2 is ~4 times higher as compared to MOS devices. It also shows that SCR devices in SOI are ~4 times weaker than in Bulk.

Technology		Normalized It2[mA/um]		
		MOS	Diode	SCR
Bulk	130nm	7	50	55
	65nm	8	57	44
SOI	130nm PD	3	13.5	14
	65nm PD	3	10.5	10.5
	65nm BST	3	10.5	10.5

Table 2. Normalized It2 performance comparison for bulk and SOI devices

V.A Layout variations

To study their influence, a number of SCR layout parameters were varied: width, number of segments, RG1/RG2 values, number of fingers, anode to cathode spacing and the number of contact rows on anode and cathode. This section will present the results of this study.

Width variations – Figure 8 presents TLP data for DTSCR devices with different SCR widths in a 65nm BST technology. If the It2 failure current is plotted against the SCR width (Figure 9), perfect linear performance scaling. This allows a straightforward way to adjust to any ESD specification.

Number of fingers variations – Figure 10 shows that there are no multi finger triggering issues, all fingers turn on and contribute to the high current capability. The two largest devices are measured on wafer while the smallest device which was measured on package. Due to calibration difficulties on wafer for very low resistive devices such as large SCR devices, the wafer measurements show a higher irregularity and on resistance, especially for low current levels. However, the holding voltage is the same for all the presented data.

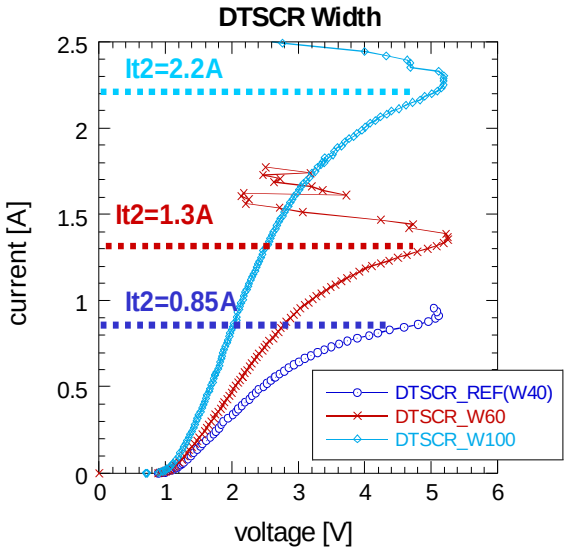

Figure 8. TLP data for DTSCR devices with different SCR widths from a 65nm BST technology.

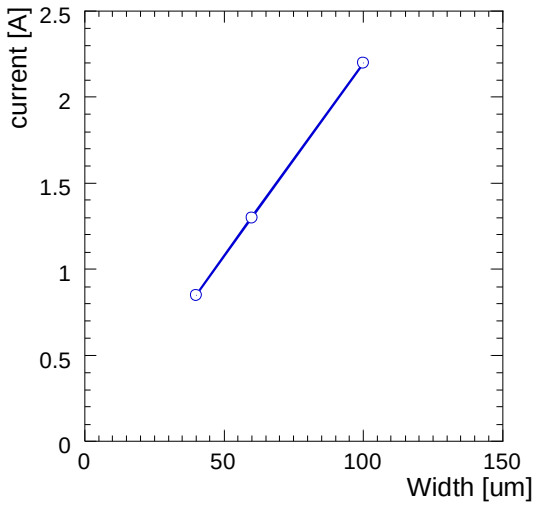

Figure 9. It2 failure current plotted against the SCR width showing perfect scaling.

Number of segments variations - Figure 11 shows the trigger current It1 of the SCR for different number of segments. Adding more segments reduces the well resistance, and therefore increases the trigger current It1 [6]. Also note the low It1 value for all variations. In a CMOS bulk process this value is typically in the order of a few mA. Therefore in SOI, care must be taken to not trigger the SCR through leakage.

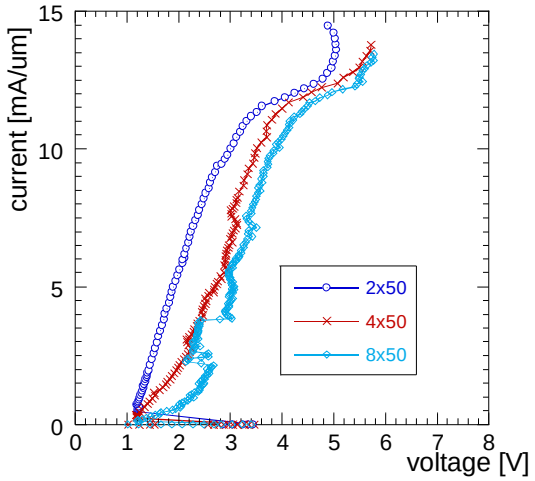

Figure 10. Normalized TLP data from 130nm PD technology for multi finger SCRs.

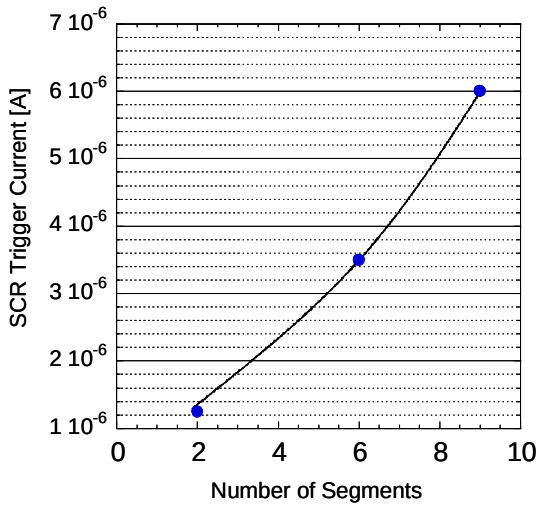

Figure 11. The SCR trigger current It1 for different number of segments for 130nm PD process (SCR width is 100um).

RG1/RG2 resistance variations– As in Bulk CMOS [6], [7] the trigger current of the SCR in SOI can be further adjusted to reach a predefined value by placing external resistors in parallel with the well resistances. Lower effective well resistances result in higher trigger currents. A low resistance value, for instance 5Ohm, increases this current from less than 1mA to more than 100mA (Figure 12).

LAC Variations - Another important parameter for the SCR design is the anode-cathode spacing LAC (cross section of Figure 6). Selecting a value which is too small results in a leaky device. However, increasing this value also increases Ron and Vh, and slows down the SCR triggering.

Figure 13 illustrates the leakage evolution as a function of the applied DC voltage for SCR bodies with different LAC spacing. The sudden increase in current for a certain voltage level is attributed to punch through. The smaller the LAC, the lower the voltage at which this punch through effect occurs. Figure 14 also shows the temperature dependency of the leakage current of the SCR. The data shown is for an 80um wide DTSCR in a PD 65nm SOI technology with a LAC of 0.7um.

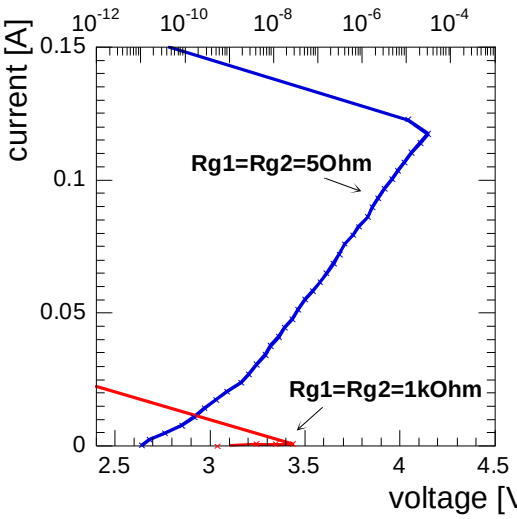

Figure 12. Influence of the parallel Rg1/Rg2 resistors on the trigger current It1 (130nm PD SOI).

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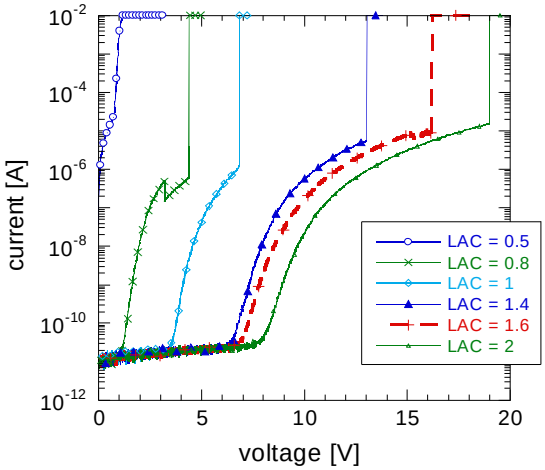

Figure 13. Leakage current for different values of LAC as a function of the voltage for a 130nm PD process (SCR width is 100um).

For 60°C, the leakage current increases as compared to room temperature and the SCR triggers at about 1.1V which is slightly above the Vdd of 1V. For 125°C, the leakage current is too high, resulting in an unfunctional SCR device. This temperature influence illustrates the danger of choosing a too small spacing between anode and cathode.

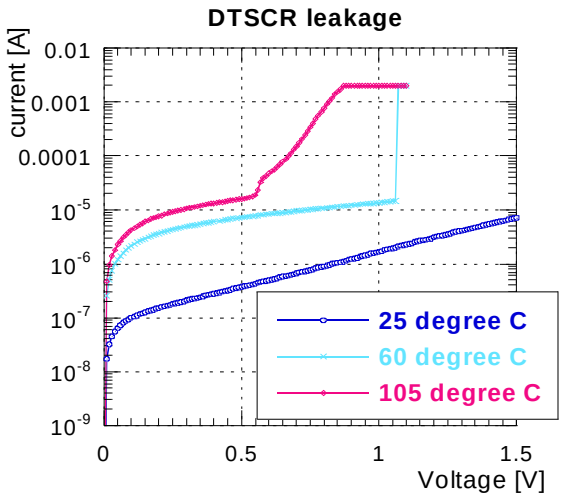

Figure 14. Temperature dependency of the leakage current of a DTSCR in PD 65nm SOI.

Number of contact rows - In Bulk CMOS, diodes and SCR devices tend to fail in the contacts. Because of the good heat dissipating capabilities of the Silicon Bulk, the silicon itself is not the limiting factor. Figure 15 presents data of a diode in a 130nm Bulk CMOS, showing significant performance increase by adding extra contact rows on the anode and/or cathode. This is different in case of SOI technologies.

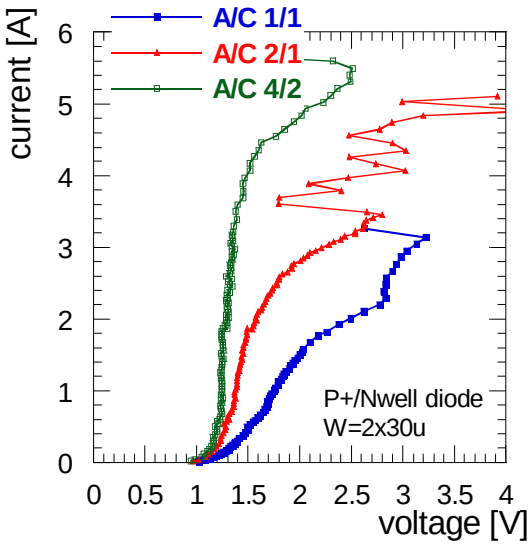

Figure 15. P+/Nwell diode in a 130nm bulk CMOS with different contact row configurations. (rows are defined per diode side)

Here it is the low heat dissipation capability due to the insulating oxide under the thin silicon film that limits the performance of the SCR. Figure 16 shows that adding additional contact rows to the anode and/or cathode does not increase the high current capability of the device. This demonstrates that in SOI SCR devices fail in the silicon itself. Also the Ron resistance does not change when adding extra contact rows, further proving that the high resistive thin Si film is the dominating parameter.

V.B. Modular design

The use of a modular approach where the trigger element is external to the SCR body, allows for optimization of the SCR separate from the trigger element and to adjust the Vt1 and/or the Vh to a desired level. An example of this modular approach is the DTSCR. Figure 17 presents the schematic of such a device [1]. Figure 18 presents measurement data on different holding and trigger diode configurations for a G2 triggered DTSCR in 130nm SOI. Each added trigger diodes increases the trigger voltage by 0.86V and each holding diode increases the holding voltage by 1V, but also acts as a trigger diode [1]. Because there is no danger of triggering a parasitic device, the number of diodes can in theory be increased to meet any desired voltage. Care must be taken however because each holding diode also increases the Ron of the device. This can increase the voltage above the maximum allowed voltage before the ESD specification is reached.

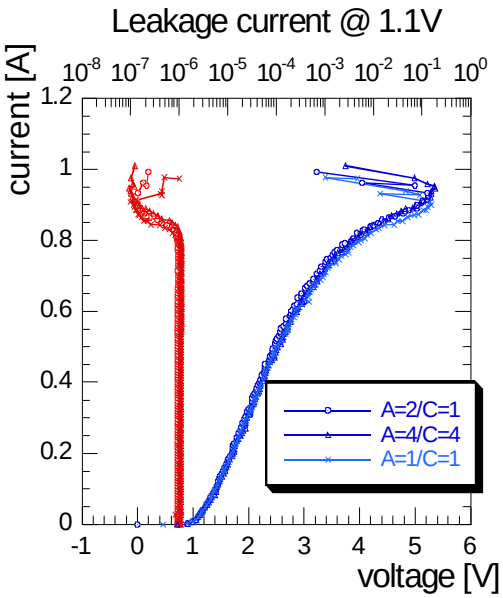

Figure 16. DTSCR with different contact row configurations. (rows are defined per SCR side)

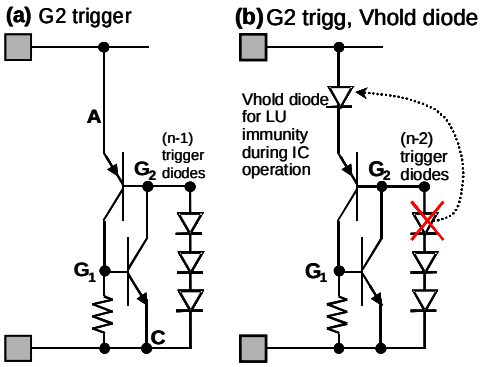

Figure 17. G2-triggered DTSCR (b/c): forward bias of Anode-G2 junction. Vhold diode for LU immunity allows removing one diode (c).

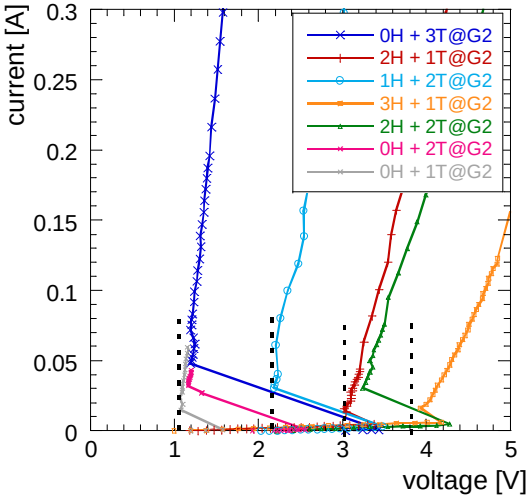

Figure 18. Different holding and trigger diode configuration for a G2 triggered DTSCR in a 130nm PD SOI technology.

V.C. Thin oxide protection

The ability to protect thin gate oxides was experimentally verified by placing a gate monitor in parallel to the SCR. Figure 19 presents TLP data on a DTSCR with a total width of 80um in a 65nm BST SOI technology. In this technology, the oxide has a thickness of 1.3nm with a BVox of 5V. The tests are performed both with a rise time of 10ns and 200ps. Figure 16 explains the principle of a DTSCR Even for the fastest transient there is no premature failure. This proves that the DTSCR is capable of protecting the thin gate oxide. The data also shows the lowering of the trigger voltage due to dV/dt effects (see inset). To prevent latch up in this technology due to ultra fast transients, the holding voltage of the SCR needs to be above Vdd. Figure 20 shows that also a GGSCR is capable of protecting a thin gate oxide.

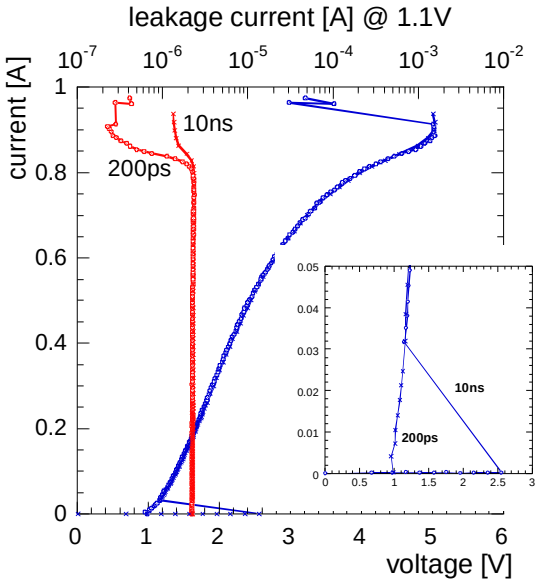

Figure 19. DTSCR (80um) in parallel with a 1.3nm GOX (65nm PD SOI) measured at 10ns and 200ps rise time.

The data for 10ns TLP tests for two different MOS trigger devices (one fully silicided and one with local bulk ties) demonstrates that the oxide is not damaged prematurely. The devices still exhibit the same high current performance as without the gate monitor in parallel.

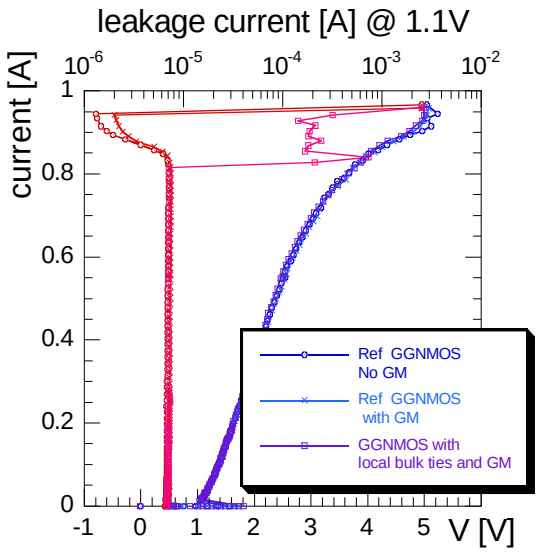

Figure 20. GGSCR devices (80um) in parallel with a 1.3nm GOX (65 PD SOI technology) measured with a 10ns rise time.

Conclusions

This paper shows that it is feasible to design a functional SCR in SOI technologies. Experimental data in different SOI technologies was presented to support this, showing a performance improvement of about 4 over snapback NMOS implementations, roughly the same as a diode. Cross-sections and layout of such a SCR was also presented along with a detailed discussion on the influence of various layout parameters. By using a modular approach to trigger the device body, it was shown that it is possible to protect thin gate oxides with this SCR structure.

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References

[1] M. Mergens, et al., “Diode-Triggered SCR (DTSCR) for RF-ESD Protection of BiCMOS SiGe HBTs and CMOS Ultra-Thin Gate Oxide”, IEDM 2003 proceedings.

[2] P. Raha, et al. “Prediction of ESD Protection Levels and Novel Protection Devices in Thin Film SOI Technology”, EOS/ESD 1997 proceedings.

[3] M. Chan, et al., “Comparison of ESD Protection Capability of SOI and BULK CMOS Output Buffers”, IRPS 1994 proceedings.

[4] S. Ramaswamy, et al. “EOS/ESD protection Circuit Design for Deep Submicron SOI Technology”, EOS/ESD 1995 proceedings.

[5] C. Russ, et al. “GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes”, EOS/ESD 2001 proceedings.

[6] M.Mergens, et al., “High Holding Current SCRs (HHI-SCR) for ESD Protection and Latch-up Immune IC Operation”, EOS/ESD 2002 proceedings.

[7] B. Van Camp, et al. “Current detection trigger scheme for SCR based ESD protection for output drivers in CMOS technologies avoiding competitive triggering”, EOS/ESD 2005 proceedings.

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Notes

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