Conference paper

SCR based ESD protection of Output Drivers in EPI technologies avoiding competitive triggering

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SCR based ESD protection of Output Drivers in EPI technologies avoiding competitive triggering

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Abstract – Self protective output drivers have been used extensively as an elegant solution against Electro Static Discharge. However, recent measurement data show unexpectedly low HBM and MM results in low resistive EPI technologies. The HBM-TLP correlation issue is investigated and a novel local parallel protection scheme for output drivers is presented, solving the competitive triggering issue using only a very small series (~10 Ohm) resistance without requiring the expensive Deep Nwell process step.

I. Introduction

For many years, the industry focused on self protective output drivers. The layout of the MOS output drivers is typically adapted to improve the ESD robustness by using silicide blocked junctions, deep Nwell and additional (ESD) implants. The same solution type is used for NMOS snapback based power protection between Vdd and Vss lines. However, recent measurement data showed that this self-protective technique has many issues due to non-uniform conduction. Moreover many correlation issues have been reported were excellent TLP data could not be confirmed with HBM or MM measurements.

This paper first presents measurement results, highlighting the industry wide problem with NMOS snapback elements in EPI technologies mainly with respect to low performance thresholds during HBM qualification. Secondly, a theory is presented to explain the low HBM-TLP correlation based on the tester parasitics. Finally the paper provides a simple and straightforward solution type for the weak output drivers with si-proven examples in a number of technologies.

II. Issues for Snapback NMOS devices in EPI technologies

Table 1 presents measurement results for two GOX1 snapback NMOS devices in a 0.18um technology on an EPI substrate. For both devices a perfect ESD performance is measured by the TLP system. Extremely low HBM and MM results show up for the first device, for the second qualification systems ('Tester2') while the results from the other tester ('Tester1') correlate reasonably well with the excellent TLP performance. This correlation problem is not visible for the deep Nwell device ('DNwell').

		Tester1		Tester2	
Device	TLP [A]	HBM [kV]	MM [V]	HBM [kV]	MM [V]
GOX1 NMOS	2.4	>4	180	0.9	80
GOX1 NMOS, DNwell	2.5	3.6	220	3.2	220

Table 1: Measurement results for two GOX1 devices in a 0.18um EPI technology. The TLP results are compared with HBM and MM results from two different qualification test systems. Large differences are found between the qualification testers except for the Deep Nwell device.

		Tester1		Tester2	
Device	TLP [mA/um]	HBM [kV]	MM [V]	HBM [kV]	MM [V]
GOX1 DNW	7.2	>4	220	4	275
GOX2 DNW	5	3.8	160	2.8	200

Table 2: Measurement results for GOX1 and GOX2 snapback NMOS devices within an isolated Pwell (Deep Nwell implementation) implemented in a 0.18um technology. Good HBM-TLP correlation and tester-tester correlation is achieved for these device types.

When Deep Nwell is used under the NMOS devices, the correlation issues are no longer evident as is shown in Table 2.

These results are confirmed in other advanced EPI technologies where low HBM, MM performance is found for NMOS devices without Deep Nwell. Moreover a large statistical spread is found in the HBM data.

In the next part, an explanation is provided for the low correlation factor.

III. HBM-TLP correlation issue

Recently many sources reported HBM-TLP correlation issues. The TLP is a measurement tool typically used during the ESD strategy development while HBM is used in the final qualification stage of the IO libraries and IC products. In all cases reported, good TLP results remained unconfirmed with the traditional HBM qualification measurement results.

Different theories have been formulated since the 2004 EOS/ESD symposium. The main artifacts are summarized in the overview on Figure 1.

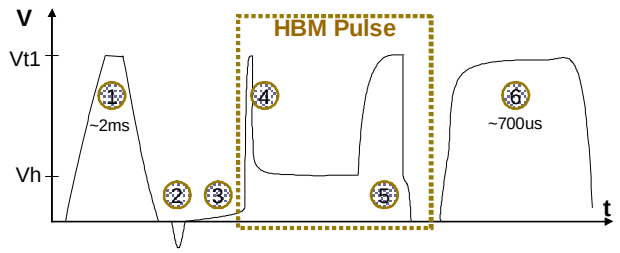

Figure 1: Overview of the different artefacts that are important in the study of the correlation issues. The artefacts are shown in the voltage scale.

A few measurement artifacts are reported to precede the real standardized HBM pulse (in dashed box on Figure 1). Ashton et al. [1] highlighted the 'pre-pulse' (1) and the slow initial voltage rise (3) before the actual HBM discharge. Barth et al., amongst others, presented evidence that a negative voltage pulse can be present in positive HBM stress pulses. Further, the dV/dt pulse behavior (4) has been studied before. Certainly for low leakage devices a turn-off & retriggering (5) can be measured quite often. Finally, Duvvury [2] and Meuse [3] presented the trailing pulse (6) as the cause of some degradation problems.

In this paper, the focus is on aspect (4), the influence of the dV/dt and dI/dt on the device behavior and on the ESD performance. The test-board capacitance Ct and Inductance Ls (Figure 3, top) influence the pulse dynamics (rate of change of Voltage and Current) before and after DUT triggering.

A. V, I rate change during the HBM pulse

HBM waveforms are typically believed to have a lower dV/dt compared to TLP due to the higher test board capacitance Ct for HBM. This lower rate of voltage change has been extensively discussed in literature and occurs after the triggering of the protection device into a low ohmic state. The larger inductance in the HBM testers also limits the rise of the current.

However before the protection element triggers, the device behaves as an open circuit and the HBM tester exhibit a higher initial dV/dt in HBM as compared to TLP. This is due to a difference in the electric circuitry between HBM and TLP. During this timeframe, the DUT and test-board capacitance are charged thru RHBM=1.5kOhm.

As a summary for HBM: The dV/dt rate is high before triggering the protection element, while it is reduced once the protection element is conducting current. dI/dt is lower after triggering due to a larger inductance in the HBM tester.

B. Influence on ggNMOS behavior

A change in transient dV/dt and dI/dt behavior has a significant impact on the multi-finger triggering behavior in NMOS snapback clamps.

Since the initial dV/dt is large, a good Vt1 reduction for ggNMOS devices (Vt1') is evident from Figure 2 and allows an easy turn on of the first device finger. Once the protection device is turned on, the dV/dt decreases due to the inductor and parasitic capacitance and this change increases the Vt1 for remaining device fingers. Multi-finger GGNMOS devices are most susceptible for this dV/dt rate change.

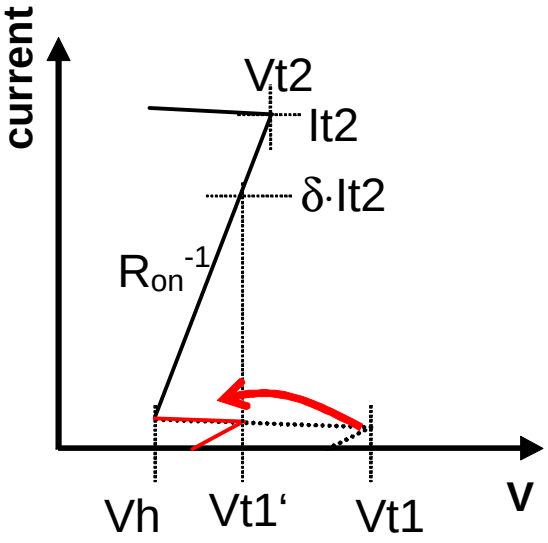

Figure 2: Vt1 trigger voltage reduction due to fast voltage rise before triggering

C. Additional current injection from the test board capacitance during snapback

Just prior to NMOS triggering, the parallel test board capacitance is charged up to Vt1 as is shown in Figure 3, top drawing.

When the protection element is brought into snapback, the voltage is reduced from the Vt1 trigger voltage to the holding voltage Vh. This voltage drop creates an additional current pulse from the discharge of the Ct capacitance into the protection device shown in the bottom drawing of Figure 3.

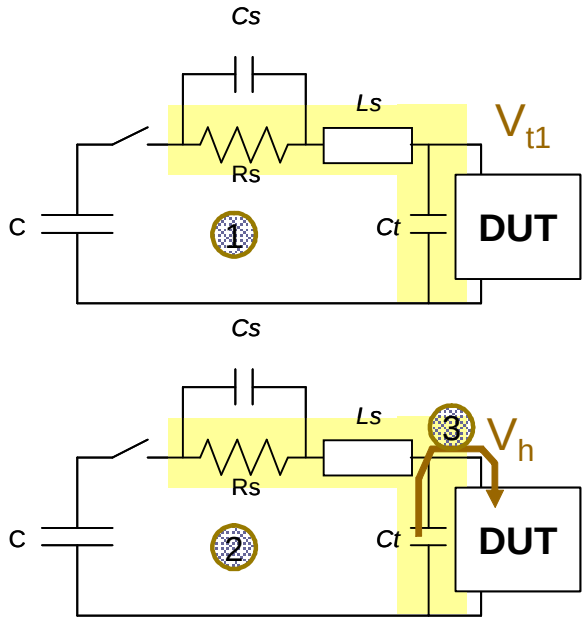

Figure 3: At snapback, the voltage drop over the Device Under Test (DUT) is suddenly reduced from the Vt1 (top) to the holding voltage (bottom). This voltage drop is accompanied by an additional current stress from the discharge of the testboard capacitance Ct.

The additional current peak can easily damage the ggNMOS device exactly at its weakest point with only a limited number of fingers triggered. This provides an explanation for the extremely low HBM values even for ggNMOS devices with a large number of device fingers.

Next, the paper focuses on different ways to create ESD robust output drivers.

IV. Output driver solution in EPI technologies

Different approaches exist for ESD robust Output protection. This part of the paper will first briefly discuss the standard approaches. In the final part, the novel RTSCR protection principle is explained in detail.

When designing an ESD protection for output driver pins, one of two methods can be applied: (A) The output drivers are made self-protective to allow the main ESD current through the drivers or (B) parallel protection elements are added for shunting the main ESD current.

A. Self-protective MOS drivers

For self-protective MOS drivers the layout needs to be altered to obtain a driver that is robust enough to conduct all the ESD current. Therefore, the total gate width is increased by including dummy fingers, proportional to the desired ESD level. Further, ballasting is typically added at the drain side. Ballast can be added through the use of silicide blocked junctions, well ballast or back-end ballasting (BEB) techniques [4-7].

The major drawback of this self-protective approach is the high area cost: each driver has to be strong enough to take all the ESD stress current. The typical total gate width is around 400-700um. Perpendicular to the gate width, the pitch is also increased by introducing ballasting. As explained above, a low correlation factor between HBM and TLP data for self-protective drivers is often seen. (e.g. Table 1, Table 2).

Because of these difficulties, self-protective are often not an attractive solution for advanced technologies.

B. Parallel protection elements

In this approach, a parallel current path is created for shunting the ESD current. The main issue to solve is the trigger competition between the two current paths: NMOS driver versus the ESD clamp. Different ways are used to limit the ESD current through the driver:

- Reduce the trigger voltage of the parallel clamp.
- Add a large resistance (>50 Ohm) (Figure 4).
- Increase the Vt1 trigger voltage of the driver by gate/bulk bias-schemes [8-9].

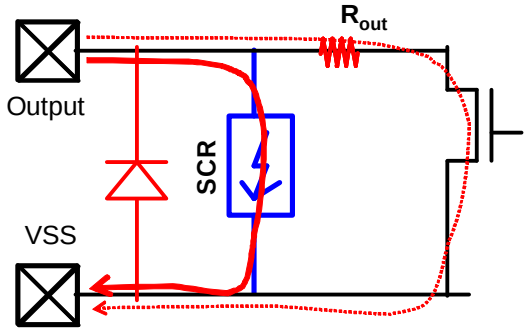

Figure 4: Local SCR clamp in parallel to the output driver: Carefull design of the output resistance is required to avoid competitive triggering issues. The resistance limits the current through the driver and builds up voltage required to trigger the SCR. The SCR conducts the main ESD current.

These 2 approaches have a big impact on the normal operation. To avoid the drawbacks of these methods, a novel SCR based solution is presented, called a Resistor Trigger Silicon Controlled Rectifier (RTSCR). The next paragraph explains the mechanism of the device and shows measurement results obtained in various CMOS technologies.

V. RTSCR principle

The basic idea behind the RTSCR is to detect ESD by monitoring the current flow into the driver. When this current exceeds a predefined level, the chip is diagnosed to suffer from ESD stress. This condition automatically triggers the protection device. For output protection this solution is highly preferable.

A. Basic schematic and principle

The typical schematic is shown in Figure 5. Three devices can be distinguished:

- The NMOS driver. The width of this device is determined by normal operation conditions, and the gate width is therefore typically not altered by the ESD protection strategy. This NMOS driver conducts the ESD current for the first nanosecond(s) and needs appropriate ballasting to prevent failure due to this current.
- The SCR. This device stays off during normal operation. During ESD, it conducts the main current. Therefore its layout can be freely determined by the ESD engineer.
- The resistor Rs. The resistance will act as the ESD detection circuit. Its value is determined by both normal operation and ESD considerations.

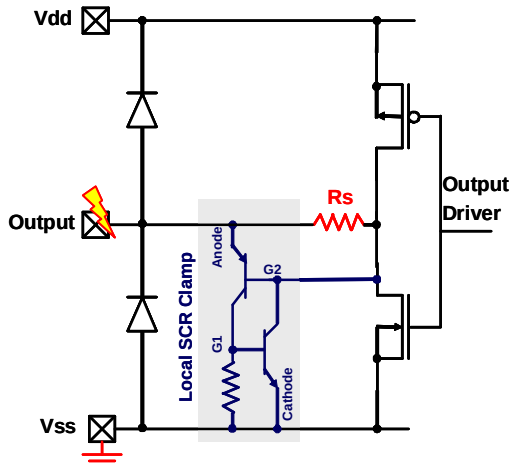

Figure 5: Schematic of the RTSCR protection device for an NMOS output driver. The SCR is triggered in a low ohmic conduction state at a fixed current level, through the NMOS. The current level is determined by the Rs resistance.

Key to the design of the RTSCR is the value of the Rs resistor. Apart from the obvious condition that Rs cannot compromise normal operation driver performance (and thus defines an absolute maximum resistance value), there are two conditions to be met:

- During normal operation the amount of current in the output pad is determined by the MOS operation of the driver. This current is typically around 0.5 mA per um NMOS gate width. The maximum value of the Rs resistor is determined by this current such that the voltage drop for maximum drive current ($I_{driver,max}$) is limited to about 300 mV, keeping the parallel SCR local clamp off.
- In ESD conditions, however, the same driver can take much more current in parasitic bipolar mode ($I_{t2,driver}$ > 5mA/um). Therefore, the voltage drop over the series resistor Rs is much larger. The minimum value of the resistance Rs can then be calculated such that >800 mV bias is generated over the anode-G2 diode junction of the SCR, turning on the local protection element.

B. Measurement results

The measurements are performed using a Barth Electronics Inc. TLP system with a fixed pulse width of 100ns. Devices from different CMOS technologies were analyzed: 0.6um 5V; 0.18um EPI TSMC 3.3V; 0.13um EPI TSMC 3.3V.

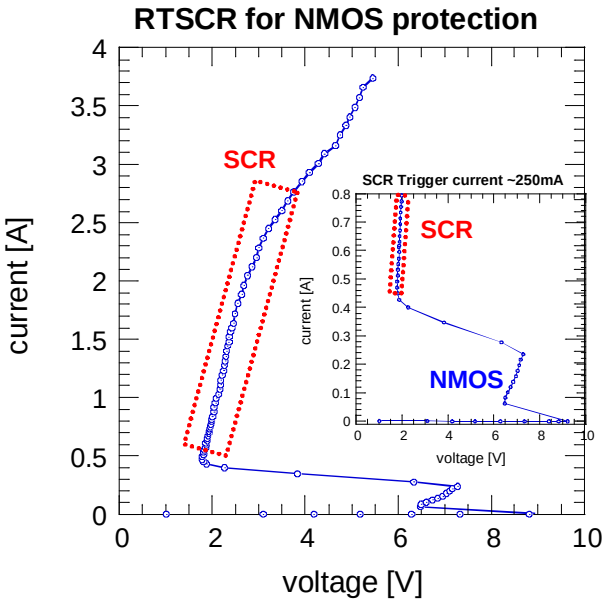

Figure 6: RTSCR measurement in a 0.6um 5V CMOS technology. Resistance value Rs=2 Ohm. The SCR (width=30um) conducts the main ESD current. ESD currents below 250mA are handled by the NMOS driver.

Figure 6 shows the basic principle for an NMOS of W= 4x34um in a 0.6um technology. It2 of this driver is ~5mA/um. At low current levels, the NMOS is conducting in the parasitic bipolar mode. For ESD current below 250mA the voltage drop over the isolation resistance (value ~2 Ohm) is too low to forward bias the Anode-G2 junction. The SCR is only triggered for current levels above 250mA. The inset of the figure depicts a close-up of the triggering of the NMOS and SCR.

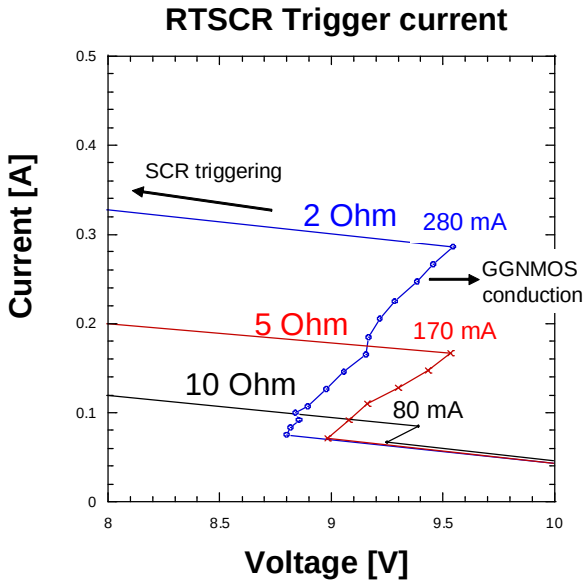

Figure 7: RTSCR measurement close up for 3 values of the resistance in a 0.6um technology. The SCR trigger current is shown to increase with decreasing resistance values.

In Figure 7, an SCR (70um wide) is triggered at different current levels for three values of the resistance. The NMOS driver (180um wide) has a gate length of 6um, about 3 times the minimum design rule value for a transistor with this particular implant. The It2 of the driver was only ~500mA. The maximum drive current during normal operation is defined as 20 uA. Three different variations of Rs are shown. Even for the largest value, 10 Ohm, there is no danger of triggering the SCR in normal operation, unless the maximum driver current exceeds ~70mA. A high It2 (~100mA/um) for all implementations was found (not shown in the figure). As expected, this SCR failure current is independent of the value of Rs.

In Figure 7, one can clearly see that the trigger current of the SCR decreases with increasing Rs. Analytically, Rs*It1~800 mV. For the Rs = 2 Ohm case, this calculation deviates slightly (280mA*2Ohm ~ 560 mV), because of the lower accuracy for the low ohmic resistors. These measurements clearly show that the Rs resistance can be used to tune the current level at which triggering of the protection device occurs. Figure 8 summarizes TLP results of the same concept applied in 0.18um TSMC technology on EPI. Different values for the resistance Rs and different NMOS driver implementations are shown together. The It2 current level for the SCR is always above 7A and HBM above 8kV. All the different driver implementations are protected by the SCR protection. The different driver implementations included 1.2V and 3.3V drivers and width variations.

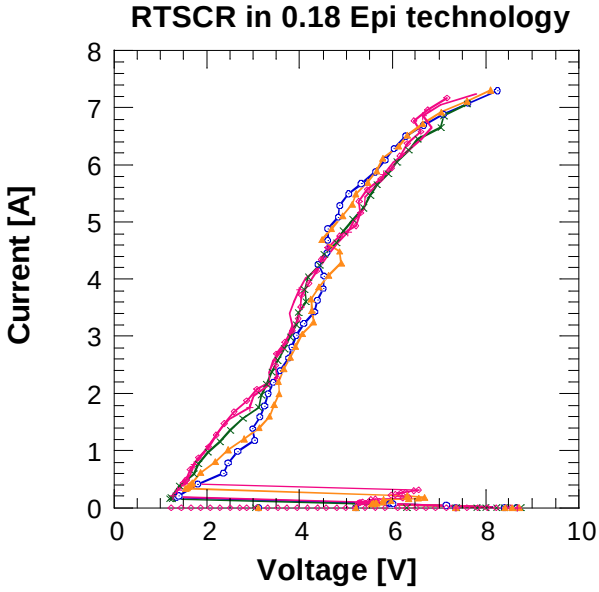

Figure 8: RTSCR measurement results in a 0.18um EPI TSMC technology for different values of R and different NMOS drivers (width and DCGS variations). The resistance and driver influence the SCR trigger behaviour, as was shown in Figure 7, but the high current regime is the same for all implementations (W_{SCR} = 2 x 50)

In Figure 9, the IV curves of two RTSCRs (2x40um wide) are shown in a 0.13um EPI technology using 2 values for Rs. There is one major difference in implementation as compared to the RTSCR in the 0.18um technology depicted in Figure 8: for the 0.13um structures, the gate of the NMOS is coupled high. This can be seen in the measurements from the fact that there is no snapback in the MOS conduction regime. (Figure 10) The voltage at the gate of the driver does not affect the triggering principle of the RTSCR.

Technology	SCR size [um]	TLP [A]	HBM [kV]
0.6 um CMOS	70	7.2	>8
0.18 um EPI	2 x 40	6.0	>8

Table 3: Summary of achieved RTSCR protection HBM levels and correlation with TLP results.

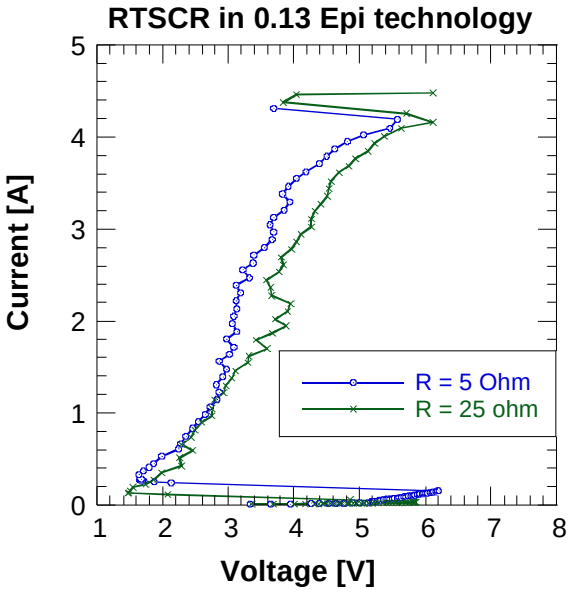

Figure 9: RTSCR in 0.13um technology. The gate of the driver is coupled high, such that no snapback is seen in the NMOS conduction regime.(see Figure 10). This way the worst case for the competitive triggering issue is simulated.

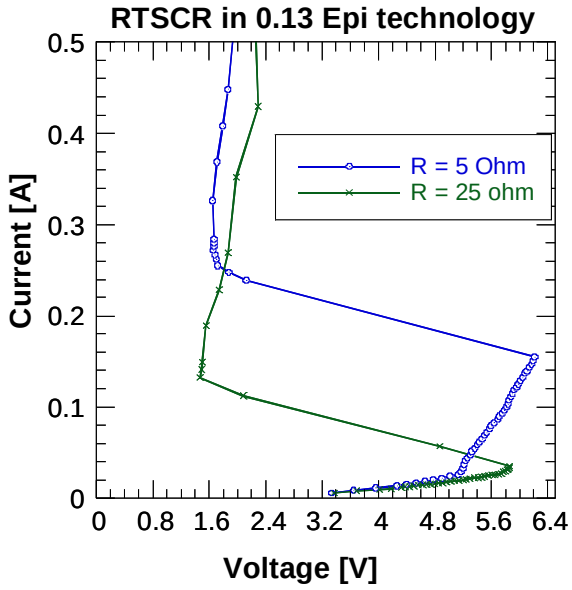

Figure 10: Zoom of triggering behaviour of RTSCR in 0.13um technology (Figure 9)

One of the key advantages of the RTSCR is that it solves much of the HBM-TLP correlation issues typically seen for self protective MOS devices. In the 0.6um and 0.18um technologies, low correlation between the HBM failure values and the TLP failure levels are found for ggNMOS devices. The RTSCR devices however did not exhibit the same weakness to HBM stresses, as can be seen from Table 3. All RTSCRs can protect the drivers up to high HBM levels (> 8 kV, the maximum level of the used tester).

Conclusions

In this paper a novel protection concept is presented, to improve ESD protection for output drivers. High protection levels are achieved, with only a minimal impact on normal operation. Measurements from various CMOS technologies are used to show the analytical alterable trigger current, and the high It2 level. The technique is applicable both for NMOS and PMOS output drivers. The main advantage of this concept is a much smaller Si area (down to 30%) required for implementing ESD protection of output drivers, depending on the drive strength for normal operation and the maximum resistance value allowed.

References

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Our business models include

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  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

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