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Concept for Body Coupling in SOI MOS Transistors to Improve Multi-Finger Triggering

EOS/ESD symposium 2006

Multi-finger SOI MOS devices exhibit a low ESD failure current, related to the thin Si-film and the complete isolation of the transistor body regions, causing non]uniform conduction in bipolar snapback mode. The traditional layout approaches (silicide blocked junctions, increased gate length) are compared and a novel layout concept is proposed to improve uniform triggering. Excellent ESD performance around 3mA/um2 is achieved for minimum dimension, fully silicided devices in a 90nm SOI technology.

Concept for Body Coupling in SOI MOS Transistors to Improve Multi-Finger Triggering

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Abstract: Multi-finger SOI MOS devices exhibit a low ESD failure current, related to the thin Si-film and the complete isolation of the transistor body regions, causing non-uniform conduction in bipolar snapback mode. The traditional layout approaches (silicide blocked junctions, increased gate length) are compared and a novel layout concept is proposed to improve uniform triggering. Excellent ESD performance around 3mA/um2 is achieved for minimum dimension, fully silicided devices in a 90nm SOI technology.

I. Introduction

Recently, advanced SOI technology nodes are being used more extensively due to a number of advantages mainly related to the reduction of the power consumption, smaller silicon area, shorter gate delay and reduced parasitic junction capacitance. Moreover, due to the completely isolated transistors, latch-up is no longer an issue.

However, SOI technology comes also with disadvantages such as the higher cost for the starting material, floating body and history effects, increased self-heating issues and a higher design complexity. Another main disadvantage is the fact that traditional snapback-based ESD solutions have a much reduced (It2) failure current. This It2 reduction compared to bulk is related to the thin silicon film and the complete isolation of the transistors which limits the dissipation and transfer of the generated heat.

For NMOS/PMOS transistors, the complete isolation in SOI (BOX and STI) also limits the transfer of the base potential between adjacent fingers. On Figure 1, the cross section of a multi-finger NMOS device is shown for bulk and SOI processes. Snapback operation of ggNMOS transistors always starts in a single finger. In the case of bulk technologies, the NPN base potential of the triggered finger is easily transferred to the adjacent fingers. The avalanche generated holes flow to the closest P+ (gnd) connection, slightly forward biasing the bulk-source junctions of the adjacent fingers. The Vt1 reduction associated with this increased base potential enhances multi-finger triggering without the need for ballast resistance at the drain junctions [1]. For SOI technologies, the base regions of adjacent NPN transistors are completely separated and the transfer of the base potential is impossible.

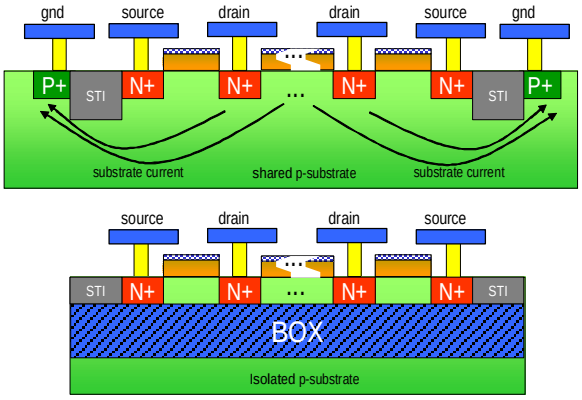

Figure 1. Graphical representation of the cross section of NMOS transistors in bulk and SOI processes. In bulk technology, the bipolar NPN base (P-bulk) potential from one finger can easily be transferred to the adjacent fingers because all the NPN base regions are created in a shared p-substrate. For thin film SOI processes, the base regions for each of the parasitic NPN devices are completely isolated from each other, preventing this potential transfer.

The paper is organized as follows: Section two presents a brief description of the technology and related design windows for output protection. Section three discusses the classical or traditional protection options and presents measurements results that serve as a reference or benchmark. Next, a layout concept is proposed to enhance multi-finger triggering in minimum dimension, fully silicided drivers. Layout and measurement data are provided. Finally conclusions are given.

II. SOI MOS Devices

The studied advanced low leakage 90 nm Partially Depleted (PD) SOI technology with a film thickness of 75nm features MOS transistors with 2 gate oxide thicknesses: GOX1 (2.3nm – 1.2V) and GOX2 (7.5nm – 3.3V). The maximum channel width is limited to reduce the Kink effect [2]. Due to this design rule, the NMOS fingers are divided into different segments as shown on the layout (right) and cross section AA' (bottom) of Figure 2. The segmentation prevents uniform bipolar conduction across segments even inside a single MOS finger.

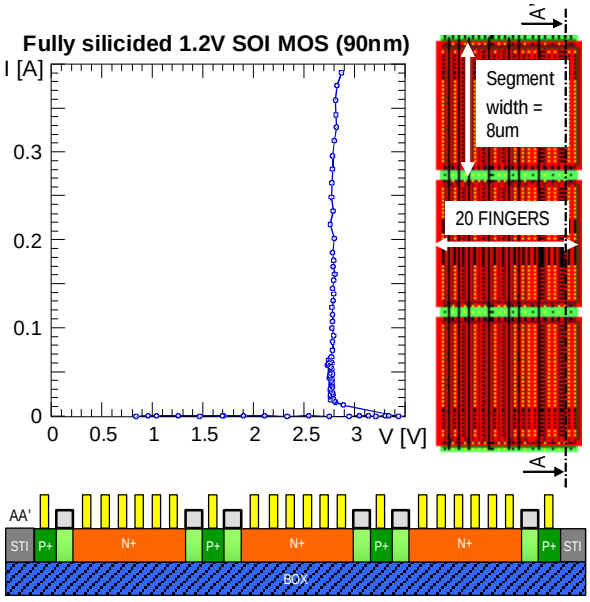

Figure 2: IV characteristic for a fully silicided GOX1 (1.2V) NMOS device. The total device width is 480um and is constructed as 20 fingers of 3 segments of 8um each (depicted on the right).

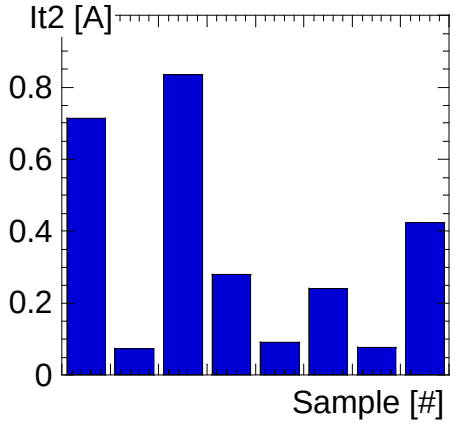

Figure 3: Limited statistical study of the It2 failure current for identical fully silicided GOX1 (1.2V) NMOS devices of 480um. A low average and minimum performance and a large statistical variation are shown.

All the MOS devices in this study have a total device width of 480um, constructed as 20 fingers of 3 segments of 8um each, as depicted on the right side of Figure 2. Measurements have been performed using Barth 100ns TLP systems. The last IV point in the IV plots depicts the failure.

This paper focuses on the thin oxide NMOS output driver device, because it represents the worst case due to the very low trigger and holding voltage. The IV curve for a 1.2V SOI NMOS transistor is shown on Figure 2 (left). The Vt1 of 3.4V and holding voltage of 2.8V are much lower compared to 90nm bulk technologies as is evident from Table 1, and from earlier publications [3, 4].

Fully silicide ggNMOS	Proprietary (i.e. non-foundry) 90nm SOI	Foundry 90nm BULK	Proprietary 90nm BULK
Vt1 [V]	3.4	4.6	5.1
Vh [V]	2.8	3.5	3.5

Table 1: Comparison of GOX1 NMOS Vt1 trigger voltage and Vh holding voltage between 90nm SOI and BULK technologies.

Moreover, as outlined above, the It2 failure current is very low (0.15 – 1.7 mA/um). Finally, because the Vt2 failure voltage is lower than the Vt1 trigger voltage, uniform triggering over all fingers cannot be guaranteed [5]. This is evident from the large statistical variation measured and plotted on Figure 3.

III. Traditional ESD solutions

This section provides a comparison of different protection approaches for the ESD protection of SOI MOS output drivers. Three basic protection techniques exist for MOS devices.

A. Self protective approach

In mature or mainstream bulk technologies, the self-protective output drivers are still heavily used. In that case all the ESD current is shunted by the output drivers. Typically ballast resistance at the drain side and inclusion of dummy fingers is required, which drastically increases the total silicon area. This approach is commonly used for over voltage tolerant pins (no diode to VDD). When the self protective approach is applied for SOI MOS, the macro ballast resistance needs to be increased because it is less effective due to the reduced intrinsic current capability. The effect is slightly compensated by the smaller difference between the Vt1 and Vh voltages.

One of the traditional forms of ballast resistance is the use of silicide blocked (drain) junctions.

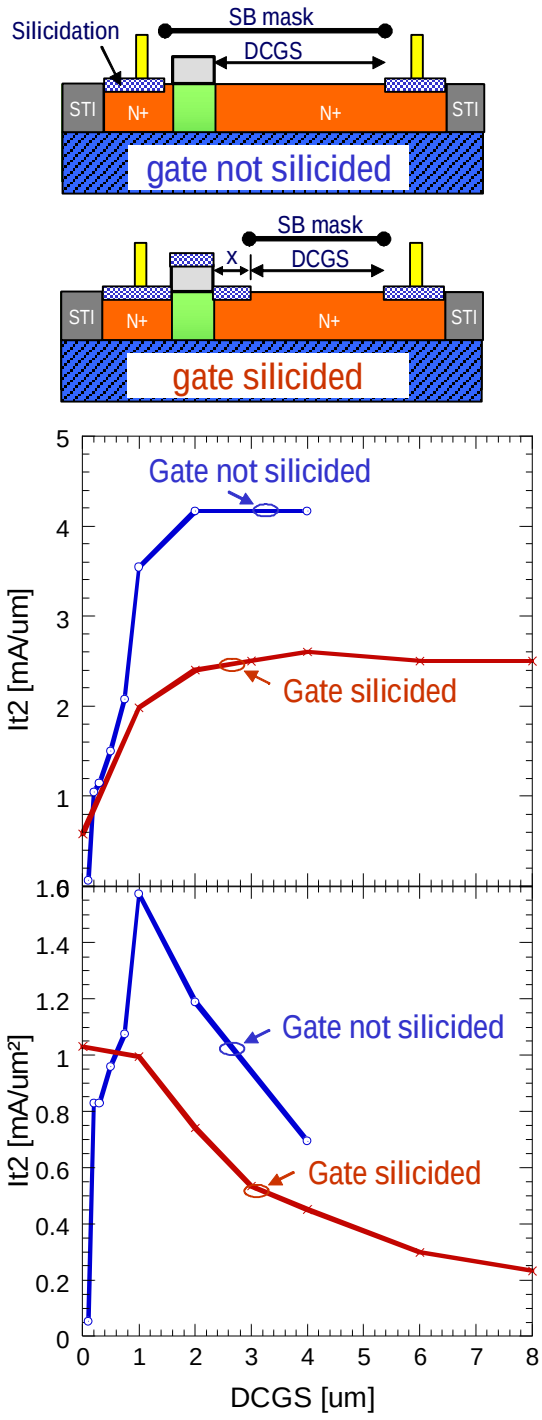

Figure 4: Normalized ESD performance (It2 failure current) per perimeter (top) and per area (bottom) for different DCGS variations. Two types of silicide blocked approaches are studied with the main difference in the silicidation of the gate. 1um presents the optimum value. All devices have a MDR (Minimum Design Rule) gate length of 0.1um. The 'X' distance in the 'gate silicided' cross section is 0.22um.

Figure 4 presents measurement results for the TLP-It2 performance per perimeter and per area for different DCGS (Drain Contact to Gate Spacing) variations. Two types of silicide blocked junctions are compared: 'Gate not silicided' is the oldest approach; 'Gate silicided' has a 'window' style silicide block area at the drain. This window style is introduced to reduce the gate resistance (silicided gate) and to reduce the related RC delay. The disadvantage of this second type is the inclusion of a partly silicided drain junction close to the gate, which has a bad effect on the failure current as is evident from the measurement results on Figure 4.

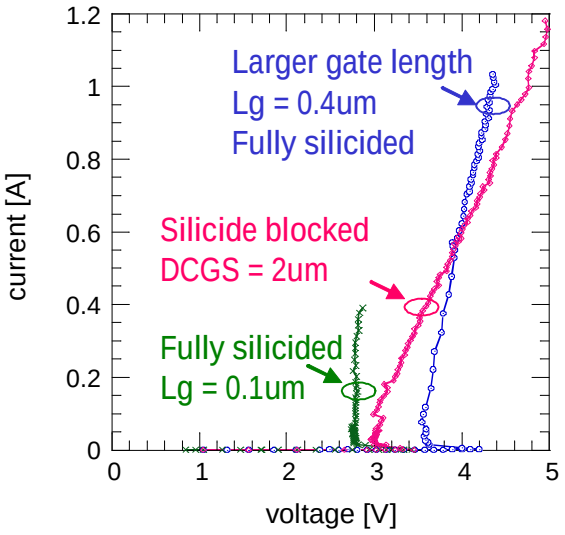

Figure 5: Comparison of GOX1 NMOS variations to improve robustness as compared to fully silicided transistors. An increase of the gate length or inclusion of silicide blocked drain junctions drastically enhances the It2 failure current through enforcing multi-finger triggering at the expense of a higher voltage drop.

Other approaches exist to improve the robustness. For advanced processes, the reverse poly effect [6] states that the It2 performance is higher for devices with a larger-then-minimal gate length. The effect is also visible in the studied 90nm technology as is evident from Figure 5 and Figure 6. The larger gate length reduces the difference between the Vt1 trigger voltage and the holding voltage and increases the Vt2 failure voltage.

B. No ESD current through drivers

A second approach, opposite to the self protective approach, is to prevent the ESD current flow through the driver. In this case the ESD protection needs to limit the voltage below the failure voltage (Vt2). The advantage, when successful, is that the smallest size, fully silicided transistors can be used as output drivers to obtain the highest speed. The protection can be achieved using the dual diode approach and an efficient power

protection using transient triggered active MOSFET rail clamps [3,7] or Silicon Controlled Rectifiers [8].

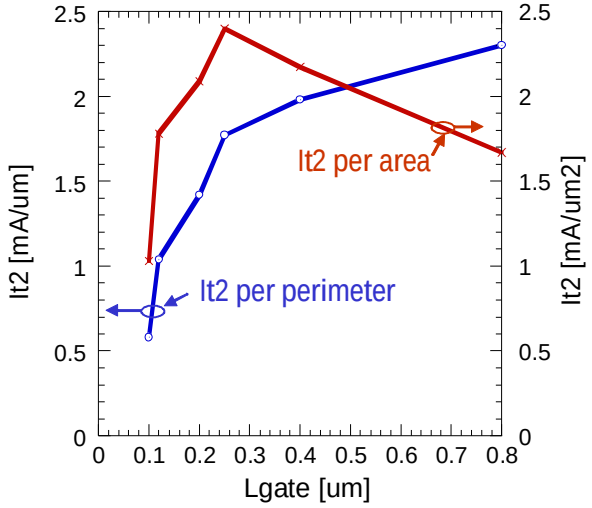

Figure 6: Normalized ESD performance (It2) per perimeter and per area for different gate length variations for fully silicided devices. The reverse poly effect is clearly visible through the much reduced ESD performance for the minimum gate length devices.

Because the Vt1, Vh and Vt2 of the to-be-protected fully silicided drivers is a lot lower in SOI, the total voltage drop over the power bus (Vdd or Vss), power clamp and diode needs to be watched carefully in such a protection scheme. Using the data from Table 1, it is obvious that the maximum voltage in the design window is extremely low. Besides selecting a low Vt1 triggered power protection, a low ohmic diode is required. To limit the total voltage drop over the diodes, gated diodes, also known as lubistors, introduced firstly by Oomura [9] can be used.

Another method uses a parallel local protection element placed at the IO. This way the influence from the bus resistance is taken out. SCR based clamps [8,10,11] are all viable candidates.

C. Limited ESD current through drivers

A third option is to add a current limiting series resistance. When a small output series resistance (~5-10 Ohm) is tolerated, the ESD current through the driver can be limited while the maximum allowable voltage at the pad is increased. In this case, the transistors still require some form of ballasting but the total area is limited. A detailed summary of the different options for this method is provided in [12].

The selection of the optimal solution depends on factors such as bus resistance, ESD specifications, tolerated series resistance, driver size and maximum IO ESD area. The next section proposes a novel layout concept that improves the robustness of fully silicided MOS transistors by restoring the body coupling between adjacent fingers. It represents an area efficient solution for GOX1 MOS driver protection.

IV. Body coupling concept

In the regular SOI MOS layout there is a complete isolation of the body regions of the different fingers as presented on Figure 1. In many technologies the body is not even connected (‘floating body’). In the case of body-contacted SOI, different methods exist to connect the body of the transistors, such as H/T-type gate edge (depicted in Figure 7) or Partial Trench Isolation (PTI). In both cases, the body connection occurs only at the edge, along the transistor length, Moreover, these body connections at the end of the segments are shorted together and all connected to the ground potential, effectively preventing inter-segment and inter-finger body or base coupling.

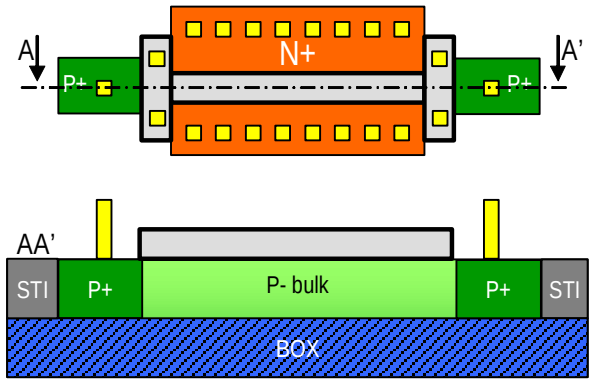

Figure 7: Standard NMOS device in SOI technology: layout and cross section for the H-type gate edge approach.

The purpose of the **body coupling concept** is to restore the body coupling between adjacent fingers. In the standard SOI MOS implementation, a number of elements block the free flow of charges between adjacent fingers: the BOX at the bottom, STI and P+ in between the segments and N+ drain and source junctions (S/D) between the fingers, depicted in Figure 8, cross section BB’.

The main idea of the body coupling concept is to create a ‘channel’ for charges by connecting the body regions of adjacent driver fingers. It is not possible to create this channel through the BOX. However, a ‘channel’ or connection can be implemented by interrupting the N+ source and drain junctions. Different layout approaches exist to create this ‘channel’ through the N+ junctions:

(1) Interrupt the N+ implant mask with a regular spacing, leaving active area with only lowly doped Pwell regions in between (Figure 8, cross section CC’). A somewhat resistive connection is created in between the fingers.

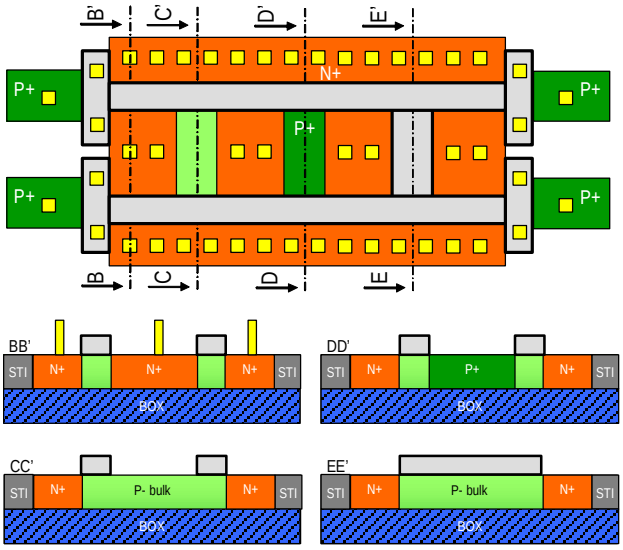

Figure 8: Layout view and cross sections of different approaches to connect the body regions of the adjacent fingers. Cross section BB' represents the traditional SOI MOS cross section for multi- finger structures. In cross section CC', the N+ implantation is blocked, leaving P- regions. The insertion of P+ islands as in cross section DD' effectively shorts the body regions of neighbor fingers. Finally, by locally adding a poly stripe (EE') a P-connection is created between the fingers.

(2) Replace the N+ implant mask by P+ rectangles at a regular pace. The highly doped P+ creates a low ohmic connection between the body regions (Figure 8, cross section DD').

(3) The first two solutions require a carefully aligned pattern of silicide block to prevent the electrical connection between the drain or source junction with the body regions and a larger gate length in case 2 to align N+ and P+ masks. A more area efficient solution consists of the inclusion of (vertical) poly gate regions (Figure 8, cross section EE') between the different fingers on a regular pitch, creating a regular grid-type poly layout. The gate poly masks the N+ implantation during processing, creating P- channels under the vertical gates.

The Body Coupled MOS (BCMOS) layout, depicted in Figure 9, enhances the transfer of the body potential between different fingers through the P-channels under the additional vertical poly stripes. This most area efficient approach can be mixed easily with the other approaches (1,2 mentioned above) when the gate of adjacent fingers is connected to different pre-driver circuitry.

Figure 10 presents measurement data for Body Coupled MOS devices with a variation of the vertical poly stripe pitch. From the IV curves it is evident from the on-resistance and It2 failure current that the devices with larger poly pitch (2 and 4um) are not triggered completely. The performance increases for a small pitch because this represents improved inter finger body coupling.

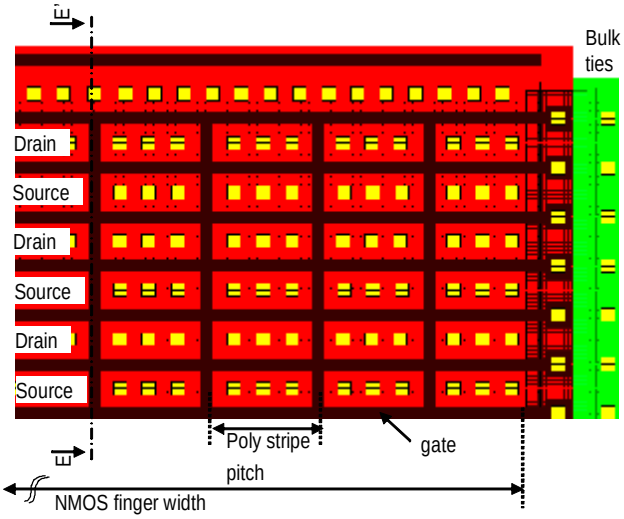

Figure 9: Layout representation of the Body Coupled MOS structure. The design is based on the minimum dimension fully silicided MOS transistor and adds vertical poly stripes to enhance body coupling between adjacent fingers. Cross section EE' is depicted in Figure 8. The top poly line of the structure is a 'dummy' poly added for improved gate etch control.

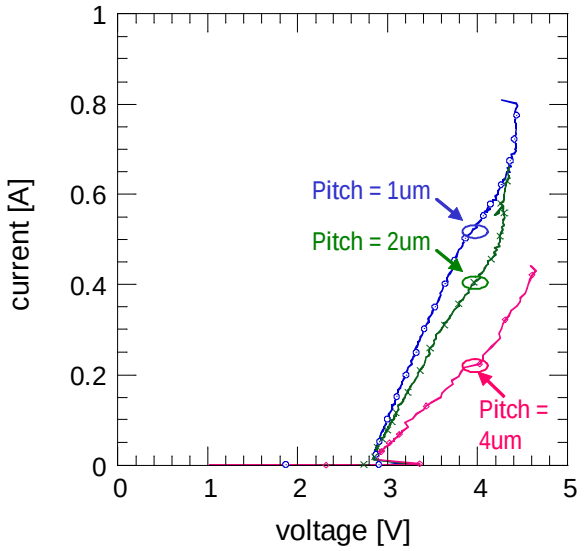

Figure 10: TLP IV characteristics for different vertical poly pitch variations.

The normalized It2 measurement data summarized on Figure 11 clearly shows the performance improvement in uniform triggering by restoring the inter finger body coupling. Also, Table 2 presents a summary of the ESD performance for the different variations discussed above. Although the Body Coupled MOS has a lower ESD performance per perimeter as compared to the silicide

blocked variations and larger gate length, there is a clear area advantage for the novel approach.

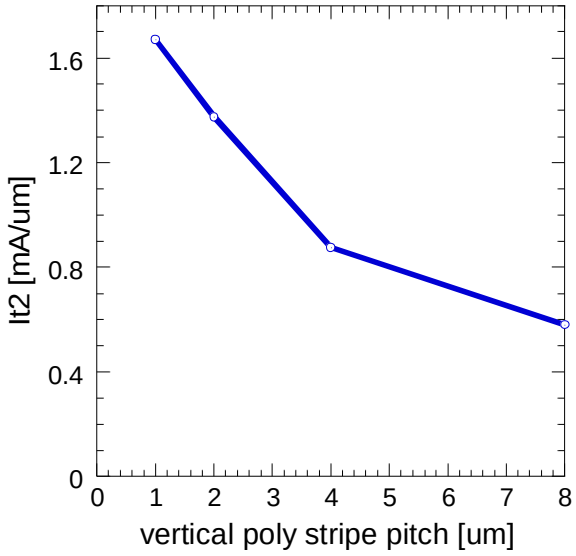

Figure 11: Normalized It2 failure current for the Body Coupled MOS device layout. The performance is higher for the minimum pitch.

GOX1 ggNMOS W = 480um	It2/perimeter [mA/um]	It2/area [mA/um^2]
Silicide blocked gate not silicided DCGS = 1um Lg = 0.1um	3.5	1.6
Silicide blocked gate silicided DCGS = 1um Lg = 0.1um	2.0	1.0
Larger gate length Fully silicided Lg = 0.25um	1.8	2.4
Body Coupled-MOS / poly stripes - 1 um pitch	1.6	**3.0**
Body Coupled-MOS / poly stripes – 1 um pitch AND silicide blocked drain junction (gate not silicided)	2.7	2.0

Table 2: Overview of ESD performance for the GOX1 NMOS transistors in the 90nm SOI technology. The new layout drastically enhances the ESD performance per area

When both approaches (BC and silicide blocked junctions) are combined, the performance per perimeter is improved due to the micro-ballasting effect of the silicide blocked junctions. However, the performance per area is slightly lower due to the strongly increased area. In the case of the silicide blocked version of the Body Coupled NMOS device, the influence of the pitch is much less pronounced.

Conclusions

Minimum size, fully silicided multi-finger MOS transistors in SOI technology exhibit a low ESD failure current in part due to the lack of body coupling necessary for uniform conduction.

The paper presents experimental data on a proprietary (i.e. non-foundry), advanced 90nm SOI technology and compares different layout methods such as silicided blocked junctions and gate length variations to improve the ESD robustness of NMOS structures.

A novel layout concept is introduced that enhances the uniform triggering by restoring the body coupling. The concept transforms the weak fully silicided transistors into robust devices without the need for the silicide block mask and without an increase of the area required for the fully silicided drivers. By connecting the body regions, the body potential of the triggered fingers can speed up triggering of adjacent un triggered fingers.

The Body Coupled MOS has been shown to have the highest ESD performance normalized per area.

Acknowledgement

The authors acknowledge the financial support of the Flemish Government through IWT030029 for research on ESD protection for advanced CMOS SOI technologies in the frame of the Medea+ T206 project. Technical support and suggestions for improvement from the mentor Christian Russ are very much appreciated.

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Notes

Version

May 2011

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