Conference paper

ESD Design Challenges in nano-CMOS SoC Design

SoC conference 2008

SARNOFF EUROPE ESD DESIGN SOLUTIONS

ESD Design Challenges in nano-CMOS SoC Design

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Savant Company Inc.
The 6th International System-on-Chip (SoC) Conference, Exhibit, and Workshops
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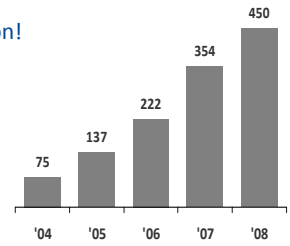
Sarnoff Europe ESD design solutions

- On-chip ESD solutions
  - **Enable customers to integrate product proven ESD solutions in their ICs**
    - Faster time to market
    - Lower R&D/IP risk and expense
- Track record in 8 CMOS generations, BiCMOS and BCD
  - Since 2007: 32 ICs released in 65nm CMOS
  - July 2008: 40nm ESD solutions validated in silicon!
  - IDM, Fabless customers and foundry partners
    - TSMC DCA partner, UMC IP Alliance partner
    - Toshiba, SONY, Infineon, Altera, PMC, Gennum, Actel, THine, AMIS, RedMere, ON…



Purpose of this presentation

- Highlight **ESD threats** in advanced SoC's in 45 and beyond
  - IO and core protection is not enough
  - Case studies: Core failures during ESD testing found
- Provide **clarification**
  - Failures at interfaces between functional blocks
  - Overview of dangerous situations
- Propose **solutions**
  - Silicon and product proven approach

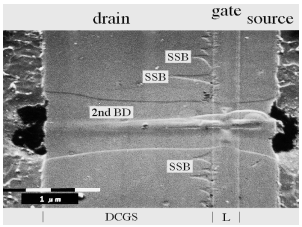
Outline

- **Introduction**
- ESD issues in System on Chip (SoC)
- Conclusions

What is Electro Static Discharge (ESD)?

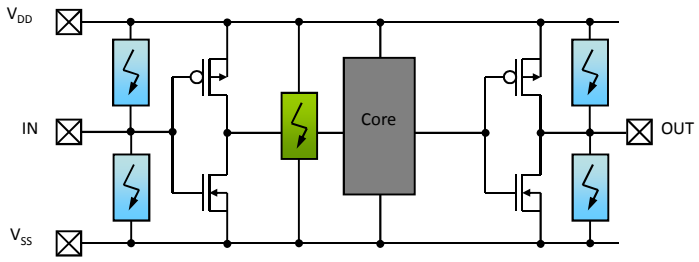
- What is Electrostatic Discharge ('ESD')?
  - The sudden discharge of a charged body
    - Short time (<1us)
    - Short rise time (<10ns)
    - High current levels (1-10A)

- **ESD damages** in integrated circuits
  - Industry quotes about ESD failures:
    - "Responsible for 20-30% of IC failures"
    - "25.8% of the products rejected"
    - "Estimated 8 to 33% of all product losses"



How to deal with ESD? – ESD protection approach

- Solution: On-chip ESD protection clamps
  - Included in IO library
  - ESD tolerant driver design (foundry guidelines)
  - **Does this solve all stress cases?**



Outline

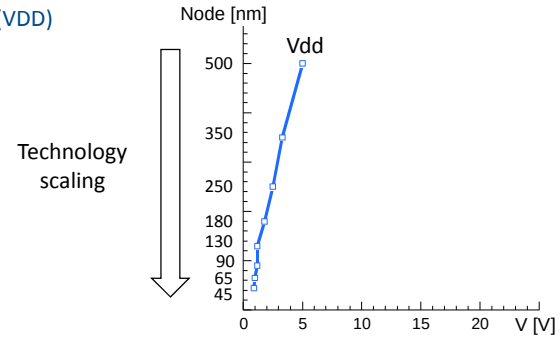
- Introduction
- **ESD issues in System on Chip (SoC)**
  - **SoC complexity**
  - **ESD in advanced CMOS**
  - Investigation of most dangerous cases
- Conclusions

System on Chip complexity – background

- System on Chip (SoC)
  - Advanced technology nodes: 65nm, 45nm
  - Multi million $ investment
    - Mask costs
    - Innovation
    - Design
    - Tools
  - High revenue based products to justify the substantial cost of investment
  - Complex architecture
    - Multiple voltage domains
    - Multiple IP blocks from various vendors
- **ESD difficulty increasing...**
  - Due to **advanced technology** and **product complexity**

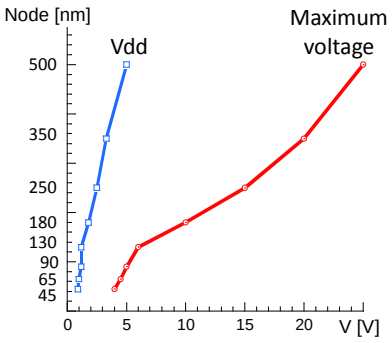
ESD Design Margin evaporates for advanced CMOS

- Decreasing solution space
  - Normal operation (VDD)
    - Slight decrease



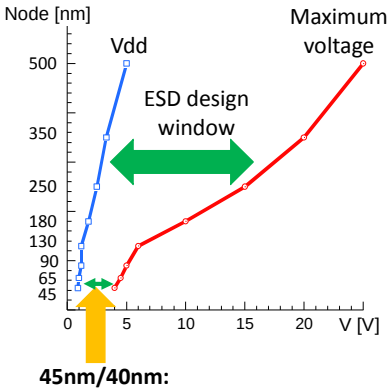
ESD Design Margin evaporates for advanced CMOS

- Decreasing solution space
  - Normal operation (VDD)
    - Slight decrease
  - Maximum voltage decreases rapidly
    - Transient breakdown of gate oxides
    - Burn-out of output drivers
    - Core failure voltage



ESD Design Margin evaporates for advanced CMOS

- Decreasing solution space
  - Normal operation (VDD)
    - Slight decrease
  - Maximum voltage decreases rapidly
    - Transient breakdown of gate oxides
    - Burn-out of output drivers
    - Core failure voltage
  - Difference = ESD design window
    - **Rapid reduction of design margins**



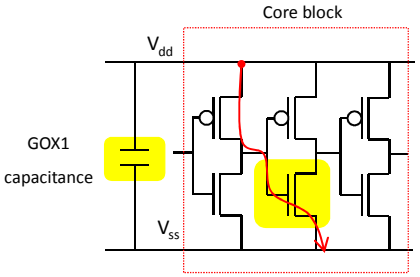
45nm/40nm:
ESD design space reduced to 3V!

Outline

- Introduction
- **ESD issues in System on Chip (SoC)**
  - SoC complexity
  - ESD in advanced CMOS
  - **Investigation of most dangerous cases**
- Conclusions

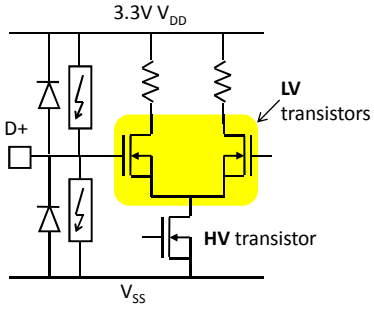
How about your ASIC circuits?

- Dangerous situations (1/4)
  - Cause: Include on-chip decoupling capacitors
    - Stabilize Vdd supply potential
    - Reduce board level components: BOM
    - Designers use GOX1 gate capacitance: highest Cap/area
  - Problem:
    - LV Core breakdown determined by sensitive thin gate oxide
    - Reduced ESD design margin
  - Solution:
    - Low voltage triggered power clamp



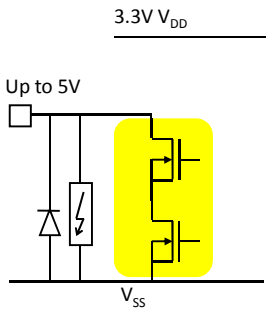
How about your ASIC circuits?

- Dangerous situations (2/4)
  - Cause:
    - Analog tricks to improve circuit speed
    - Include core transistors in 3.3V domain
    - Designers use GOX1 transistor for speed reasons
    - Designers do not use ESD foundry rules
  - Problem:
    - HV Core breakdown determined by sensitive thin gate transistor
    - Reduced ESD design margin
  - Solution:
    - Low voltage triggered power clamp for High Voltage domain



How about your ASIC circuits?

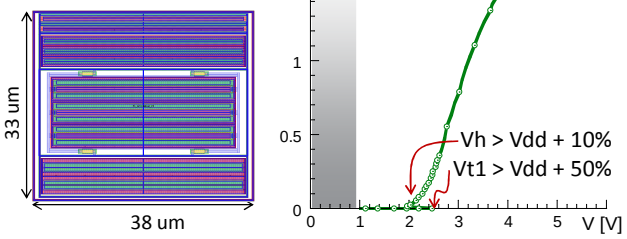
- Dangerous situations (3/4)
  - Cause:
    - Cascode configurations
    - Increase signal voltage tolerance (5V tolerant)
    - Designers do not use ESD foundry rules
  - Problem:
    - Unballasted cascode design ESD sensitive
    - Reduced ESD design margin
  - Solution:
    - Improved cascode layout
    - Local (IO) protection approach



How about your ASIC circuits?

- Issues 1-3
  - Reduced ESD design margins
  - Example solution
    - 40nm CMOS – 0.9V domain
    - 3.6kV HBM
    - 245V MM
    - < 100pA leakage

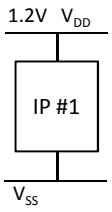
40nm 0.9V power clamp example



SoC's add another level of complexity

- SoC's main ESD problem?
  - IP block 1: Within specs
    - Fully qualified for ESD protection
    - Silicon proven, product proven

IP#1 alone
>2kV HBM,
>500V CDM



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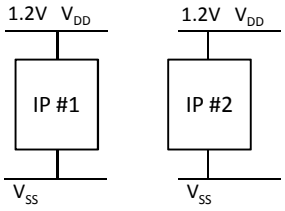
SoC's add another level of complexity

- SoC's main ESD problem?
  - IP block 1: Within specs
    - Fully qualified for ESD protection
    - Silicon proven, product proven
  - IP block 2: Above specs
    - Fully qualified for ESD protection
    - Silicon proven, product proven

IP#1 alone
>2kV HBM,
>500V CDM

IP#2 alone
>4kV HBM,
>1000V CDM



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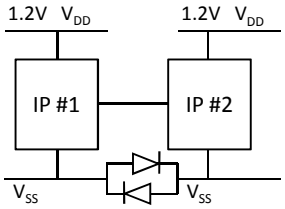
SoC's add another level of complexity

- SoC's main ESD problem?
  - IP block 1: Within specs
    - Fully qualified for ESD protection
    - Silicon proven, product proven
  - IP block 2: Above specs
    - Fully qualified for ESD protection
    - Silicon proven, product proven
  - Wired together in SoC: Below spec
    - Functionality: OK
    - ESD qualification: **below spec!**
    - **Which IP provider is responsible?**

Full product <1kV HBM, <100V CDM

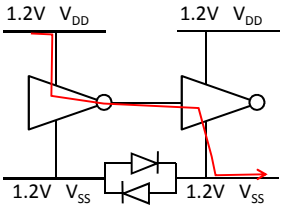
IP#1 alone >2kV HBM, >500V CDM

IP#2 alone >4kV HBM, >1000V CDM



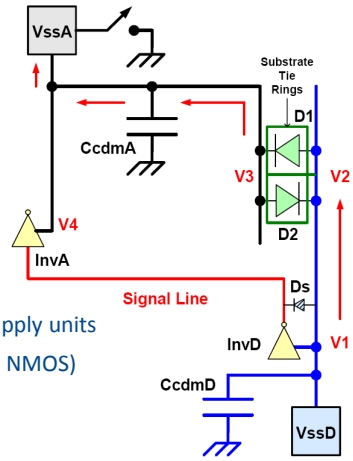
How about your ASIC circuits?

- Dangerous situations (4/4)
  - Cause:
    - Multiple functional core blocks – separately biased
    - Multiple voltage domains (Digital, Analog, IO, ...)
    - Multiple IP blocks from various vendors
  - Problem:
    - Unprotected internal / on-chip communication lines
  - Solution:
    - Ground to ground
    - Improved cascode layout
    - Local (IO) protection approach



Industry reports on this issue since 90nm node

- Worley (Conexant), 2004
  - Oxide failure at receiving circuit
    - Signal line between 2 domains
  - Different solution approaches
    - Remote blocks
    - Adjacent blocks
- Hayashi (Oki), 2004
  - ESD failure at signal line between two supply units
  - Reason: **slow** power/core protection (SB NMOS)
- Brennan (IBM), 2004



Outline

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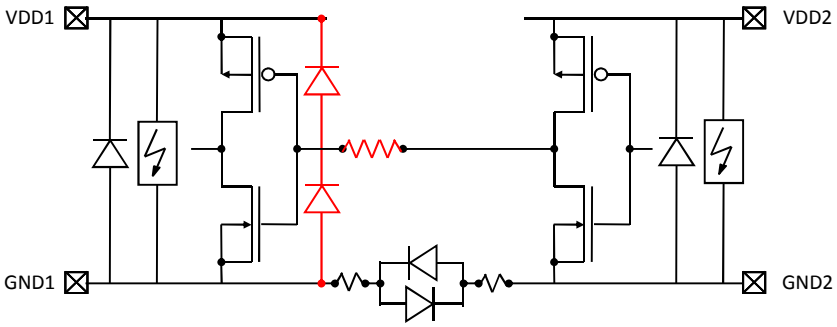
- ESD issues in System on Chip (SoC)
- **Conclusions**

Conclusions

- Growing difficulty for ESD protection
  - Advanced CMOS
  - Complex System-on-Chip designs
- Public solutions
  - Exploding silicon cost, increased risk (Industry group)
  - IO based protection not suffucient
  - Core interface circuits need specific care
- **Solutions available**
  - Treat on-chip interfaces as external interfaces for ESD
  - Include protection clamps at sensitive receiver

Simple solution to core failures?

- L. Avery (Sarnoff patent), 1996 – **Rubber band** technique
  - Multi domain core protection
  - Isolation resistance to limit the current
  - Local gate protection for most sensitive gates



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About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

Version

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