Conference paper

ESD relevant issues and solutions for overvoltage tolerant, hot swap, open drain, and failsafe interfaces

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ESD relevant issues and solutions for overvoltage tolerant, hot swap, open drain, and failsafe interfaces

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***Abstract* – The 'Dual diode' approach is one of the most used on-chip and off-chip concept for ESD protection of IO interfaces. It is simple to implement, smaller than any other IO/ESD concept, has a low parasitic capacitance and low leakage. However, especially the 'diode up', from IO-pad to V_{DD} can create a lot of problems in the functional operation of the circuits. This paper summarizes a number of problems that are caused by the 'diode up', describes the differences between overvoltage tolerant, hot swap, open drain and failsafe interface concepts and provides solutions that can solve both functional operation and ESD.**

INTRODUCTION

The 'Dual diode' approach is probably the most used on-chip and off-chip concept for ESD protection of IO interfaces. It is simple to implement, smaller than any other IO/ESD concept, has a low parasitic capacitance and low leakage. The diodes from V_{SS} to IO-pad and from IO-pad to V_{DD} shunt the ESD current to/from the power lines in the different stress modes (PS, PD, NS, ND [1]) as shown in Figure 1.

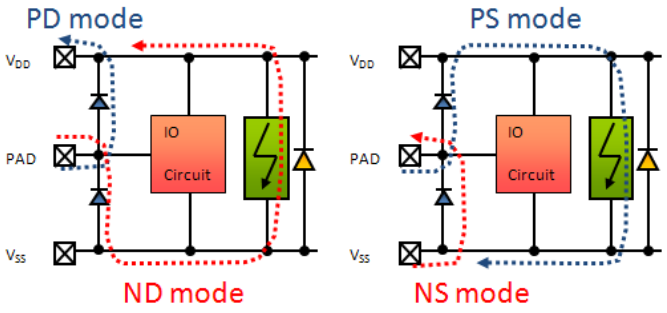

Figure 1: PS, PD, NS, and ND stress cases force current through the ESD diodes at the IOs.

The 'diode up', from IO-pad to V_{DD} can create a lot of problems in the functional operation of the circuits. The diode can strongly reduce the battery life time of a mobile application that is connected to another device that is switched off. It can limit the voltage tolerance of interfaces which reduces the compatibility between ICs. The diode can couple noise from the power supply into the IO. And it can modify the termination resistance that is used in many interface concepts.

This paper first summarizes a number of problems that are caused by the 'diode up'. Secondly, the paper describes the other ESD concepts that can be used to replace the diode to V_{DD} for overvoltage tolerant, hot swap, open drain and failsafe interface concepts. Examples are used to highlight solution concepts that can solve both functional operation and ESD.

I. DIODE UP ISSUES

The 'diode up' influences the functional operation in many ways. This section describes some functional circuit requirements that cannot tolerate a diode to V_{DD}.

A. Difference in voltage levels of ICs

In the design of electronic systems, PCB designers have to select a set of integrated circuits from various vendors that together will perform the desired function. However, the supply and signal voltage levels used by the different ICs are not always compatible. One of the reasons for the incompatibility is the fact that the voltage tolerance of the most advanced technology is much lower than the levels that were used in the past technology nodes. The supply levels have been reduced as part of the ITRS roadmap to sustain or improve on-chip reliability.

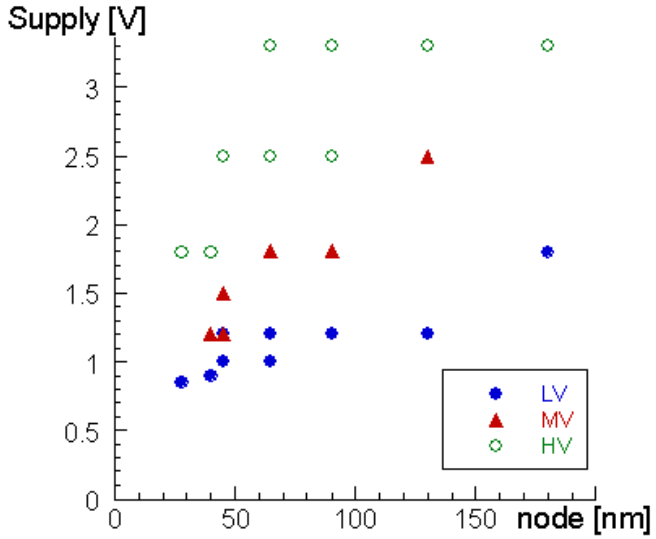

Figure 2: Supply levels for low (LV), medium (MV) and high (HV) voltage domains across process generations between 180nm and 28nm, multiple fabs, and process variations.

Figure 2 gives an overview of the used technologies and the different available power domains divided in low, medium and high voltage. The low voltage domain is decreased from 1.8V in a 0.13um technology to 1.2V for most 65nm processes and further down to 0.85V in 28nm. A similar trend is seen for the MV and HV domain.

Another view on the incompatible levels is shown on Figure 3 below [2]. It shows the logic threshold levels for

different supply voltages and device technologies. Two devices are compatible if the following requirements are met:

- The V_{OH} (Output High Voltage) of the driver must be greater than the V_{IH} (Input High Voltage) of the receiver.
- The V_{OL} (Output Low Voltage) of the driver must be less than the V_{IL} (Input Low Voltage) of the receiver.
- The output voltage from the driver must not exceed the IO voltage tolerance of the receiver.

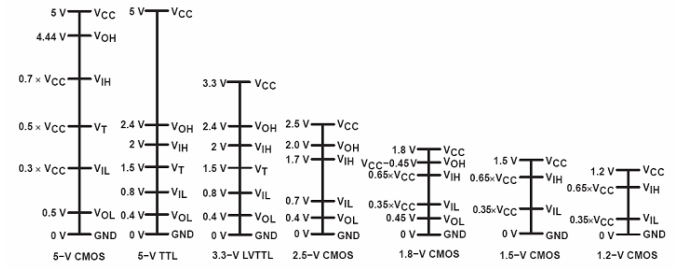

Figure 3: Logic threshold voltage levels for the different supply voltages [2].

To cope with the difference in voltage levels, designers use so-called open drain interface circuits as shown on Figure 4. If for example, the maximum voltage in the IC (V_{CCA}) is limited to 2.5V it can still communicate with 5V interfaces. An off-chip (or inside the receiving IC) resistor '$R_{pull-up}$' is connected from the open drain to the 5V supply line (V_{CCB}).

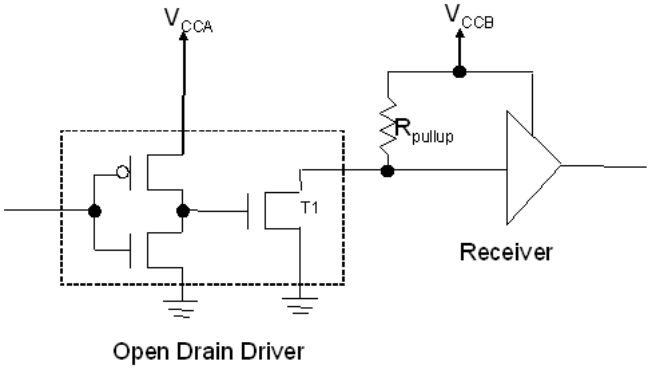

Figure 4: Schematic representation of an open drain driver. The driver consists of a NMOS only. The PMOS is omitted so the 'drain is open' [2].

If the NMOS is turned off, V_{CCB} will pull the receiver input all the way to 5V. If the NMOS is turned on it will pull down the receiver input. In this kind of application a 'diode up' from the NMOS drain to the V_{CCA} supply line is not tolerated because it would connect V_{CCA} 1 diode drop (~1V) below V_{CCB}. The open drain approach is used for many different concepts described below. Another ESD concept is required when there is a difference of signal voltage level between transmitting and receiving ICs.

B. Communication channel shared by different ICs

In many electronic systems ICs share a common communication channel or bus-line. For example the broadly used I2C bus concept [3] is simplified in Figure 5. The communicating ICs all use open drain output drivers similar to Figure 4. Suppose that all ICs connected to the bus lines are powered with the same voltage level (V_{DD}) one might believe that it is possible to use a dual diode based ESD protection concept. However, even when all the chips on the bus use the same voltage level there can still be a problem. For instance, if one of the ICs connected on the channel is powered down, to reduce power consumption, then the output drivers can be switched off (high impedance) to ensure that the communication between the remaining ICs can continue. However, if a diode is included from the output driver pad to the on-chip V_{DD} then the system V_{DD} supply will try to pull up the IC power supply through the pull-up resistance and the diode at the IO to V_{DD}.

Some IC vendors tag their ICs with the 'Failsafe' name when the IC can be shut down without influencing the shared communication line. Clearly another ESD approach must be used when pull-up resistances are shared between different ICs that may be powered down.

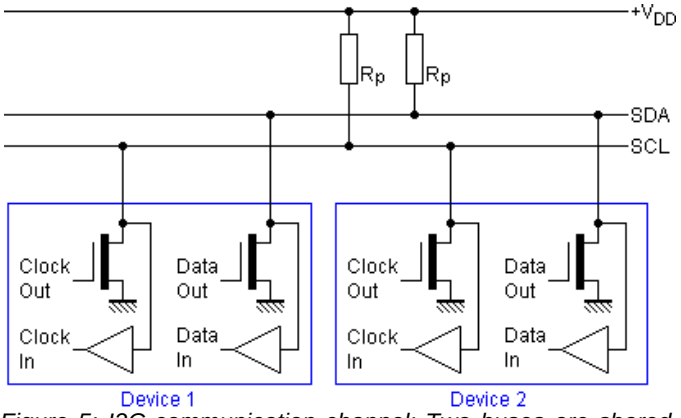

Figure 5: I2C communication channel: Two buses are shared between different ICs: SDA for data and SCL for Clock. Both buses are tied to V_{DD} through a pull-up resistance.I2C does not fix the supply level of V_{DD}

C. High speed differential interfaces

In the recent past high bandwidth communication changed from (massive) parallel to ultra fast serial communication due to growing issues with cross talk between neighbor lines in the parallel communication cables. In the differential serial communication the lines are twisted around each other to ensure a high common mode rejection ratio (CMRR). CMRR is a measure of how strong an interface can reject/filter signals that are common to both inputs.

Figure 6 shows a highly simplified schematic of a differential output/transmit stage (TX) used by several high speed serial interfaces. Despite the fact that the 'termination resistance' is now on-chip, that the supply voltage levels are the same and that there is no need to power down one part there could still be problems when dual diode based protection is used. In this kind of circuits it is not desirable to include a diode from the differential outputs to V_{DD}. The parasitic capacitance of the diodes could reduce the CMRR of the output stage. Moreover, a diode to V_{DD} would strongly influence the value and variation of the termination resistance.

Other ESD protection approaches must be used where the capacitance to V_{DD} is minimized.

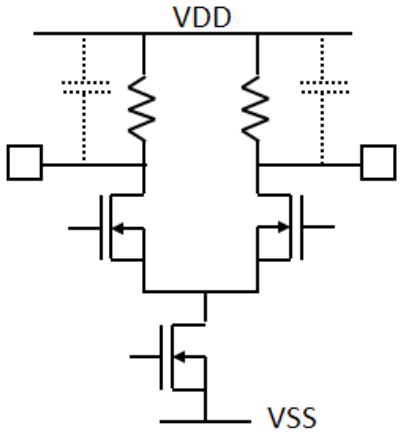

Figure 6: Simplified schematic representation of a differential output stage. Parasitic capacitance between V_{DD} and the differential interfaces can ruin the CMRR.

D. Hot swap / Hot plug

End-users of consumer electronic appliances like computers, MP3 players, digital still cameras and many other devices have the tendency to plug-n-play USB, HDMI or Firewire cables while devices are running. Suppose a user connects a USB-memory stick (powered down) to an already running computer. This could lead to voltage applied on the IOs before the memory device is up and running. Because the total (parasitic) capacitance on the IOs is many times smaller than the total capacitance of the power domain the power up rate of the supply is much slower. If a 'diode up' is placed from the IO to the V_{DD} line in the memory controller IC the computer may try to charge up the memory controller IC's supply capacitance through the IOs. Also in this case another type of ESD protection is required.

E. Back drive protection

Similar to the hot plug/hot swap issue another problem for the dual diode ESD concept is related to the combination/connection of powered and non powered devices. If a powered digital still camera is connected to a powered down LCD TV set, the camera battery may run down very quickly if the LCD set does not have 'back drive' protection. A diode to V_{DD} in the receiving circuit of the LCD panel can cause a large current flow from the camera through the data lines, through the diode to V_{DD}. Basically, with a diode up, the camera battery is 'charging up' the LCD-TV.

F. Inductive loads

In certain applications the output drivers of an IC are connected to coils or to devices with an inductive behavior. Inductive loads can be dangerous in fast switching circuits. The signal voltage can quickly increase by 100% if the transmitter changes state. Dual diode based protection is not tolerated because the IO voltage can rise quickly above the supply voltage level. The large amount of current could make the supply lines noisy. Designers include so-called 'snubber' circuits to prevent large voltage overshoots. Ideally the snubber circuit is combined with the ESD clamps.

G. Electrical Over Stress

Similar to the inductive loads the voltage on IO pins can be higher than expected during some electrical over stress situations. E.g. advanced CMOS timing circuits in LCD panels may receive a voltage as high as 17V for a long duration. In USB and HDMI applications another problem can occur. The USB/HDMI high speed data lines operate from a 3.3V supply. However there are also 5V lines in the same cable. One of the tests submitted to USB ICs is the '5V short circuit withstand' requirement. It is used to check if the USB data lines are damaged or degraded if they are shorted together with a powered VBUS line for 24 hours.

H. Summary

As described above there are many issues caused by the ESD 'diode up' from IO-pad to V_{DD}. While the end result of these issues is the same (removal of the 'diode up') it is clear that the reasons behind the removal are not identical. That has lead to a set of names that are sometimes wrongly used. It is however important to use the correct term because the optimal ESD solution depends on it.

- 'Open drain' basically depicts the fact that the typical CMOS inverter output driver is changed to a single MOS on the chip and a pull-up resistance (or pull-down in case of PMOS driver) off chip. The open drain scheme is used by many of the concepts listed below.
- 'Overvoltage tolerant' means that an IO pin can be connected to a voltage beyond the IC power supply level. In many cases an open drain scheme is used. In this case the ESD concept must be able to tolerate a voltage beyond the nominal core/IO voltage of the IC.
- 'Failsafe' is used for ICs that are connected to a communication line shared by multiple ICs. When the IC shuts down it will not influence the communication between the other ICs. Typical bus concepts like I2C describe the use of open drain schemes.
- 'Hot plug' depicts IC interfaces that can tolerate signal voltage on the IO lines well ahead of a powered supply. These interfaces can rely on open drain output drivers. The hot plug circuitry ensures that the IO lines are in high impedance state until the power supply has stabilized.

In all those cases the ESD protection approach must be changed from the typical dual diode concept. The next section provides a summary of techniques to cope with the omission of the diode to V_{DD}.

There is one other issue that is related to the use of dual diode based ESD protection. Specifically in advanced CMOS a dual diode based protection concept cannot guarantee sufficient, effective protection of thin oxide transistors. For instance in 65nm and below it is not possible to protect thin oxide transistor gate-source or drain-source [4]

III. ESD PROTECTION SOLUTIONS WITHOUT 'DIODE UP'

In the different concepts described above, the diode from IO-pad to V_{DD} has been removed to improve circuit performance. However without the diode the ESD stress current path during the combinations 'PS' and 'PD' (Figure 1) is not well defined. In the case of open drain circuits the main problem is the PS stress combination. Different solution approaches are summarized below.

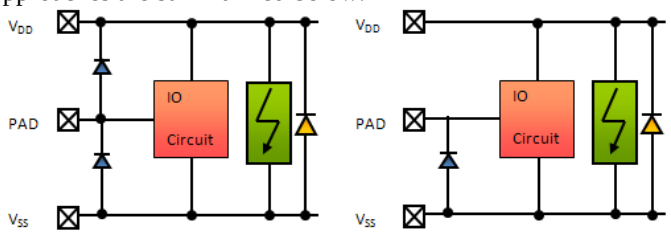

Figure 7: Normal dual diode concept (left) and single diode (right side). In this case, ESD stress from PAD to V_{DD} (PD) and PAD to V_{SS} (PS) need to be shunted through additional clamp devices.

A. Series connection of forward diodes

In most of the cases described above (Overvoltage tolerant, Failsafe, and hot plug) the diode from IO-pad to V_{DD} is not tolerated because it starts conducting current at a voltage difference of 1V. E.g. if the voltage at the IO is more than 1V above the V_{DD} level then the 'diode up' is in forward conduction causing a sort of leakage current.

The most straightforward solution is then to increase the number of diodes between IO-pad and V_{DD} (Figure 8). The number of diodes defines the voltage level at which the forward diodes start to conducts current. The drawback is the higher voltage drop during ESD stress situations. This will typically cause most problems during IO-pad to V_{SS} stress because the total voltage drop between IO-pad and V_{SS} consists of the voltage drop across the series diodes, the bus resistance and the power clamp device. Certainly in advanced CMOS technologies this poses strong constraints for the voltage drop across the power protection clamp. The area increase is rather limited. The capacitive loading between IO-pad and V_{DD} (good for CMRR) can also improve because the series diodes then act as a series connection of capacitance.

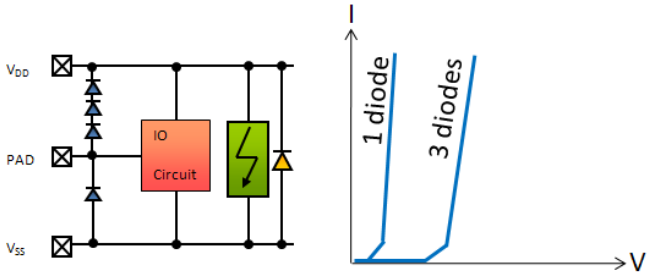

Figure 8: By connecting a number of diodes in series the 'diode up' issue can be easily solved for a number of cases. The amount of series connected diodes depends on the maximum voltage that the IO-pad can raise above the V_{DD} level.

B. ESD clamp device from IO-pad to V_{DD}

Similar to the series diodes, the ESD designer may replace the 'diode up' with a dedicated ESD clamp device as shown in Figure 9. The clamp forward conduction is from IO to V_{DD}.

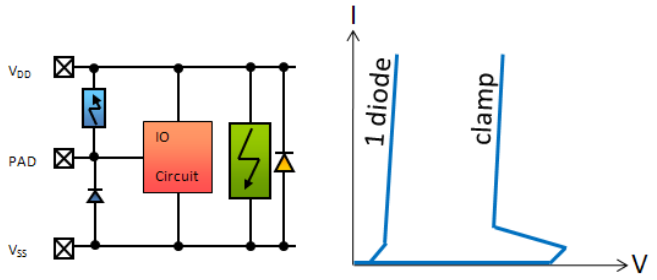

Figure 9: The single diode can be replaced by a dedicated clamp device. The series connection of diodes (Figure 8) is actually a special case of concept 'B'.

C. Use of another V_{DD} reference

Another simple approach consists of connecting the diode from IO-pad to another voltage reference as shown on Figure 10. This solution works only under certain conditions.

- The second domain (V_{DD-2}) has to run at a voltage level above the maximum signal voltage on the IO-pad and must remain powered. This is a problem for failsafe, hot swap and many overvoltage tolerant cases.
- An efficient ESD protection clamp is required between the V_{DD} and V_{DD-2} domains
- A strong back-end / metal connection for V_{DD-2} is required at the IO-pad

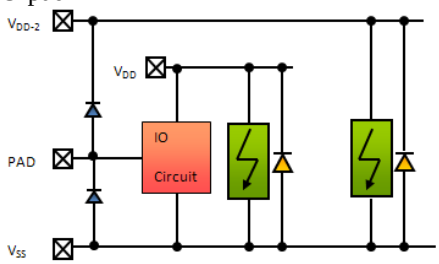

Figure 10: Connect the 'diode up' to another voltage domain. This solution only works under certain conditions

D. Use of an internal bus separate from the V_{DD} power line

Similar to case 'C' above the V_{DD-2} could be an internal 'ESD bus' only, without connecting it outside of the IC as shown in Figure 11. In this concept the first constraint can be dropped: The ESD bus does not need to be powered.

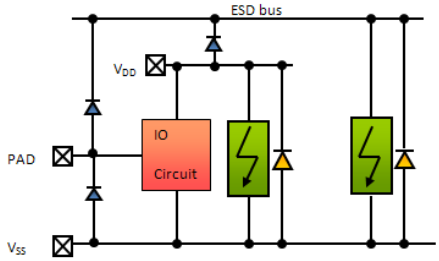

Figure 11: The 'diode up' can be connected to the ESD bus. The advantage is that the ESD bus does not need to be powered.

It is important that the ESD-bus domain does not introduce a lot of leakage current and capacitance to ensure that failsafe and hot swap concepts can be supported.

E. Selfprotective drivers

Many open drain concepts rely on selfprotective output drivers. The ESD stress current from IO-pad to V_{SS} (PS) and from IO-pad to V_{DD} (PD) runs through the NMOS output driver. There are 2 different options in this case.

- A first and most used option consists of triggering the output driver into snapback operation. The parasitic bipolar device inside the NMOS can be an area efficient clamp device if it can survive snapback operation
- A second option is to use gate and or bulk bias to turn on the MOS device into active mode during ESD stress.

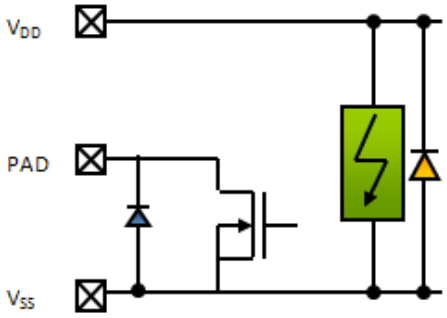

Figure 12: The selfprotective driver acts as an ESD clamp device from IO-pad to V_{SS}.

In several open drain circuits the output driver is designed as a big device to handle the large amounts of current under functional operation. It therefore feels appropriate to rely on the selfprotective concept and not waste additional silicon space to include dedicated clamp elements. However there are a number of issues that need to be considered:

- Despite the large size, many output drivers are very sensitive for ESD stress. Some drivers, especially in high voltage technology can get damaged at the edge of snapback operation. Removing silicide at the drain combined with ballasting cannot always solve that problem and further introduces even more parasitic capacitance, leakage and wastes a lot of silicon real estate.
- When the open drain application is also overvoltage tolerant the output driver must be able to tolerate a 'beyond nominal' voltage level for long durations. Cascading two or more MOS devices can solve this voltage issue. However that approach can suffer from early ESD failures because the cascaded MOS transistors tend to be more sensitive during ESD stress.

To solve the issues with early failures in output drivers, designers have come up with hybrid clamp devices where an SCR is integrated into the sensitive MOS driver. Another approach is provided below: parallel local clamps

F. Local clamp between IO-pad and V_{SS}

Selfprotective output drivers suffer from all kinds of issues as detailed above (case E). Local clamp devices can be inserted in parallel to prevent damage in the output drivers.

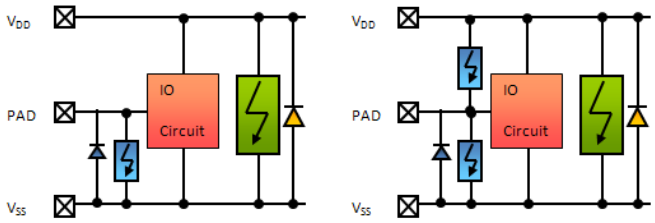

Figure 13: Local clamp protection concepts. In most cases the left version (clamp between IO-pad and V_{SS}) is sufficient. However, if there is ESD sensitive circuitry between V_{DD} and IO-pad that requires low voltage clamping then a second clamp can be added between V_{DD} and IO-pad.

On Figure 14, IV curves of several local clamp devices for the protection of open drain concepts are shown. The clamps are processed in TSMC 130nm low voltage CMOS and can be used to protect 5V tolerant interfaces. The holding voltage is around or above 5V ensuring latch-up immunity even under transient latch-up conditions.

Open drain applications are used a lot in high voltage applications. Especially in high voltage the output drivers are rather weak under ESD stress and triggering of the driver must be prevented. In a 0.25um BCD process various clamps are

Concept	Overvoltage tolerant	Failsafe	Hot swap	Leakage	Capacitance to V_{DD}	Area
Dual diode	Not OK	Not OK	Not OK	Low	100%	Small
A. Series diodes	OK	OK	OK	Low	<100%	Small
B. Clamp to V_{DD}	OK	OK	OK	Low	>100%	Larger
C. V_{DD-2} reference	Sometimes OK	Not OK	Not OK	Low	0	Small
D. ESD BUS	OK	OK	OK	Low	0	Small
E. Self protective	HVMOS or cascade needed	OK	OK	High	0	Largest
F. Local clamp to V_{SS}	OK	OK	OK	Low	0	Medium

Table 1: Summary table, comparison between the different protection concepts

developed to protect output drivers in 12V, 24V, 40V and 60V domains. Figure 15 shows the TLP IV curve of a 40V clamp that protects 40V output drivers, even when the gate is biased.

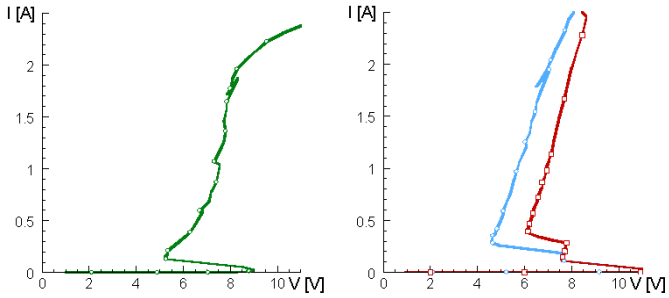

Figure 14: TLP IV curves for different hebistor clamp devices verified on a TSMC 130nm process technology. The clamps are ideally suited for protection of 5V legacy interfaces.

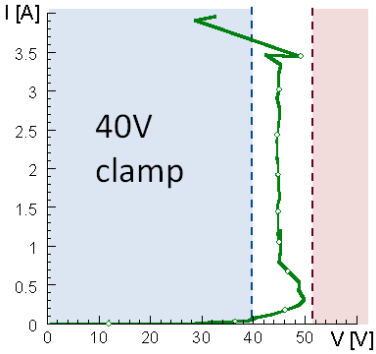

Figure 15: TLP behavior of the 40V hebistor clamp in the TSMC 0.25um BCD technology. It can protect 40V output drivers connected in parallel. The high holding voltage ensures that there is no concern about latch-up.

The presentation will provide additional examples. Table 1 briefly summarizes the different concepts and usage limitations. The most optimal concept depends on the actual requirements, maximum voltage difference between the IO and powered down V_{DD} for instance.

CONCLUSION

'Dual diode' based ESD protection is the most used concept for IO protection. It has many benefits but can also introduce a lot of problems during functional operation of the protected circuit. This paper provided examples where the 'diode up' influences the circuit performance and summarized different concepts like overvoltage tolerant, hot swap, open drain, and failsafe.

Problems are caused by communication between ICs running on a different supply voltage or through communication between multiple ICs with a bus channel that uses a shared pull-up resistance. Another set of problems are related to high speed interfaces where the CMRR and the value of the on-chip termination is strongly influenced by the diode to V_{DD}. Further, electrical communication between powered and non-powered ICs may create havoc. Also electrical over stress requirements may push IC designers away from dual diode based protection. Finally, dual diode based protection is not effective in the most advanced CMOS technology.

When the diode to V_{DD} is removed to improve functional operation another ESD device or concept is required to ensure that the circuit is well protected. Various concepts are described and compared. The most optimal concept depends on the actual requirements.

NOTE

As is the case with many published ESD design solutions, this publication contains techniques and protection solutions that are covered under patents and cannot be copied freely.

REFERENCES

[1] M.D. Ker

[2] "Secrets of level-translation revealed", Prasad Dhond, Applications Specialist, Texas Instruments, http://www.eetimes.com/electronics-news/4169927/Secrets-of-level-translation-revealed

[3] http://en.wikipedia.org/wiki/I%C2%B2C

[4] "Comprehensive ESD Protection for Flip-Chip Products in a Dual Gate Oxide 65nm CMOS Technology", J. Miller, EOS-ESD symposium 2006

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Our business models include

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  - Enable unique requirements for Latch-up, ESD, EOS
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  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
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- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

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