Conference paper

Latch-up immune ESD Protection Clamp for High Voltage optimized on TSMC BCD technology

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This paper first presents an overview of the EOS, ESD, latch-up and other requirements that IC makers face today. Secondly the TSMC BCD technology that was used as the verification platform is touched upon. Finally analysis results and on-going product implementations are shown on 0.25um BCD and 0.18um BCD technology. The unique BCD ESD solutions are available for TSMC foundry customers at a fraction of the development cost.

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***Abstract* – Applications like motor control, power management and conversion, LCD panel drivers and automotive systems require IC interfaces that can tolerate and drive high voltages (10V to 100V). Moreover, in most of these applications the ICs are operated in harsh environments (high temperature, high current/voltage transient disturbance), close to the boundaries of the IC technology. Further, to reduce the Bill of Materials (BOM) system makers are constantly shifting requirements that were once a system/PCB issue to the IC makers. IC makers designing high voltage applications need robust and reliable technology that can meet a growing set of requirements.**

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INTRODUCTION

A growing set of IC applications require a high voltage interface. Examples include power management, power conversion and automotive chips with interfaces typically between 12V and 100V. Also mobile devices like cell phones and personal navigation devices today include interfaces above 10V to e.g. control and sense MEMS gyroscopic or compass sensors. And, most LCD/OLED display technologies require driving voltages between 10 and 40V. Besides the power, MEMS and display interfaces many devices include some sort of motor like the optical zoom lens and shutter control of digital cameras or the 'silent mode' vibrator in cell phones.

Though these applications represent fast growth markets, the underlying silicon process technologies lack standardized high performance ESD solutions. The purpose of ESD protection is to provide a safe, robust current path while limiting the voltage drop below the critical voltage determined by the circuit-to-be-protected. Today, different protection clamp types are used in the industry, each with significant performance and cost burdens that prevent generic use. The main problems with traditional solutions are high leakage current, large silicon area consumption and extensive custom (trial and error) development cycles for each process/fab change.

Despite the efforts from the 'ESD council' to reduce the component level ESD performance levels there is a opposite trend to push system related ESD/latch-up requirements down to the IC design level in order to reduce system failures and improve user safety. This is mostly prevalent in automotive, industrial and consumer electronics markets. OEM makers request very robust and latch-up immune on-chip ESD protection devices. This paper introduces hebistor clamps that address these stated needs and requirements.

The paper first provides an overview of the requirements for a generic high voltage ESD device. Section II describes the TSMC technology used in the development. Section III introduces the analysis of the hebistor solution. The main benefits are summarized in the Conclusion.

I. REQUIREMENTS FOR HIGH VOLTAGE ESD CLAMPS

This section outlines the broad set of requirements for on-chip ESD protection clamps. Foremost, the ESD clamp needs to protect the chip circuitry. This can be an entire power domain (supply pin protection) or a single input, output or IO circuit (IO pin protection).

ESD protection is typically qualified using HBM, MM and CDM testers. For an in depth analysis however, Transmission Line Pulse ('TLP') testers are used to characterize the ESD relevant performance parameters of the protection clamps as shown in Figure 1.

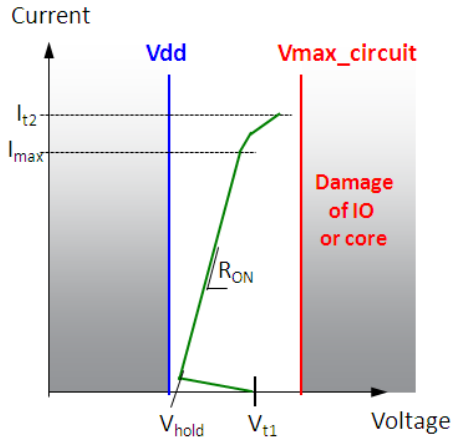


Figure 1: Generic clamp behavior based on TLP analysis. The clamp remains off until the trigger voltage 'Vt1' is reached. The clamping mode is characterized by a holding voltage 'Vh' and the on-resistance 'Ron'. The clamp failure current is called 'It2'.

While ESD devices are routinely characterized with TLP to determine the optimal design, additional analysis is required to study the time dependent behavior (turn-on, long pulse stress) and to check the influence of bias voltage on adjacent pins or power pads.

On-chip ESD protection for high voltage interfaces must fulfill many requirements. Current public solutions cannot provide a low leakage, cost-effective and latch-up immune ESD protection clamp without degradation effects that is needed for the growing set of high voltage applications. The hebistor devices discussed in Section III provide a possible solution.

II. TSMC BCD TECHNOLOGY

TSMC has a complete portfolio of process technologies and options targeted at high voltage applications like display driver ICs, power management and automotive applications. Process options include high voltage capacitors, resistors, Zener diode, and thick top metals. Ultra-High Voltage (UHV) options ranging from 500 to 800V are also available for "green technology" switching mode power supply designs. Especially the power management market is quickly growing as every electronic device needs one. The BCD platforms are good candidates for all kinds of automotive ICs, another fast growing segment.

In high voltage IC applications flexibility of the process is an important aspect. Every high voltage interface has its own set of requirements, each project is different. Therefore TSMC has defined a modular approach where IC designers can select the most appropriate modules and voltage domains. In the 0.25um BCD platform for instance designers can use different transistor modules (2.5V, 5V, 12V, 24V, 40V and 60V) and have 3 options for the core gate voltage (2.5, 5 or 12V).

Figure 2: TSMC's modular 0.25um BCD process

Sofics has verified its hebistor device concepts first on TSMC 0.35um 15V process. Next, with the help of TSMC IP and LQMP divisions Sofics has performed a full characterization on TSMC 0.25um BCD and 0.18um BCD platforms. The Sofics PowerQubic technology is currently used in the development of products on TSMC 0.35um 15V and on TSMC 0.18um BCD 18V. It is also being evaluated for automotive products in TSMC 0.25um 40V. The 40V solution passed very severe automotive requirements like a 45V load dump (ISO 7637-2) and various transient latch-up conditions.

The next section provides measurement results from ESD devices on the 0.25um BCD process. TSMC and Sofics have cooperated closely to define the ESD design windows for each transistor type. The Sofics measurement data on the hebistor clamps has been reviewed in detail by the LQMP department to ensure that the TSMC 9000 program is correctly followed.

III. HEBISTOR CLAMPS FOR ESD PROTECTION

Sofics started with a complete technology characterization including for instance an ESD relevant study of the interconnect layers, example shown on Figure 3. This data defines the minimum required metal width for every ESD current path and is used to accurately calculate the connection resistance on a full chip. Sofics also analyzed gate oxide layers and transistor devices in detail to assess the ESD design window of any custom circuit.

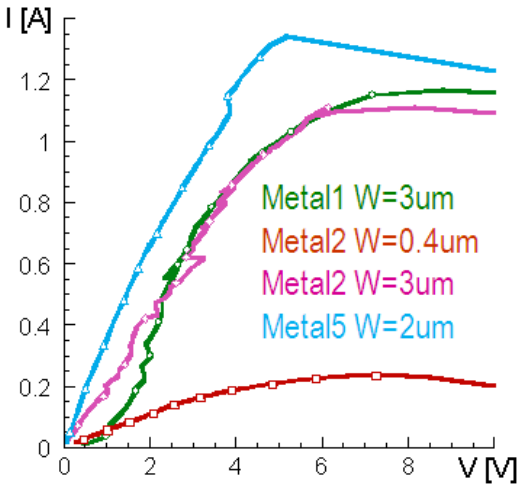


Figure 3: TLP IV curves of interconnect test structures on TSMC 0.25um BCD. The data is used to define the minimum required width for each ESD current path and allows to calculate the voltage drop of these ESD paths.

The TSMC 0.25um BCD technology allows different voltage domains to be used on the single die like 12V, 24V, 40V. Sofics has proven device concepts for all these voltage options. A subset (<5%) of the clamp measurement data is shown on Figure 4.

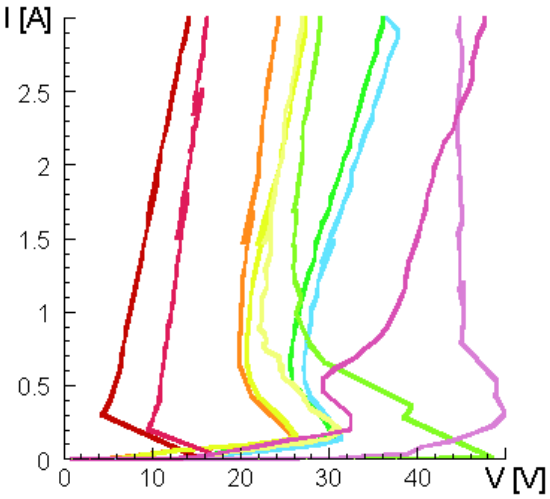


Figure 4: TLP IV curves of the hebistor clamp devices with a broad set of variation in the key behavior parameters, verified on the 0.25um BCD technology. A transient trigger effect to reduce the trigger voltage under ESD conditions is visible on some curves that is not present under DC conditions.

Similar like the TSMC 0.25um BCD platform, Sofics' hebistor clamps are designed to be extremely flexible. The key behavioral parameters like trigger voltage, holding voltage and failure current can be set independently from each other as graphically shown on Figure 5. Two separate control circuits are used for the holding ('Vh') and trigger ('Vt1') voltage. The size of the clamp body determines the failure current ('It2'). All variations are based on layout changes only, there is no process tuning involved.

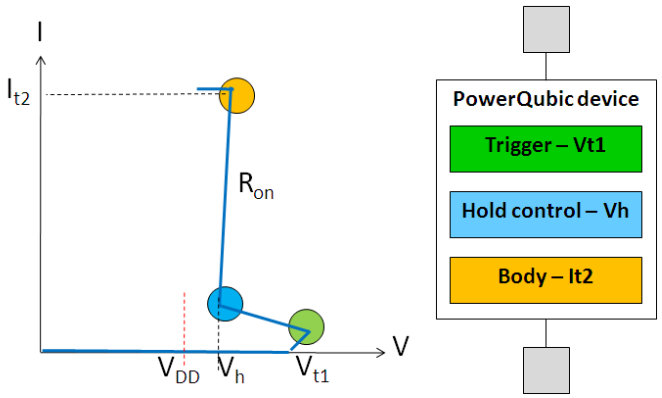


Figure 5: Generic overview of the Sofics hebistor device: thanks to separate control circuits for the trigger and holding voltage the key parameters can be set independently.

For instance, the trigger voltage 'Vt1' can be set to meet specific requirements. Some high voltage interfaces operating at 20V for instance require a trigger voltage above 40V. This trigger voltage tuning is obtained through the connection of external (separate from the clamp body) and interchangeable trigger circuits. The trigger circuits are based on well known basic building blocks available in the process technology like forward diodes, Zener diodes, MOS transistors, RC timing filters or combinations of these elements. A histogram of the trigger voltage options measured on the latest 0.25um BCD test chip is shown in Figure 6.

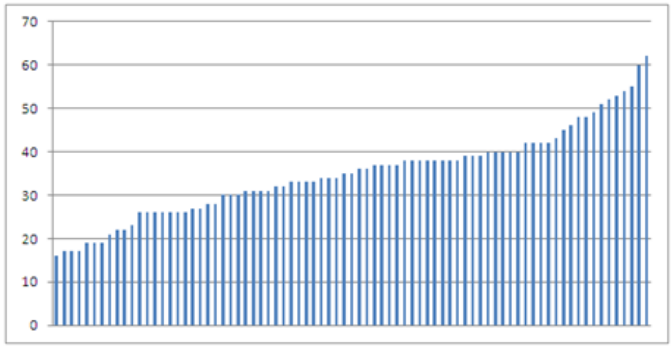


Figure 6: Histogram of TLP, transient Vt1 trigger voltage for the hebistor devices measured on the 0.25um BCD technology. The value of the trigger voltage under DC conditions can be different/higher. Clearly, a broad set of trigger voltage requirements can be supported.

Secondly, the holding voltage of the hebistor clamps can be defined by layout changes in the holding circuit. Sofics has created a family of 5 hebistor device types each with another intrinsic holding voltage. The holding voltage can then be further optimized through layout adaptations in the holding circuit and by stacking different elements. Figure 7 shows an example of a simple variation in the holding circuit. On the figure, 3 hebistor devices are compared. The clamp body and the trigger circuit is the same for all devices. The only difference is the value of a resistor in the holding circuit.

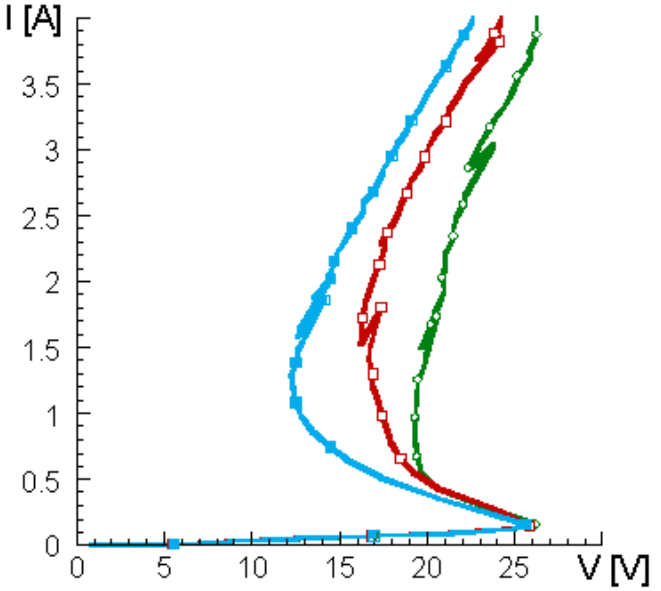


Figure 7: 3 variations based on a single hebistor type. The clamp body and trigger circuit are kept the same. The only difference between the 3 devices is the value of resistor which is changed between 20 and 200 Ohm. This simple layout change has an effect on the holding voltage. In this way it is easy to optimize the device behavior for variations in the latch-up requirements.

Similarly as in the case with the trigger voltage a histogram is created to summarize the different holding voltage options verified on the ESD test chip – see Figure 8.

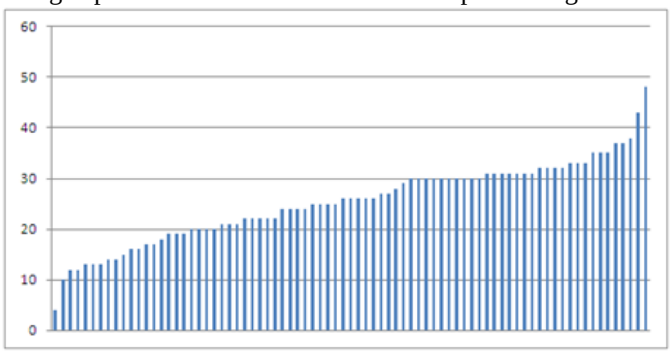
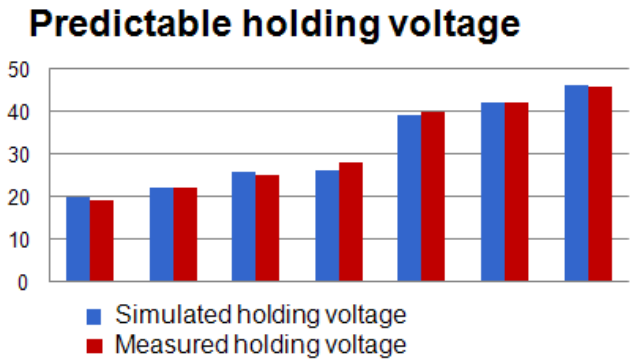


Figure 8: Histogram of TLP holding voltage 'Vh' variations measured on the 0.25um BCD platform. A broad set of applications can be protected based on this flexible device concept.

The hebistor technology allows customizing the clamping behavior. With a limited set of process characterization data it is possible to determine the holding voltage of customized clamp devices. The table/figure 9 below shows that the difference between the simulated and measured holding voltage is smaller than 6%



Before test chip simulated Vh [V]	After test chip Measured Vh [V]	Difference
20.1	19	6%
22.1	22	0%
25.8	25	3%
26.4	28	-6%
39	40	-3%
42.2	42	0%
46.2	46	0%

Figure 9: the figure and table shows the small difference between simulated and measured holding voltage of a set of hebistor clamps in TSMC 0.25um BCD technology. Clearly the measured holding voltage can be accurately estimated based on ESD characterization data on basic ESD devices like MOS and diode.

As explained in section I, during the development of ESD devices in high voltage technology one should use other equipment besides TLP testers to validate latch-up properties and leakage for instance. Therefore extensive waveform analysis was performed (Example on Figure 10 for a 40V clamp) to investigate the holding voltage under long duration stress. Clearly the holding voltage does not drop below the supply voltage even under longer pulse durations.

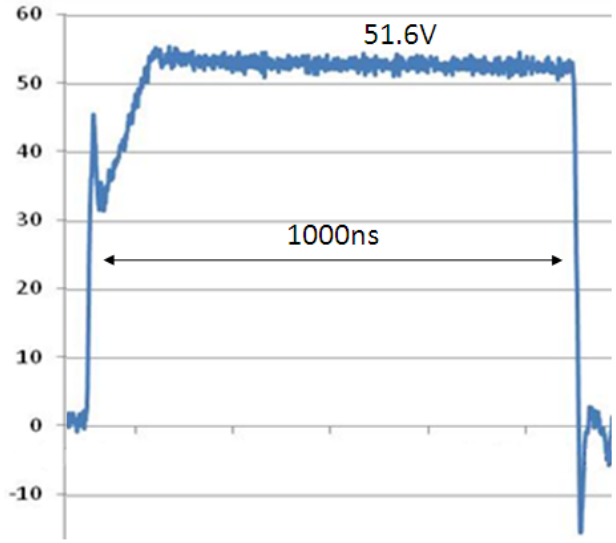


Figure 10: The voltage waveform for the 40V clamp after triggering shows that the holding voltage remains above 50V even for long pulses.

The hebistor device behavior was also checked with various transient latch-up approaches. One such test consisted of a 100ns TLP pulse of 1 ampere that is superimposed on a 50V DC bias level. Figure 11 shows the voltage and current waveforms captured during the test for the 40V reference clamp. At about 100ns from the start of the measurement, the biased (50V) device is stressed with a high amplitude (1A) TLP pulse. The current waveform shows the current flowing through the device. After the TLP pulse is over, the bias voltage restores to 50V while the current through the device is reduced to the level before the ESD stress (hebistor leakage current). The overshoot and undershoot are related to a combination of device response and test system parasitic inductance.

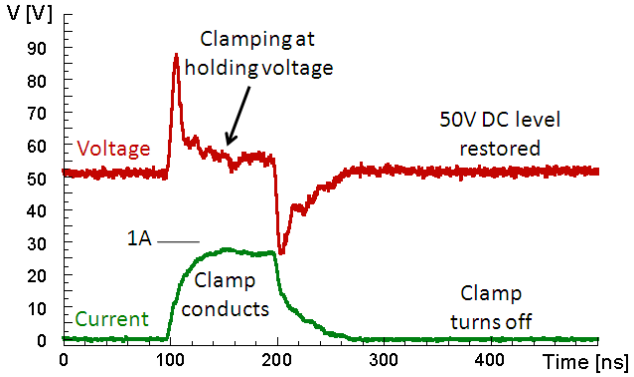


Figure 11: Transient latch-up test where a 1 ampere TLP pulse is superimposed on a 50V bias level. After the TLP pulse the voltage restores to 50V while the current through the clamp returns to the (leakage) level before the TLP pulse. The hebistor clamp does not remain latched.

The robustness level scaling to any HBM level was verified by extensive silicon testing, shown on Figure 12.

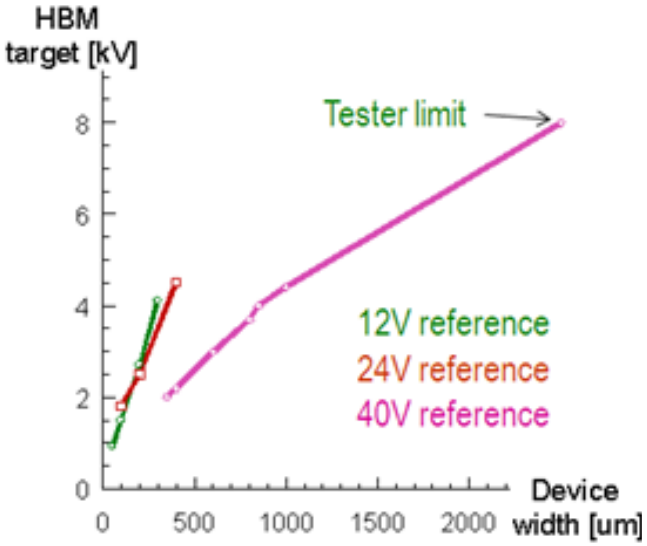


Figure 12: HBM performance for different hebistor device widths: a linear scaling is achieved for the 12V, 24 and 40V reference clamps.

To check for hidden degradation effects, the final hebistor clamps have been stressed multiple times at a level of 80% of the It2 failure current. No degradation effects were found even after 2,000 stress pulses.

IV. Hebistor clamps in advanced CMOS

The hebistor technology was developed specifically for ESD protection in high voltage and BCD processes. However, the technology can be ported to low voltage process nodes too. The high intrinsic holding voltage makes them perfect candidates for protection of 5V tolerant interfaces in advanced CMOS. The following plots provide data in 130nm and 65nm.

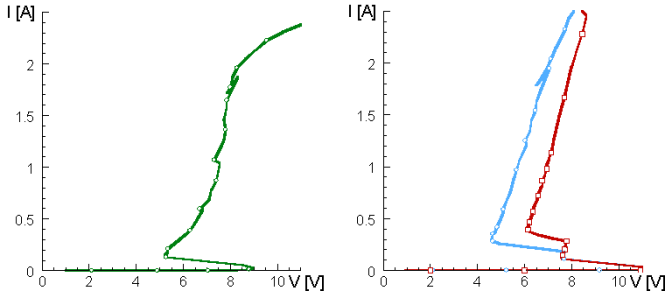
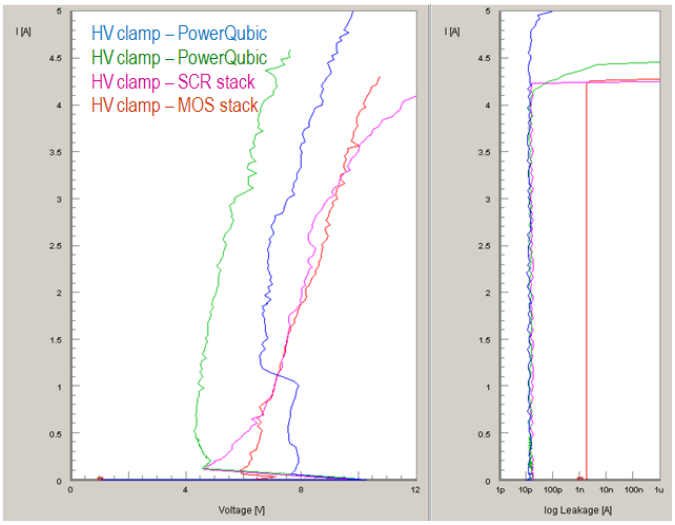


Figure 13: TLP IV curves for different hebistor clamp devices verified on a TSMC 130nm process technology. The clamps are ideally suited for protection of 5V legacy interfaces.



Device	Vt1 [V]	Vh [V]	It2 [A]	Imax [A]	Ron [Ohm]	Leakage [nA]	HBM [V]
MOS stack	7.13	5.9	4.27	3.42	1.14	<10	5600
SCR stack	9.88	4.61	4.23	3.38	1.91	<1	5600
PowerQubic	10.0	4.56	4.16	3.33	0.61	<1	5500
PowerQubic	10.3	7.6	4.8	3.84	0.386	<1	6400

Figure 14: TLP data on PowerQubic hebistor clamps verified on the TSMC 65nm LP process. The results are compared to stacked SCR's and stacked MOS devices.

V. Hebistor clamps in IC products

The Sofics PowerQubic technology is currently being evaluated for different products. This section describes a number of product implementations in various applications. The different set of requirements show the real power of the hebistor technology: it can be adapted to a broad set of requirements quite easily.

A – 13.5V interface in TSMC 0.18um BCD

For example, a developer of Ethernet systems required an on-chip ESD protection for its IC in 0.18um BCD technology. A customized clamp was prepared to protect the 13.5V interface build on 18V transistors.

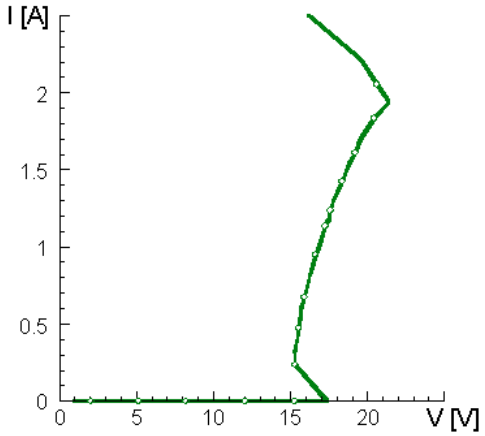


Figure 15: TLP behavior of a customized hebistor clamp implemented as ESD protection for a 13.5V line driver circuit in TSMC 0.18um BCD technology. The clamp area is smaller than 10.000 um².

To ensure the interface can tolerate all kinds of noisy signals the clamp holding voltage was set at 15V. The device TLP behavior is shown on Figure 15. The clamp, scaled for 2kV HBM is implemented on the engineering sample. Product implementation measurement results will be available at the time of presentation.

B – 40V interface for automotive application

In another example, a 40V PowerQubic clamp (Figure 16) was evaluated for an automotive product in TSMC 0.25um BCD technology. It passed severe automotive specifications including a 45V load dump pulse (ISO 7637-2 pulse type 5). Several kinds of transient latch-up conditions were applied like the measurement on Figure 11. The clamp type was further scaled up to verify the ESD performance against on-chip stress of IEC 61000-4-2. It passed 4.8kV. A 6kV version is being tested.

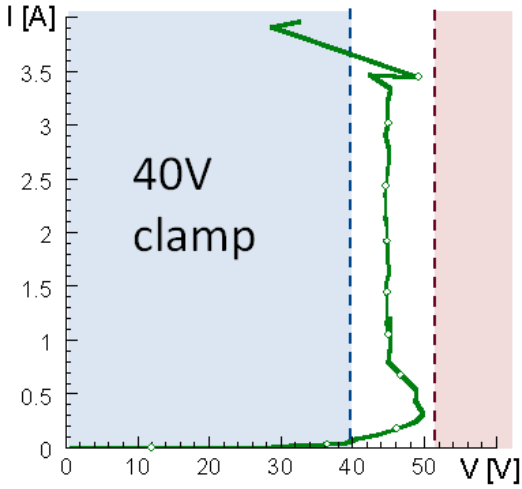


Figure 16: TLP behavior of the 40V reference clamp in the TSMC 0.25um BCD technology.

C – 12V LIN interface protection in automotive

A company designing automotive parts requested a bi-directional protection clamp for a 12V LIN interface with the following requirements

- Foundry/node: TSMC 0.25um BCD technology.
- Bi-directional protection
- Breakdown voltage under DC conditions +/- 40V
- Survive Load dump (ISO 7637-2 pulse type 5) test above 40V
- +/- 6kV IEC 61000-4-2 performance
- EMC compatibility

The LIN pin needs to pass severe EMC tests (IEC 62132 DPI) to mimic harsh conditions in the car applications. Together with the end customer EMC measurements are performed on standalone clamps to verify if the ESD clamp remains off. The measurements are performed using the setup shown in figure 17. The customized hebistor clamp performed better than the original customer clamp device.

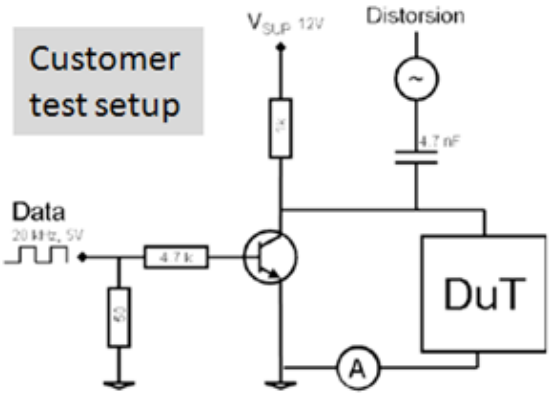


Figure 17: measurement setup to asses EMC immunity of the ESD clamp. The distortion is capacitive coupled on the 12V supply line. Voltage swings of about 10V peak to peak are coupled onto the LIN pad. The ESD structure must remain an open circuit.

The customized clamp is implemented in the LIN product. The ESD protection part of the LIN circuit is shown on the layout below (Figure 18).

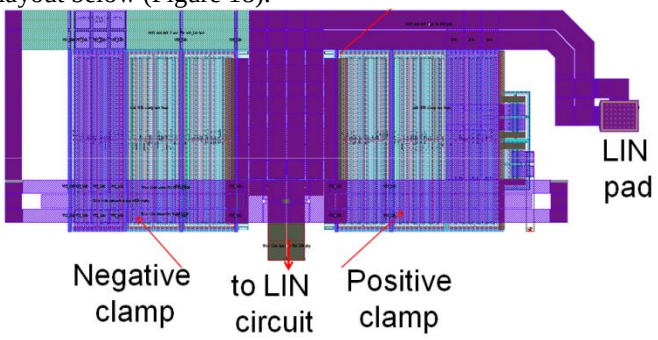


Figure 18: Layout of the ESD clamp for protection of the LIN circuit. For bi-directional protection two identical clamps are used. The reverse breakdown voltage of each clamp is high enough

D – 25V interface in TSMC 0.25um BCD

For a 25V interface a customized clamp is created with the following characteristics:

- Foundry/node: TSMC 0.25um BCD technology
- EOS/EMC requirement
  - Turn-on above 45V
  - Clamp above 25V
- ESD requirement
  - 6kV HBM
- Silicon area of 6500um² including guard bands

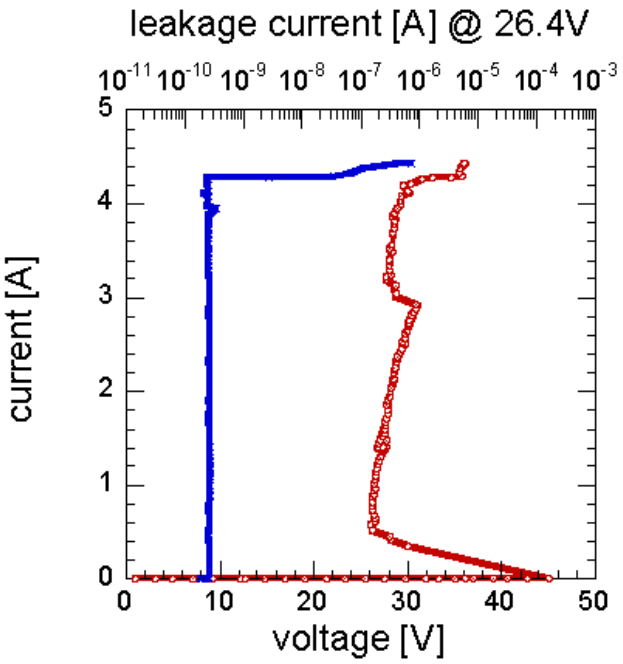


Figure 19 – IV curve of a customized clamp for a 25V interface to be used in an automotive application. The trigger voltage is increased above 45V to pass several automotive requirements.

E – 15V interface in TSMC 0.18um HV

For a solar power conversion system a customer required a protection clamp for a 15V interface in TSMC 0.18um LDMOS process. Based on data on the TSMC 0.18um BCD process several clamp candidates were developed. Fortunately the 15V interface circuit is built based on 32V transistors, providing a lot of safety margin in the ESD design window. Different versions are prepared and are being verified on a MPW shuttle. The clamp trigger voltage for the different versions is between 19V and 39V while the holding voltage is set between 19V and 26V. Together with the end customer the most appropriate clamp will be selected based on performance, trigger and clamping behavior and device size. All the clamps are scaled for 2kV HBM, 200V MM. The clamp size varies between 7500um² and 30.000um².

CONCLUSION

While high voltage interfaces are used in many IC applications like motor control, power management and conversion, LCD panel drivers and automotive systems, IC designers still lack a low leakage, cost effective and latch-up immune ESD protection clamp.

IC designers worldwide continue to produce very creative systems and applications based on HVCMOS or BCD technology nodes but the ESD protection clamps have almost not evolved: the industry is still using large area, highly leaky clamps that typically require extensive process tuning and time consuming trial and error experiments and analysis.

This paper introduced a newly developed protection device, called hebistor clamp based on extensive analysis on TSMC high voltage platforms like 0.35um 15V, 0.25um and 0.18um BCD technology. The Sofics PowerQubic technology is currently used in the development of products on TSMC 0.35um 15V and on TSMC 0.18um BCD 18V. It is also being evaluated for automotive products in TSMC 0.25um 40V. The 40V solution passed very severe automotive requirements like a 45V load dump (ISO 7637-2) and various transient latch-up conditions.

The hebistor devices are latch-up immune for the various industry standard requirements including transient latch-up, long pulse durations and high temperature conditions and are extremely flexible to allow customization for any set of requirements. The unique BCD ESD solutions are available for TSMC foundry customers at a fraction of the development cost.

NOTE

As is the case with many published ESD design solutions, this publication contains techniques and protection solutions that are covered under patents and cannot be copied freely.

About Sofics

ESD SOLUTIONS AT YOUR FINGERTIPS

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

Version

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