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Conference paper Unexpected failures due to dynamic avalanching caused by bipolar ESD stress

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The bipolar nature of ESD pulses such as MM introduces failure mechanisms that cannot be reproduced by TLP/HBM. A lowered breakdown voltage due to dynamic avalanching was observed. The key issue is that carriers injected during the first swing remain in the device after the current switches polarity. A case study for high-voltage diodes is presented.

Unexpected failures due to dynamic avalanching caused by bipolar ESD stress

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Abstract - The bipolar nature of ESD pulses such as MM introduces failure mechanisms that cannot be reproduced by TLP/HBM. A lowered breakdown voltage due to dynamic avalanching was observed. The key issue is that carriers injected during the first swing remain in the device after the current switches polarity. A case study for high-voltage diodes is presented.

I. Introduction

Transmission Line Pulsing (TLP) is an indispensable tool in analyzing ESD protection designs and making accurate predictions about their corresponding ESD robustness. Failure current (It2) measurements obtained from a 100ns TLP tester are typically used to define a technology-specific correlation factor between TLP failure current and HBM or MM failure voltage. On the other hand, for CDM, this is not so straightforward because of the very short duration of the pulse (only a few nanoseconds) and the fact that CDM is a one-pin test as opposed to the two-pin TLP set-up. Even the correlation with Very Fast TLP (VF-TLP has yet to be proven [1]. For HBM and MM it is more common to have a good correlation, although this is not always true. In the past various correlation issues between TLP and HBM have been published. A well determined and widely applicable correlation factor offers many advantages. If a linear scaling of the perimeter of a protection device gives a linear scaling in TLP failure current, such a correlation factor will also induce the same linear increase in HBM and MM failure voltage. This enables the ESD designer to reach any targeted HBM or MM specification. However, this assumption is not always valid. In some cases, the MM failure voltage is much lower than the calculated failure voltage by using the fixed HBM/MM ratio and empirical HBM test results. Furthermore the MM failure voltage doesn't scale in function of the perimeter of the device, even though HBM does. In this case, it is impossible to use one unique ratio between MM and TLP or HBM for that technology. This lower failure level is in this case only observed with MM tests and never with HBM or TLP tests.

In general there are three good reasons to justify the existence of a fixed ratio between HBM and MM. First of all, although the peak current and induced energies differ between the HBM and MM model, these can be correlated and taken into account in the correlation factor (Figure 1). Secondly, the rise time of both models is comparable. Finally, the bipolar nature of MM (this means that the current/voltage has both polarities (positive and negative) during the course of the pulse) is rather slow so that for most cases the influence of the previous positive or negative swing can be neglected, reducing the physical effects of MM to the unipolar case as HBM. All these three facts explain the theoretical validity of the fixed correlation factor used in the industry between HBM and MM.

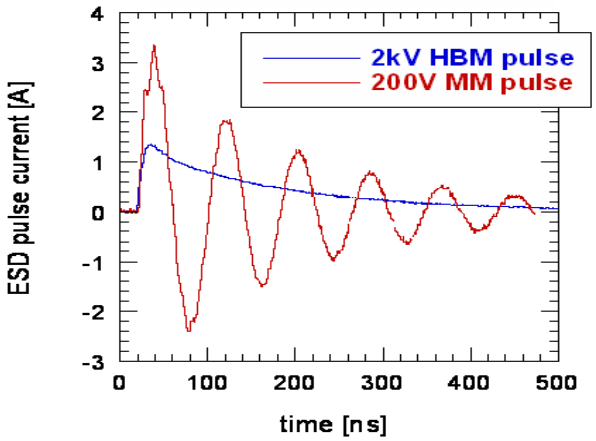

Figure 1: MM and HBM pulse, note the bipolar characteristic of the MM pulse

However, this is not always true. Important exceptions can arise, because the bipolar nature of MM will have an important influence on the behavior of the ESD circuits, which can no longer be neglected. Note that the bipolar nature of ESD pulses is not just a characteristic of a MM pulse alone, but also of other ESD models like system level (IEC tests) as presented in previous work [4] and that the phenomena described in this paper could also occur in these cases. In the following section, this paper introduces one of

the cases where we have seen the influence of the bipolar nature of an ESD pulse. Afterwards the concept of "dynamic avalanching" which causes this correlation issue will be introduced and a deeper insight in the physical background of this phenomenon will be offered. Finally, with knowing the theoretical background a solution is explained in the last section. We have found this problem only in high voltage processes.

II. Case study

One of the technologies where we have seen the problem of the bipolar nature of the MM pulse is a 0.35 um 13.5V CMOS process. The product targeted the high volume LCD driver market for big flat-screen TVs. The protection scheme of one of the outputs is shown in Figure 2. A small output driver is protected with a dual diode protection scheme and a 200 Ohm resistor connected to the drains of the driver. The diode up is formed in an NWell and the diode down in the P-substrate. The power clamp is a SGPMOS (source gated PMOS) triggered SCR (SGPSCR). This SGPSCR is optimized to prevent latch up.[3]

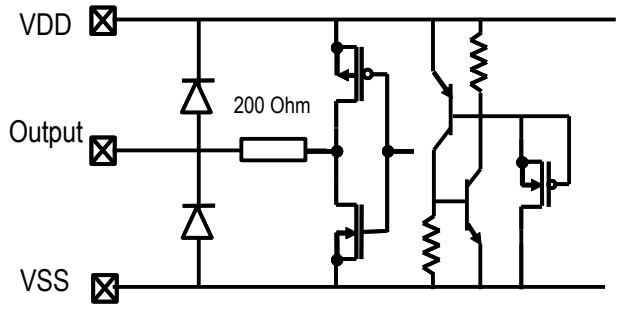

Figure 2: ESD Output protection for a 0.35 um CMOS process

All possible pin combinations reached both the 2kV HBM and 250V MM specification, except the stress case where the output pin was stressed positively with respect to the VDD power pin (Table 1). For HBM, this stress case translates into current flowing from the output pin to the power line (VDD) through the diode. The designed behavior of the ESD protection during MM can be explained as follows: during the first positive MM pulse the diode up will conduct current. When the MM pulse becomes negative the diode will be in reverse mode. As the trigger voltage of the clamp is slightly higher than the avalanche voltage of the diode, the diode will conduct some avalanching current in reverse. The voltage across the diode stays well below its failure voltage. When the trigger voltage of the clamp is reached the SGPSCR will turn on and take all the ESD current (due to the low holding voltage of SGPSCR). All the clamps are well designed to take the appropriate amount of current. The failure voltage obtained from a HBM test for this stress case equaled 5.3 kV. For this technology the experimentally extracted HBM/MM ratio is determined to be 20. This factor is minimum observed correlation factor between HBM and MM from several hundred correlation measurements over various device types processed in this technology. Therefore, the calculated MM value should at least equal 265V in this case.

HBM: 2kV	VSS-GND	IO-GND	VDD-GND
VSS-ZAP		pass	pass
IO-ZAP	pass		pass
VDD-ZAP	pass	pass	

MM: 250V	VSS-GND	IO-GND	VDD-GND
VSS-ZAP		pass	pass
IO-ZAP	pass		fail
VDD-ZAP	pass	pass	

Table 1: HBM/MM test results

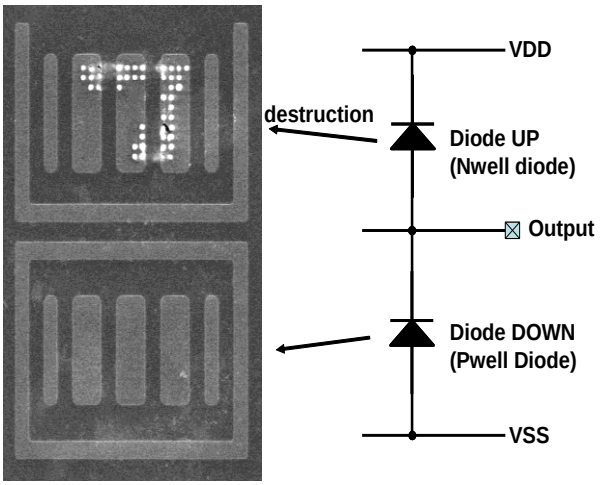

Figure 3: Failure analysis of diode up

Measurements, however, indicate a failure voltage of 150 V MM, which is significantly lower than the expected value given above. After testing, failure analysis showed that the diode up was destroyed with the worst damage occurring at the edge of the diode. (Figure 3).

The static avalanching voltage of the diode is 18V and the failure voltage 63V. The power clamp triggers at a voltage (24V – Figure 4) which is lower than the failure voltage of the diode in reverse.

Assuming the bipolar nature of MM can be neglected, this data can not explain why the diode up fails during MM. Another striking observation is that, when the same stress is applied to the PWell diode (stress between VSS and output) the results are as expected based on TLP and HBM results: no early MM failure occurs in this case.

In the domain of discrete power devices, there are some studies about a phenomenon called “dynamic avalanching”[3-9]. This effect can explain the early failure of the diode in reverse.

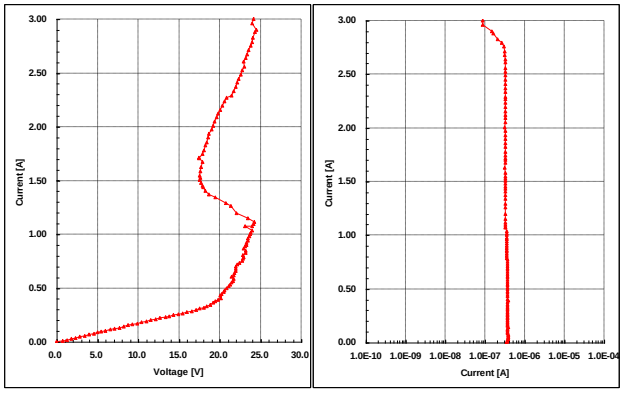

Figure 4: TLP measurement of the power clamp (in product) TLP IV curve on left side. Leakage plot on right side. The power clamp fails at a current above 2.5A. The Vt1 trigger voltage is about 24V.

III. Dynamic Avalanching

There are fundamental differences between a quasi-static current swing and a dynamic one. In some cases a MM pulse can not be considered quasi-static and then dynamic avalanching can occur (Figure 5) [3-9]. In total, three degrees of dynamic avalanching exist. Considering a simple PN-junction diode, during the first positive MM swing, the diode is in forward mode, and excess to carriers are injected into the bulk of the diode (High Injection Mode, Figure 5.1). As the current pulse switches polarity, these excess carriers will still be present in the diode bulk (Figure 5.2) with a reversed biased junction. And the carriers will even contribute in the reverse avalanching, such that the avalanching is more severe and occurs earlier in the dynamic case for the same electrical field as compared to the static case (Figure 5.3). This is called *first degree of dynamic avalanching*, which is typically non-destructive. The failure voltage of the diode is nearly the same as with static avalanching.

For higher forward bias current levels, a feedback mechanism is present that lowers the avalanche breakdown voltage: the excess carriers can be annihilated by the carriers created by the avalanching. This creates a small negative resistance regime, which is the signature of *the second degree of dynamic avalanching*. Although this causes some current filamentation, this is most often still not destructive, as it is counteracted by two other mechanisms:

- The current filamentation can rapidly and locally deplete the bulk of the diode from excess carriers, such that the cause for the dynamic avalanching locally disappears.
- With the current filamentation, a hot spot is created. The avalanche voltage increases with temperature, overcoming the negative resistance regime.

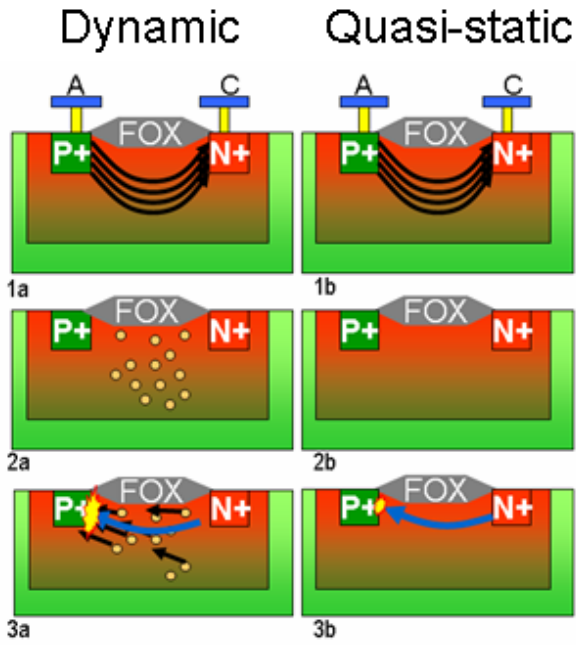

Figure 5: Schematic representation, comparing the dynamic case (1a-3a) to the static case (1b-3b) for three different moments in time (1: Strong forward bias, 2: zero bias, 3: negative bias)

Destruction is only likely when *the third degree of dynamic avalanching* is reached. The large current flow through the diode causes the formation of a strong electric field at the N+/Nwell junction. Eventually this field will reach a value high enough to cause this junction to start avalanching. The generated carriers increase the excess carriers in the bulk of the diode, thereby causing a positive feedback. The electrical field associated with this behavior is shown in Figure 6a. Instead of a linear field (dotted line), two peaks are observed at the P+/Nwell and N+/Pwell junctions. This is called an “Egawa” field. A consequence is that due to the higher fields the diode fails at a much lower voltage. Although this figure is taken for a discrete power diode, the physics are similar for CMOS technologies.

Dynamic Avalanching is one of the physical effects that show that the fundamental differences between uni-polar stress such as TLP and HBM and bipolar stress, such as MM, cannot be neglected. It makes it clear that using a unique correlation between MM and TLP is not always possible. Not only diodes are influenced by the bipolar nature of MM. Another example related to this subject is the lowering of the

trigger voltage due to carriers in the substrate of a ESD clamp device. This becomes important when the trigger voltage of a parasitic path becomes lower than this of an ESD clamp. These effects cannot be explained with uni-polar stress methods such as HBM or TLP. This is also observed in [1].

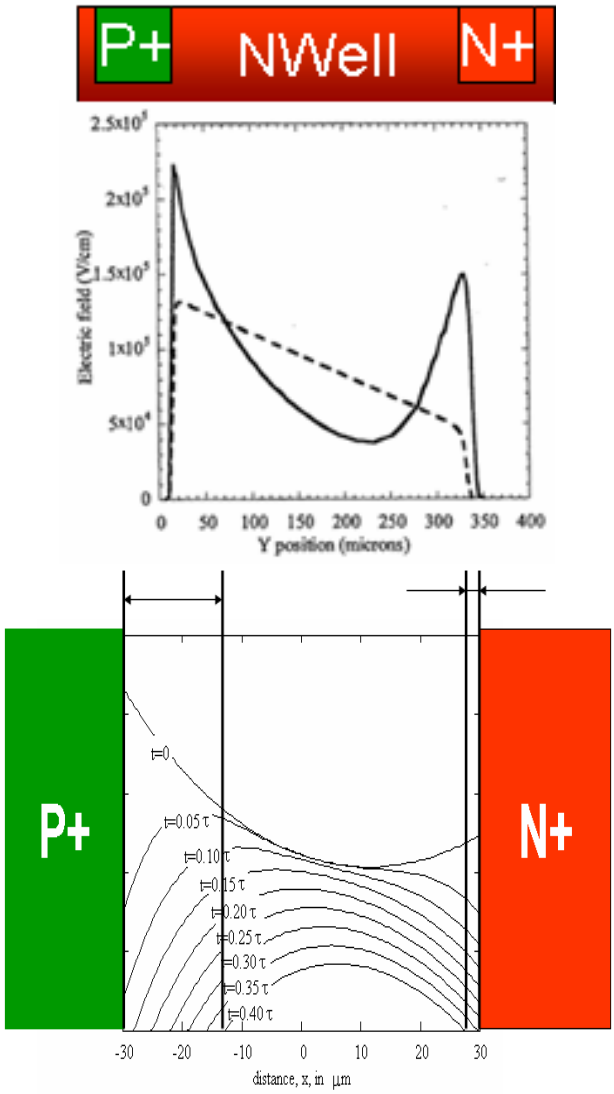

Figure 6: a)Schematic representation of the electrical field (Solid line) during the third degree of dynamic avalanching. b) Formation of the depletion regions at different times [9]

In order to have a comprehensive understanding, an additional explanation is needed for why the same failure does not occur for the diode down. The relevant stress case is now a negative MM zap between IO and Vss. Considering Figure 6.b, three regions can be designated in the diode: a depletion region at the P+/NWell and N+/NWell region and an intrinsic region between. In the depletion regions, current is handled by carriers drifting through the large electric field. The main current flow mechanism in the second region is diffusion of the carriers from the high concentration intrinsic regions towards the depleted region. It can easily be seen that the depletion region grows much faster at the P+ side than at the N+ side. This is due to the difference in diffusion coefficient between holes and electrons. At the left side the velocity is determined by the electron mobility of the electrons diffusing towards the N+/NWell junction and at the right side due to hole mobility of the holes flowing to the P+/Pwell junction. Thus, the dynamic avalanching behavior is the same for Nwell as for Pwell diodes. The electrical field however is built up over the PN junction. The voltage can change more rapidly in the depletion region than in the intrinsic region (i.e. the region with excess carriers). This gives rise to different behavior of both diode types: for the Nwell diode, the voltage built up is fast, as it is located at the rapidly growing P+/Nwell depletion region, such that the excess carriers will be swept through a large electrical field. For Pwell diodes, the voltage change is only moderately fast, because the N+/Pwell depletion region extends slower [10]. Therefore, there is more time for the excess carriers to leave the bulk of the diode, without having to go through a large electric field.

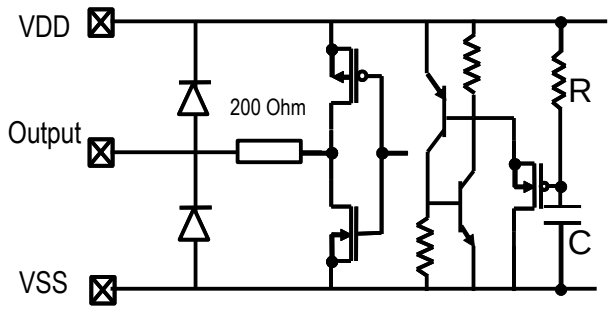

Figure 7: New protection scheme

IV. Improvements

Due to the Egawa fields the failure voltage of the diode will be much lower compared to the static case (63V). One solution to improve the results of the reflected case is to lower the trigger voltage of the power clamp. This voltage must be lower than the dynamic avalanching and failure voltage of the diode in reverse. This is solved for this product by using an RC triggering scheme connected to the gate of the PMOS of the SGPSCR. The MOS does no longer operate in bipolar mode but uses MOS current to turn on the SCR. The width of the PMOS, R and C are determined with a SPICE simulation. The lower trigger voltage of 10V gives the expected HBM and MM specifications. (Figure 7 and Figure 8).

The diode inherent in the PMOS is protected by the 200 Ohm resistor.

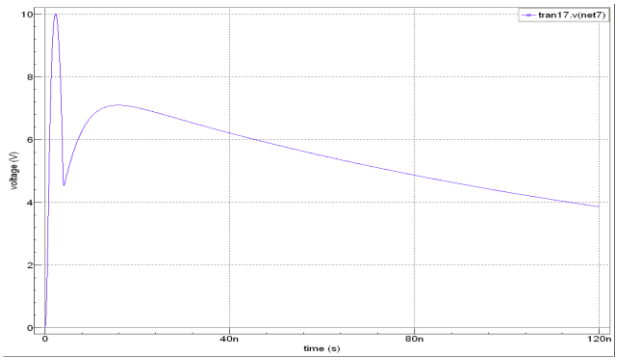

Figure 8: Simulation of the behavior of the improved clamp

V. Conclusion

It's crucial to be aware that the bipolar nature of an ESD pulse can become important in some cases and cannot always be neglected. Bipolar pulses, such as MM, cannot always be considered as a sequence of unipolar pulses. Effects as dynamic avalanching, never seen in HBM or TLP pulses, become important. Using a fixed correlation between HBM and MM can therefore sometimes result in unexpected failures in products. It is important that appropriate test set-ups are used to accurately analyze ESD protection designs in light of this phenomenon and to mitigate the risk of unexpected product failures to the MM.

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Our service and support

Our business models include

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- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

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