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# Sofics, ICsense Merge ESD and I/O Technologies, Deliver 3.3V Signalling on Icera's 40nm, 1.8V I/O Baseband Chip

## IP for World's First True 3.3V I/O from 1.8V Transistors Now Available; TSMC 28nm Version in Development

GISTEL & LEUVEN, BELGIUM (January 27, 2011) – Sofics bvba (www.sofics.com) of Gistel, a leading provider of ESD solutions for ICs, and ICsense (www.icsense.com) of Leuven, a prominent designer of analog, mixed-signal, and high-voltage ICs and turnkey ASICs, today announced that they have partnered to create the world's first integrated ESD and I/O design solution to allow a stable, fully protected I/O of 3.3V with 1.8V transistors in a TSMC 40nm process.

IP for the novel, patented design is available now. It provides a general-purpose I/O pad that can interface with legacy off-chip components and devices including SIMs and DDR and SDXC memory which are used in WIFI, GPS, and Bluetooth, and other wireless devices, and in advanced multimedia interfaces such as HDMI, USB 3.0, and SATA. A TSMC 28nm version is under development.

The technology was originally developed for the Livanto® ICE8060 baseband IC from Icera Inc. (www.icerasemi.com), the leading supplier of soft modem chipsets for smartphones, tablets and mobile broadband devices. This device is now in production.

"We wanted true 3.3V signalling on our new baseband chip without the extra cost of 2.5V/3.3V masks," said Peter Hughes, Icera Vice President of Silicon Engineering and Operations. "By integrating ESD protection with high-voltage capability, the Sofics/ICsense team gave us the ability to safely handle off-chip interfaces up to 3.6 volts with 1.8-volt internal transistors. The design worked right the first time."

According to Sofics CEO Koen Verhaege his company and ICsense worked in close collaboration to achieve these results. "Our TakeCharge® technology contributed full ESD

protection up to 4kV HBM and 300V MM while reducing the silicon footprint of the I/O pads," he said.

Bram De Muer, ICsense CEO, agreed that close collaboration between an ESD expert and an analog IC design specialist was crucial to meeting the challenge of designing the custom I/O. "ICsense used our high-voltage-in-low-voltage expertise to achieve tolerances of -0.3V to 3.9V. This allows chips to communicate reliably under a wide range of start-up and power scenarios, with robust ESD protection.

"It's a truly integrated technology, incorporating the best of both disciplines."

More information on the 1.8V/3.3V-capable general purpose digital I/O design pad is available directly from Sofics or ICsense, or by visiting the companies' web sites.

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**About Sofics**
Sofics (www.sofics.com) focuses on product development, licensing, engineering tools and design services for on-chip device- and system-level protection and reliability. Sofics is an independent IP provider, fully owned by Kogeni bvba.

**About ICsense**
ICsense (www.icsense.com) is an ISO 9001:2000 certified IC design house offering analog, mixed-signal, and high-voltage IC design services and ASIC turnkey solutions for the automotive, medical, industrial, and consumer markets. ICsense services extend from consultancy and building block design up to complete mixed-signal ASICs or SoCs.

**About Icera**
Icera is a fabless semiconductor company, pioneering software-defined modem chipsets for the fast-growing smartphone and Mobile Broadband device markets. Icera technology delivers the highest performance modem solutions with the smallest silicon die size for smartphones, tablets and USB sticks and other 'internet-everywhere' consumer electronic devices. Icera technology supports 4G (LTE), 3G (HSPA) and 2G standards. Founded in 2002, Icera is headquartered in the UK, with design locations in the UK, France, USA and China, with customer engineering and sales offices in Europe, Asia and the USA. For more information, visit the Icera web site at www.icerasemi.com.