White paper

Sofics hebistor clamps

Latch-up Immune on-chip ESD protection for High Voltage processes and applications

While high voltage interfaces are broadly used in many IC applications like motor control, power management and conversion, LCD panel drivers and automotive systems, many IC designers still lack a low leakage, cost-effective and latch-up immune ESD protection clamp that can be applied across various applications.

The behavior of many of the traditional on-chip ESD clamps is tied to the process conditions, which limits the possibilities to adapt to changing specifications. Moreover, severe reliability requirements that were long requested only for industrial and automotive applications are now being transferred to consumer electronics too.

This white paper introduces a new family of ESD/EOS/IEC protection devices, called hebistor clamps that provide competitive advantage through improved yield, reduced silicon footprint and low leakage operation. The hebistor devices are developed to protect a broad set of high voltage interfaces in BCD and high voltage CMOS and are branded under the Sofics PowerQubic portfolio. Based on measurements on TSMC 0.35um 15V and TSMC 0.25um BCD 12V, 24V, 40V and 60V technology the flexibility of the novel device is demonstrated.

Introduction

A growing set of IC applications require a high voltage interface. Examples include power management, power conversion and automotive chips with interfaces typically between 12V and 60V. Also mobile devices like cell phones and personal navigation devices today include interfaces above 10V to e.g. control and sense MEMS gyroscopic or compass sensors. Most LCD/OLED display technologies require driving voltages between 10 and 40V. Besides the power, MEMS and display interfaces many consumer appliances include some sort of motor like the optical zoom lens and shutter control of digital cameras or the 'silent mode' vibrator in cell phones.

Though these applications represent fast growth markets, the underlying silicon process technologies lack standardized high performance ESD solutions. Today, different protection clamp types are used in the industry, each with significant performance and cost burdens that prevent generic use. The main problems with traditional solutions are high leakage current, large silicon area consumption and extensive custom (trial and error) development cycles for each process/fab change. Moreover the behavior of many of the traditional concepts is strongly tied to the process conditions. This limits the ability to use the clamps for new applications or to target more severe ESD/EOS requirements.

Sofics introduces a family of hebistor clamps that addresses these needs. This white paper first discusses the requirements for on-chip ESD protection in the high voltage applications. Section II introduces the innovative solution from Sofics that meets all these requirements within a small silicon area and without the need for semiconductor process tuning. Section III describes the flexibility of this novel device concept. The last section demonstrates that the hebistor clamp types can be transferred to advanced CMOS technology for the protection of legacy interfaces like 5V compatibility in 40nm.

I. Requirements for the high voltage ESD clamps

This section outlines the broad set of requirements for on-chip ESD protection clamps.

Foremost, the ESD clamp needs to protect the chip circuitry. This can be an entire power domain (supply pin protection) or a single input, output or IO circuit (IO pin protection). While different tests like HBM, MM and CDM are used to quantify protection levels, Transmission Line Pulse ('TLP') testers are standard systems to characterize the ESD relevant performance parameters of the protection clamps.

Example TLP curves are depicted on Figure 2 (top) for a Zener diode, HV-PMOS, SCR device and a hebistor clamp device, all produced in a 0.35um 15V technology [1].

Three important conclusions can be drawn:

- The Zener, HV-PMOS and hebistor clamps all have a high enough holding voltage above VDD to ensure latch-up immune operation. The SCR holding voltage is well below Vdd which may result in latch-up problems.
- The operation regime of the Zener is above the maximum allowed voltage ('Vmax') leading to destruction of the sensitive to-be-protected circuits, hence rendering the clamp ineffective.
- The PMOS device has an ineffective operation region above 0.8 Ampere which means that the clamp size has to be increased if more than 1kV HBM (with a minimum safety margin) is required.
- SCR and hebistor clamps provide effective protection.

Figure 1 (bottom) also provides an overview of the silicon footprint for the 4 devices types scaled to an ESD protection level of 8kV HBM. Clearly, the SCR and hebistor clamp types are much smaller than the HV-PMOS and Zener based ESD protection approaches.

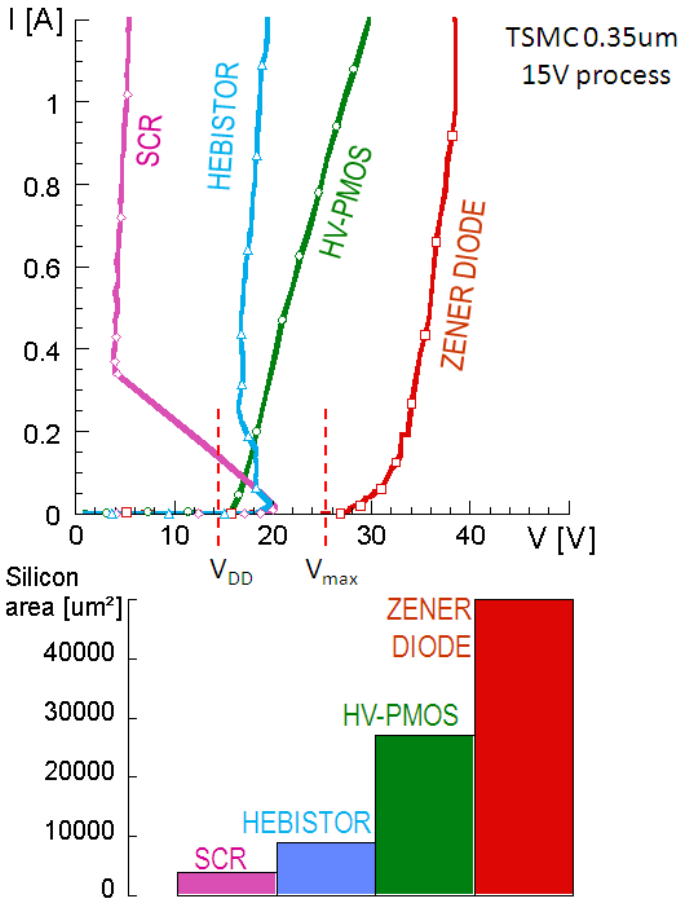

Figure 1: Transmission Line Pulse ('TLP') IV curves for 4 device types measured on 0.35um 15V CMOS technology: Zener diode, HV-PMOS, avalanche triggered SCR and the novel Hebistor. The bottom figure provides a comparison of the silicon footprint for the 4 device types designed to achieve 8kV HBM robustness.

While ESD devices are routinely characterized with TLP to determine the optimal design, there are 4 main problems with TLP measurements that are relevant for this discussion:

- The TLP characteristic is based on averaged values of voltage and current versus time waveforms, hence the TLP curve hides relevant information about the time dependent behavior [2-4].
- The TLP pulse width is typically limited to 100ns; that is enough for ESD relevant analysis but it is not relevant for EOS (electrical overstress) which has a much longer timeframe.
- TLP measurements are performed on 2 pins, leaving other pins floating. No bias is applied at Vdd so latch-up issues cannot be investigated [5].
- Most TLP systems use 50 ohm characteristic impedance, not suited for analysis of HV snapback clamps [4, 6].

Therefore, in addition to standard TLP analysis, it is important for high voltage applications to look carefully into the full waveform information and to include longer pulse durations in the evaluation. This is evident from Figure 2: the voltage versus time waveform of the Basic HV SCR shows that the device has an operating regime well above Vdd for the first 100ns (TLP time domain – highlighted by the rectangle). However the operating voltage drastically decreases below the Vdd voltage for longer pulses. This means that latch-up issues may occur when this device is used as ESD protection clamp under transient latch-up situations like some EOS and IEC 61000-4-2 stress situations. To compare, the novel hebistor device (Figure 3, right side) exhibits the desired behavior under long stress pulses. The clamping voltage stays above the supply level.

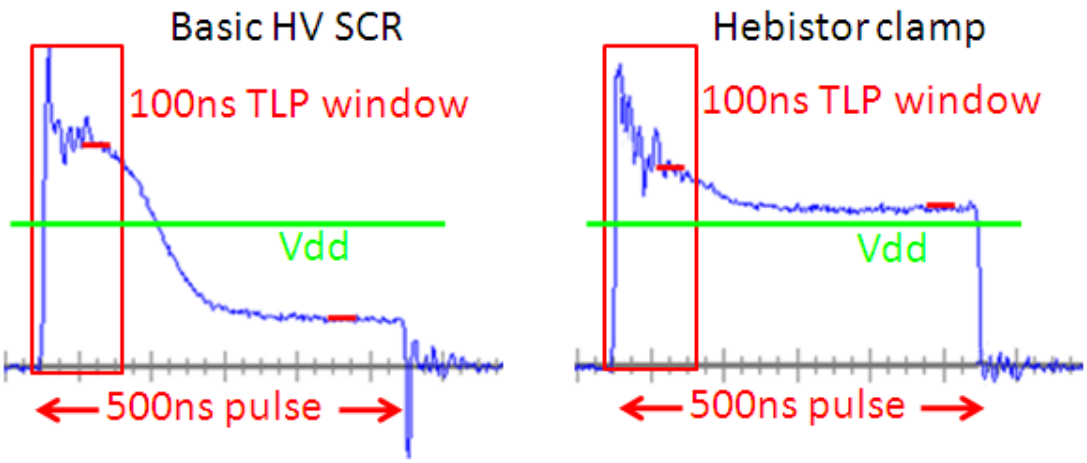

Figure 2: Voltage versus time waveform characterization of a basic high voltage SCR device (left side) and the novel hebistor clamp (right side) in 0.35um 15V CMOS. The voltage waveforms are measured with a TLP like setup with solid state pulse generators with a much longer pulse width (500ns instead of the TLP standard 100ns duration). Within the 100ns TLP window the measured holding voltage is high enough for both devices. However for the Basic HV-SCR device, the voltage drops drastically below the supply level after 250ns… which can lead to latch-up. The hebistor device on the other hand shows a voltage level above the supply voltage for the entire pulse width which ensures latch-up immunity.

Despite the improved ESD awareness and control in assembly factories and the related push for a reduction of IC level ESD performance [7, 8] components still need adequate ESD protection. Actually the OEM makers tend to increase the ESD requirements. On the various conferences speakers [9, 11] stressed that the severe system level requirements are being pushed down to IC makers. OEM and system makers want to ensure zero defects and long life time of their products during the actual use. This means that the on-chip ESD clamps must be able to tolerate higher ESD current levels, much beyond the standard 2kV HBM traditionally used. Many of the traditional concepts need considerable silicon area to cope with these new ESD constraints.

Other measurement approaches exist to verify the transient latch-up susceptibility. Professor Ker from Taiwan for instance tends to use a system depicted in figure 3 [12-14]. First a DC bias of Vdd (40V in the example) is applied to the device under test. Secondly a sharp pulse is superimposed on the DC level by connecting a charged capacitor to the biased device. Such test has many different names depending on actual conditions: Vlatch, Charged Capacitance Latch-up (CCL) [15], transient latch-up [16] or Machine Model under powered conditions. It can also be simulated with a multi-level TLP approach [17]. Due to this pulse, the ESD protection clamp will turn on to shunt the ESD current. If the clamp is latch-up immune the voltage returns to the initial DC bias level once the superimposed MM pulse is over. When performing such transient latch-up tests it is important to use a fast and low resistive power supply for the DC bias.

When such a test is applied on a HV ggNMOS device the latch-up problem is clearly demonstrated (Figure 3 bottom). After the ESD pulse, the voltage quickly drops to a low value of about 7V and remains latched at that low value until the end of the test or failure of the NMOS device.

Finally, in real world applications end-user systems can receive multiple ESD stress pulses over the product lifetime. Certainly HV-NMOS based protection devices are prone to degradation issues. The example given below (Figure 4) shows two TLP measurements of identical grounded gate HV NMOS snapback clamps in a 0.5um (43V) technology [18].
After snapback, at roughly 73V, a clear and steady degradation is visible in the leakage current. Different TLP stress step levels are used to define the real failure current level. The data shows that the final failure current (device leakage in uA order of magnitude) is dependent on the pulse density. When a small stress step is applied, the failure current is much lower.

Clearly, on-chip ESD protection for high voltage interfaces must fulfill many requirements. Current solutions cannot provide a low leakage, cost-effective and latch-up immune ESD protection clamp that is needed for the growing set of high voltage applications.

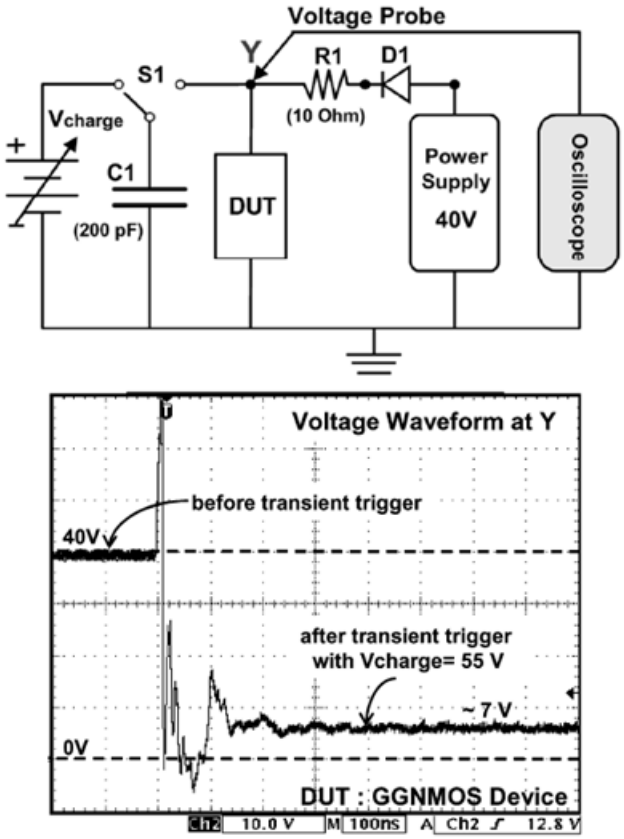

Figure 3: Transient latch-up setup described by professor Ker [12-14] (top). A charged 200pF capacitor is discharged to a biased device under test. When such a pulse is imposed on a HV-NMOS device in a 40V technology the latch-up problem is clearly visible (bottom).

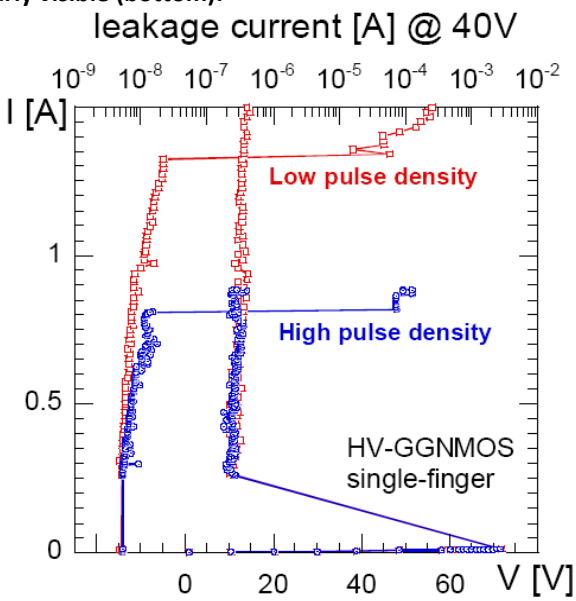

Figure 4: TLP curves on HV-NMOS devices in a 0.5um 43V process technology. The TLP stress is applied at 2 devices, once with large steps (low pulse density) and once with small steps (high pulse density). Due to the degradation effect the number of stress pulses strongly influences the failure current It2.

II. Hebistor clamps: ESD protection for high voltage applications

Sofics has developed a family of novel ESD clamps that can fulfill all requirements for protection of high voltage interfaces. This section provides measurement results from TSMC 0.35um 15V and TSMC 0.25um BCD 12V, 24V, 40V and 60V hebistor clamps that support this claim.

1. TSMC 0.35um 15V

The TLP curve for the hebistor device in 0.35um 15V CMOS is compared to the Zener diode, SCR and HVPMOS clamps on Figure 1. The measurement with long pulse duration depicted on Figure 2 (right side) shows that the holding voltage remains above the supply voltage.

Further beyond-the-standard transient latch-up stress tests demonstrate that the hebistor device is guaranteed latch-up free as shown on figure 5. Similar to the experiment outlined in figure 3 a Agilent 8110 pulse generator [19] is used to combine a DC bias level of 15V (pulse source 1) and a pulse of 5V (pulse source 2) to turn on the hebistor protection clamp. After the transient pulse is over the voltage is restored to 15V: no latch-up situation occurred.

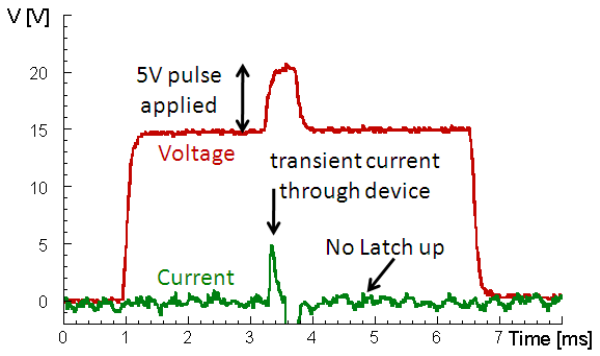

Figure 5: Voltage and current versus time for a 15V hebistor device in the 0.35um TSMC process. The device is biased at 15V prior to the transient stress pulse which turns on the hebistor. After the stress pulse the voltage returns to 15V showing no latch-up occurred.

2. TSMC 0.25um BCD 12V, 24V, 40V and 60V

The TSMC 0.25um BCD technology allows different voltage domains to be used on the single die like 12V, 24V, 40V and 60V. Results from the different domains are described below. Figure 6 provides a set of 3 curves with different holding voltage tuned for different applications.

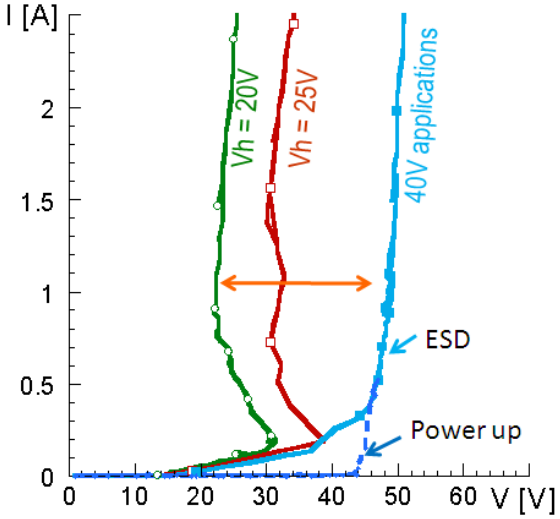

Figure 6: TLP IV curves of the hebistor clamp with different holding voltages in the 0.25um BCD technology. Holding voltage and transient trigger voltage for the 40V clamp are 44.5V. The Vt1 trigger voltage is well below the failure voltage of the circuit. A transient trigger effect to reduce the trigger voltage under ESD conditions is visible. Under DC conditions the breakdown voltage is increased above 50V as is evident from figure 7

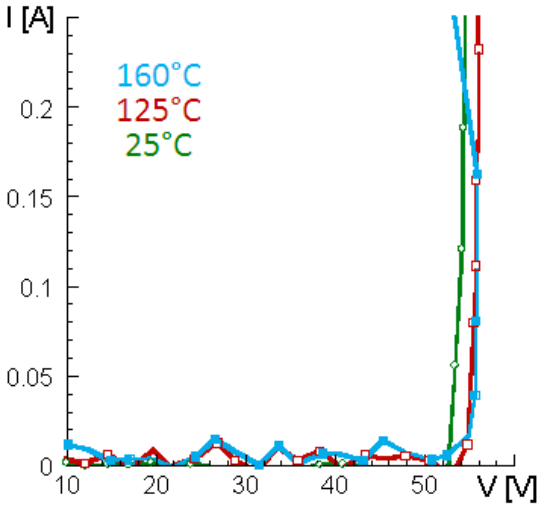

Figure 7: Under DC conditions the breakdown voltage is increased above 50V to ensure there is no problem with unwanted triggering of the device under normal operation.

The TLP IV measurements (Figure 6) of the hebistor clamp show a high holding voltage, high failure current of more than 2.5A and a very low on-resistance. Not shown on the figure is the low leakage of 50nA for the 40V clamp scaled for 4kV HBM/200V MM at 125°C. The IV curve shows a transient trigger effect to reduce the trigger voltage under fast transient conditions such as ESD stress. Under DC conditions however the breakdown voltage is increased above 50V (Figure 7).

Besides TLP IV measurements 'long pulse' waveform analysis was performed (Figure 8) to investigate the holding voltage. Clearly the holding voltage does not drop below the supply voltage even under longer pulse durations.

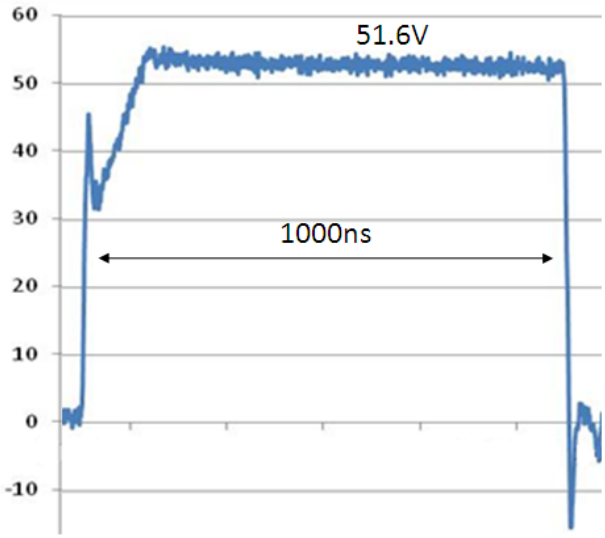

Figure 8: A voltage waveform for the 40V clamp shows that the holding voltage remains above 50V even for long pulses.

The hebistor device behavior was also checked with various transient latch-up approaches. One such test consists of a 100ns TLP pulse of 1 ampere that is superimposed on a 50V DC bias level – very similar to the approach described in Figure 3. Figure 9 shows the voltage and current waveforms captured during the test. At about 100ns from the start of the measurement, the biased (50V) device is stressed with a high amplitude (1A) TLP pulse. The current waveform shows the current flowing through the device only during the superimposed TLP pulse. After the TLP pulse is over, the bias voltage restores at 50V while the current through the device is reduced to the level before the ESD stress (hebistor leakage current). Unlike the HV-NMOS device described in the experiment from Prof. Ker (Figure 3 bottom) the hebistor does not remain latched. The overshoot and undershoot are related to a combination of device response and test system parasitic inductance.

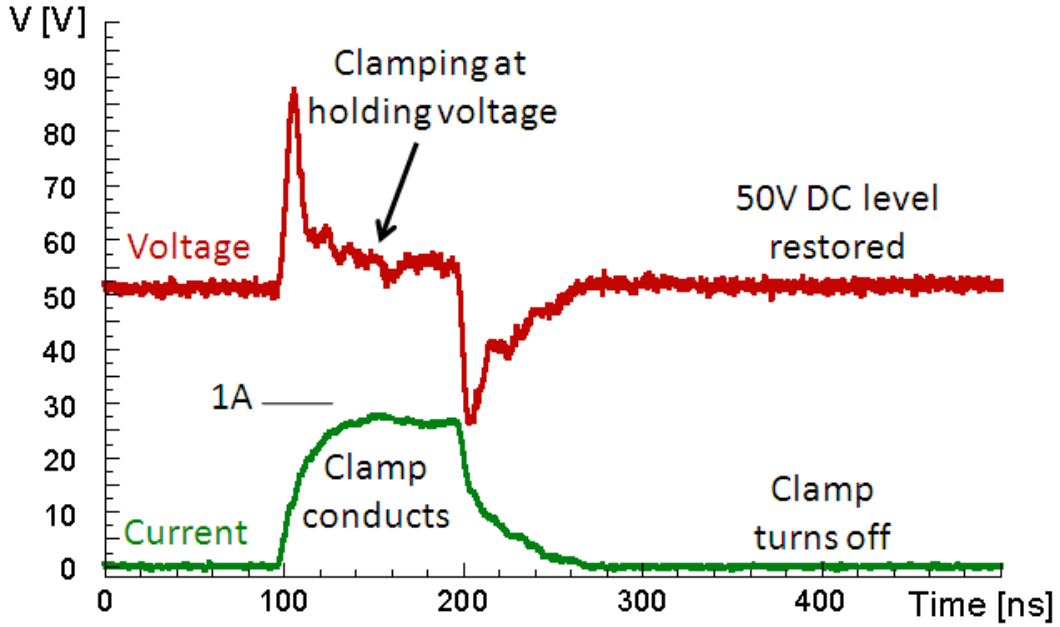

Figure 9: Transient latch-up test where a 1 ampere TLP pulse is superimposed on a 50V bias level. After the TLP pulse the voltage restores to 50V while the current through the clamp returns to the (leakage) level before the TLP pulse. The hebistor clamp does not remain latched.

Another test investigates the turn-off behavior of the hebistor clamp. Figure 10 shows the measurement setup and resulting voltage and current waveforms.

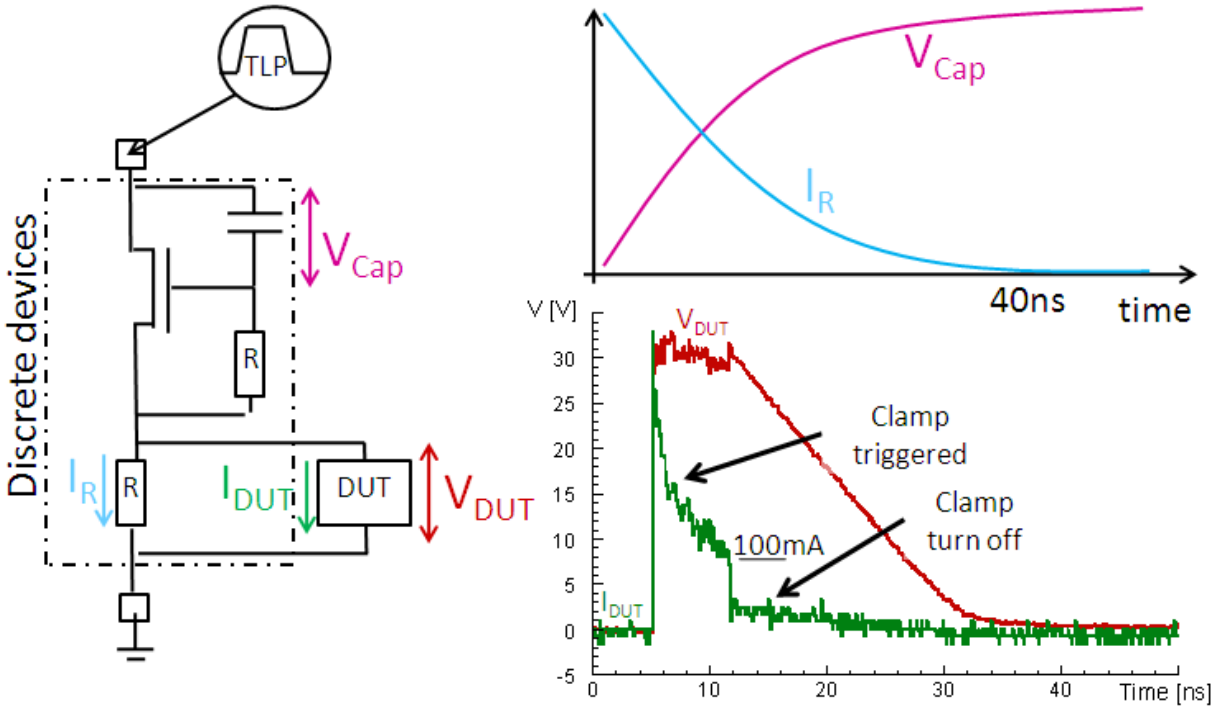

Figure 10: Measurement setup (left) to validate the turn-off behavior of the hebistor clamp. The setup stresses a discrete HV MOS device with a TLP pulse to create another pulse shape on the 'Device Under Test' (DUT) with a fast rising edge and slow falling edge. The measurement (bottom right) shows that the hebistor (30V clamp) is first triggered (fast rising edge), clamps the voltage at its holding voltage and is then turned off clearly showing the holding voltage of 30V.

To check for hidden degradation effects, the final hebistor clamps have been stressed multiple times at a level of 80% of the It2 failure current. No degradation effects were found even after 2,000 stress pulses.

The PowerQubic portfolio contains different variations such that the trigger voltage and holding voltage can be tuned. This ensures that various application types and IO circuits can be protected with the same generic approach. Further details about the holding voltage tuning are described in section III.

III. Hebistor clamp tuning

Many different variations are possible through independent tuning of the trigger voltage and holding voltage. This ensures that various application types and IO circuits can be protected with the same generic approach. Figure 11 demonstrates that the holding voltage and trigger voltage can be tuned to a broad set of values through the use of different clamp body types combined with tuning control circuits. This section provides some further examples on the tuning of the holding voltage.

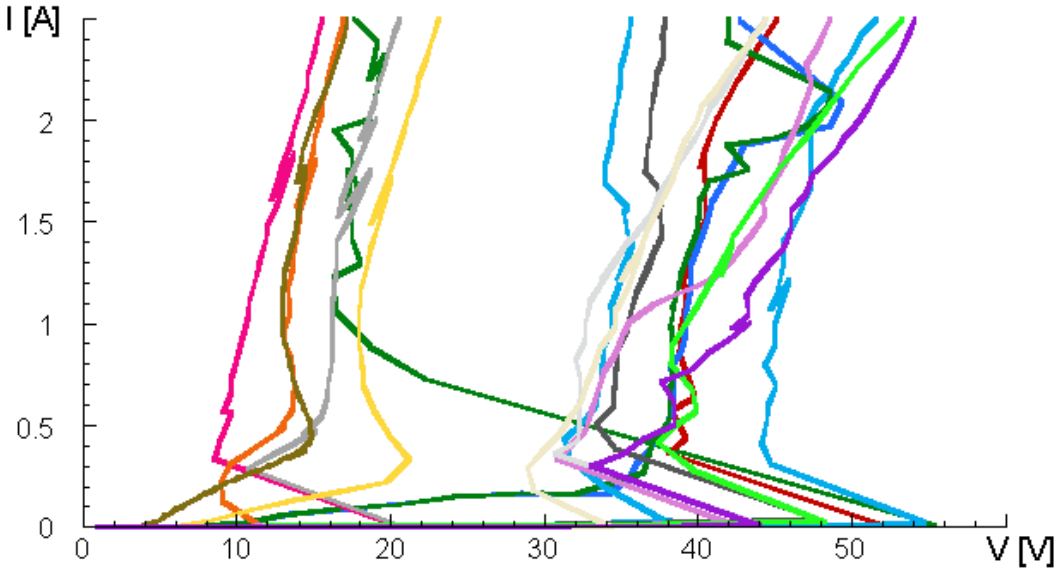

Figure 11: Overview of various hebistor clamp types in the TSMC 0.25um BCD 12V, 24V, 40V, 60V technology. The figure demonstrates that many different clamp types can be defined in the same process technology based only on layout changes. The holding voltage of each of clamp body types can be further adapted through the use of holding voltage control circuits while the trigger voltage can be easily set by an independent trigger circuit. Clearly, in this TSMC 0.25um BCD technology, a broad set of applications can be covered with the same generic approach.

The PowerQubic hebistor clamp consists of different sub-elements like the main clamp body, the separate trigger circuit and the holding circuit as depicted in Figure 12.

- Tunable trigger voltage V_{t1}
  - External trigger circuit
    - Separate and interchangeable
    - Well established TakeCharge technique
- Tunable holding voltage V_{hold}
  - Holding circuit variations
    - By layout and/or design
    - Novel approaches
- Tunable performance I_{t2}, R_{on}
  - Clamp size variation
  - Different clamp bodies

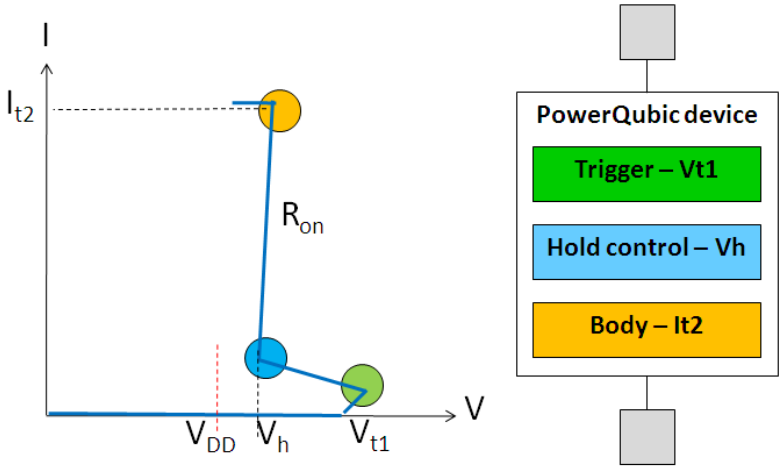

Figure 12: The flexible PowerQubic hebistor clamp consists of different sub elements. The trigger voltage, holding voltage and failure current can be set independently through the connection of separate circuits to define the trigger voltage and circuits to control the holding voltage. The failure current is set to the appropriate level by sizing the main clamp body.

1. Trigger voltage Vt1

The trigger voltage is determined by a separate trigger circuit that is external from the rest of the clamp elements. This approach allows to easily changing the trigger condition to any desired trigger condition. The trigger circuit can consist of NMOS/PMOS elements, chain of forward or reverse biased diodes, bipolar transistors, RC-timed elements or a combination of different elements. This approach is similar to the other on-chip ESD protection portfolio (TakeCharge) already in use in 10 technology generations and several hundreds of ICs.

2. Holding voltage Vh

The holding voltage can be tuned in different ways. At first the voltage is defined by the selection of the hebistor type. The PowerQubic portfolio consists of a family of device concepts, each with an intrinsic holding voltage. With holding control circuits it is possible to further fine tune the holding voltage. The following examples (Figure 13) demonstrate this flexibility. Fine tuning of the holding voltage consists of changing resistor values, number and location of diodes and scaling of sub elements within the hold-circuit.

3. ESD performance level It2

To address different ESD protection levels the clamp body can be scaled. This affects the failure current It2 and the on-resistance. Clamp variations have been proven up to 8kV HBM (test limit) and 660V MM. Figure 14 shows the linear behavior between the clamp perimeter and the HBM level for one hebistor clamp type.

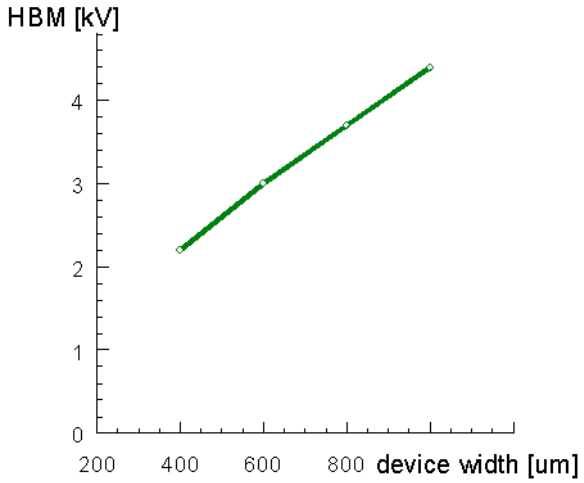

Figure 14: Scaling up of the device width increases the HBM performance level.

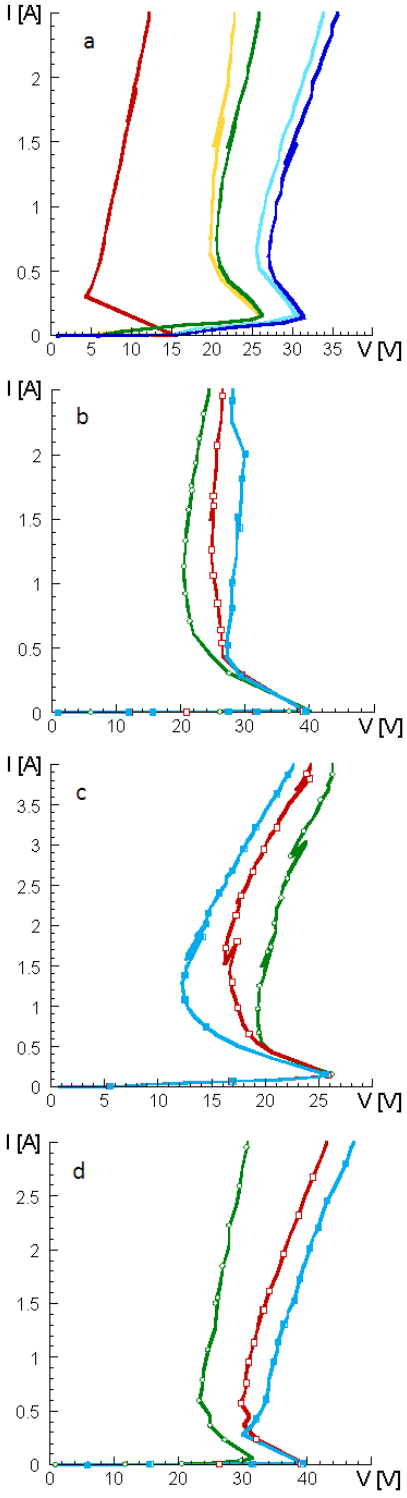

Figure 13: Examples of holding voltage tuning: (a) adding and removing diodes in the hold control circuit, (b) variation of a resistor (1…20 Ohm) inside the hold control circuit, (c) Variation of a resistor in the hold control circuit (20..100 Ohm) coupled to another hebistor clamp body and (d) size variation of one MOS element in the hold control circuit.

IV. Hebistor clamps in advanced CMOS

This white paper described the use of the hebistor clamps in high voltage (>10V) and BCD technologies. However there is a need for high voltage capable devices in advanced CMOS too. The core voltage in advanced CMOS technology has been scaled down from 3.3V (0.35um CMOS) to less than 1V (40nm CMOS). Also the typical IO voltage has been reduced from 3.3V down to 1.8V. In 40nm for instance the standard process does not include 3.3V compatibility. Various interfaces like USB, HDMI, PCI, I²C and others however still require so-called 'legacy' 3.3V or even 5V signals and supply levels. To cope with this higher voltage level, IC designers typically use a series connection of IO transistors. It takes analog design expertise to ensure that the voltage across all terminals never exceeds the maximum ratings. Such custom designed circuits are typically very weak during ESD stress which means that dedicated local ESD protection clamps are required as the 'dual diode' approach cannot be used since the signal level can be higher than the Vdd level.

To facilitate the protection of 5V tolerant or capable circuits, Sofics has successfully transferred some of the PowerQubic hebistor clamp concepts to advanced CMOS. Figure 15 demonstrates two clamp types and the holding voltage tuning capability in TSMC 130nm CMOS. As described in section III, the trigger voltage can be set independently.

Besides the trigger voltage and holding voltage also the failure current can be set easily to protect for instance 5V USB or I²C interfaces up to 8kV IEC 61000-4-2.

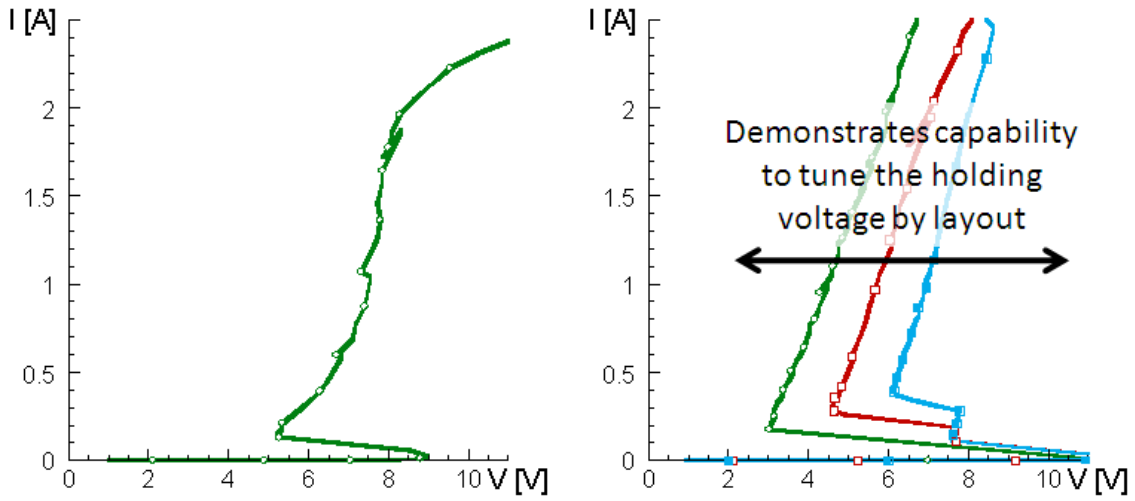

Figure 15: Two hebistor clamp types created in low voltage TSMC 130nm CMOS technology. With a holding voltage above 5V (left) the clamp can be used for IO protection of legacy interfaces. The clamp holding voltage can be tuned (right).

Conclusion

While IC designers worldwide continue to produce very creative systems and applications based on HVCMOS or BCD technology nodes the ESD protection clamps have almost not evolved: the industry is still using large area, highly leaky clamps that typically require extensive process tuning and time consuming trial and error experiments and analysis.

Time has come to change that: Sofics' PowerQubic portfolio with the novel hebistor protection clamps provides effective protection for various HV circuits like motor control, power management and conversion, LCD panel drivers and automotive systems without the disadvantages of the traditional solution types. This paper introduced the newly developed hebistor protection device based on extensive development and silicon verification on TSMC 0.35um 15V and TSMC 0.25um 12V, 24V, 40V and 60V high voltage process technology.

The PowerQubic hebistor devices are latch-up immune for the various industry standard requirements including transient latch-up, long pulse durations and high temperature conditions and are very flexible by design to address any ESD specification level and combinations of ESD/EOS/LU/functional requirements.

Sofics' hebistor clamps are already available today on TSMC 0.35um 15V, TSMC 0.25um 12V, 24V, 40V, 60V and are being ported to other foundry and proprietary technology nodes of IDM companies for the protection of power management ICs. Sofics team is highly experienced in technology transfer through which PowerQubic hebistor solutions can be customized and transferred to any proprietary (foundry or IDM) silicon process technology.

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About Sofics

ESD SOLUTIONS AT YOUR FINGERTIPS

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

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Sofics BVBA
Groendreef 31
B-9880 Aalter, Belgium
(tel) +32-9-21-68-333
(fax) +32-9-37-46-846
bd@sofics.com
RPR 0472.687.037