Data sheet

LIN PHY IP macro

Transceiver for on-chip integration

TSMC 180nm BCD gen II

The Sofics LIN PHY is an IP macro for on-chip integration. The LIN PHY targets automotive applications and is compliant with ISO 17987-4 and ISO 17987-7 standards as well as IEC 62228-2 for EMC compatibility.

It is designed in TSMC 180nm BCD Gen II, but can be ported to other technologies upon request.

LIN PHY IP for TSMC 180nm BCD gen II

The Sofics LIN PHY is an IP macro for on-chip integration. It contains the physical interface layer for the LIN protocol and the necessary provisions to interface with on-chip digital core.

A LIN transceiver has to meet several challenging electrical reliability requirements. We designed a solution that can handle all of those, within a small silicon area.

The Sofics LIN PHY targets automotive applications and is compliant with ISO 17987-4 and ISO 17987-7 standards as well as IEC 62228-2 for EMC compatibility. By default a 4kV IEC 61000-4-2 ESD protection is included, this is however scalable to other levels. This specific IP macro is designed in TSMC 180nm BCD Gen II, but can be ported to other technologies upon request.

Key features

- LIN slave
- Compliant with ISO 17987-4/ISO 17987-7/IEC 62228-2
- Temp range -40°C to 150°C TJ
- 30kΩ integrated pullup
- 300kΩ pullup for low power mode
- Integrated 4kV IEC 61000-4-2 ESD
- Programmable slope control
- 5V digital interface
- Test hardware for ATE included

Description

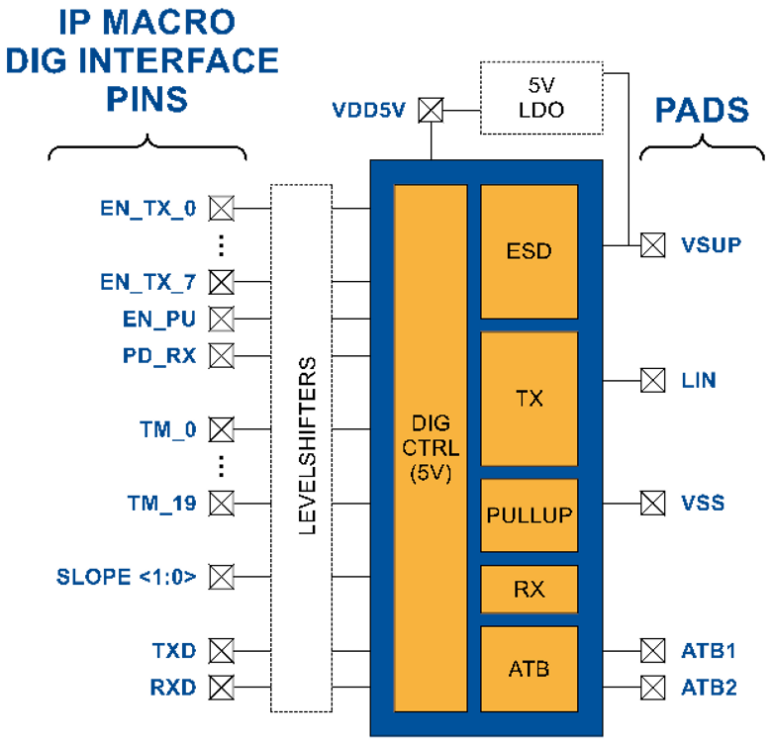
The IP includes different I/O Pads and pins to the core block.

PAD	Description
VSUP	Supply voltage (7V – 18V)
LIN	LIN bus
VSS	LIN ground pad
ATB1/2	Analog test bus 1/2

PIN	Description
EN_TX0…7	Enable pins transmitter
EN_PU	Enable pullup
PD_RX	Power down receiver
TM0…19	Test mode pins
SLOPE<1:0>	Slope selection
TXD	Transmitter data pin
RXD	Receiver data pin
VDD5V	5V supply

Block diagram

The generic digital interface has the flexibility to support different system modes (sleep, normal, customer-defined modes, …).



A feedback loop controls the slope time (slope in V/us scales with VSUP voltage).

The SLOPE<1:0> bits can be used to:

- Change typical process slope times between 8us/10us/12us
- ATE trim for on-chip RC variation of the slope time

Included blocks and additional or optional features

The LIN IP from Sofics contains the physical interface layer for the LIN protocol and the necessary provisions to interface with on-chip digital core. Special features that are “analog” of nature, like thermal shutdown, internal regulator, … can be supported upon request.

Example features available upon request:

- Level shifters digital core / 5V interface
- 5V regulator
- Other “analog” features

It is assumed that the other parts of the LIN protocol stack as well as some additional digital features like remote wakeup, sleep mode timer are implemented by the customer. This way, there is flexibility to reuse this IP in several applications.

Quick reference

Parameter	Unit	Minimum	Typical	Maximum
VSUP max rating	V	-0.3		40
LIN max rating	V	-27		40
Silicon area	mm²		0.4	
Normal mode I_{sup} (LIN recessive)	mA	0.7	1.2	2
Normal mode I_{sup} (LIN dominant)	mA	1.7	3	4.8
Sleep mode I_{sup}	uA	2.5	7.2	22
Pullup	kΩ	23	30	37
Weak Pullup	kΩ	222	300	379
Slope time	µs	5	10	15

ESD/EMC compliance

Built-in 4kV IEC 61000-4-2 combined ESD clamp at LIN and VSUP for area efficiency. Compatible with IEC 62228-2 for RF emission (class III) and immunity (class III damage; class II malfunction).

Physical implementation

- TSMC 0.18um BCD Gen II 1P5M
- No UTM, MIM cap or STI required
- Pad size 70um x 70um

ATE test

The LIN PHY contains 2 analog test bus pads (ATB1/2). These can be used for probing at ATE wafer sort. Optionally they can also be bonded for final test. They are designed for 1kV HBM. The LIN PHY comes with a detailed ATE test plan and optional support during customer testing.

About Sofics

Sofics (www.sofics.com) is a foundry independent semiconductor IP provider that has supported 100+ companies worldwide with customized/specialty Analog IOs and on-chip ESD protection. Fabless companies using Sofics IP can enable higher performance, higher robustness and reduce design time and cost. Our technology has been characterized on 11 foundries, including advanced nodes at TSMC, UMC, GF, Samsung Foundry, as well IDM companies, including Toshiba, Rohm, Epson-Seiko, Infineon and ST Microelectronics.

Sofics IP is used for design projects at 6 out of the top-10 semiconductor companies. The technology has been silicon proven on more than 50 different processes and integrated into more than 4500 IC designs since 2000.

Sofics has also developed robust circuit and interface solutions that handle transient disturbances. The design described in this datasheet covers a LIN transceiver hard-IP block to enable (fabless) companies to embark into the fast-growing market of automotive applications.

Sofics online

More information can be found online

- Website: www.sofics.com
- Blog articles: https://monthly-pulse.com/
- LinkedIn: http://linkedin.com/company/sofics
- Twitter: https://twitter.com/Sofics_team
- Vimeo video channel: https://vimeo.com/sofics

Notes

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Sofics BV

SINT-GODELIEVESTRAAT 32
B-9880 Aalter, Belgium

(tel) +32-9-21-68-333

bd@sofics.com

RPR 0472.687.037