Cell listing

Analog I/O's with high ESD robustness

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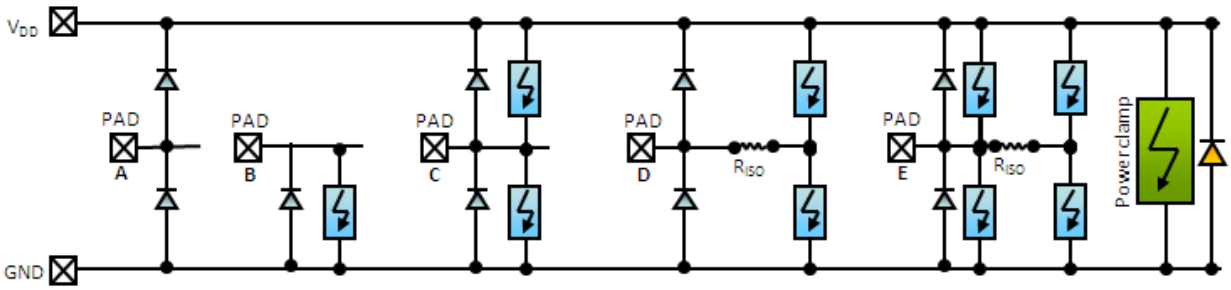
Sofics has verified its TakeCharge ESD protection clamps on a wide variety of processes, including CMOS, SOI and FinFET technologies across various fabs and foundries. The ESD clamps are silicon and product proven in more than 3000 mass produced IC-products. The cells provide competitive advantage through improved yield, reduced silicon footprint and enable high speed, higher operating voltages and complex architectures. Higher robustness level for a wide range of ESD/EOS and other specifications are available upon request.

Analog I/O's with high ESD robustness

The following table provides an overview of the Sofics High ESD clamps in advanced CMOS. The solutions are highly portable to other processes and different flavors.
Furthermore, the cells can easily be adopted for other ESD protection levels and can be further customized to ensure compatibility with specific metal schemes and I/O pitch. Cells for other voltage domains can be provided as well.
All clamps in the table were created based on customer requests, other options are available. Please discuss your specific requirement with our sales person at bd@sofics.com.

The Sofics ESD cells cover all types of protection concepts and approaches as detailed in the figure below.



Different pad types available in the solution set from Sofics. For each power domain a power clamp is available. For the IO's several pad-types exist.

Foundry	Node	Voltage domain [V]	Type clamp	Leakage	Cap [fF]	ESD performance	Info
Atmel	130	3.3	PC, B	< 50pA	900	> 8kV HBM	Includes Power clamp and protection for 2 IO's
Atmel	130	5	PC	< 100pA	NA	8kV IEC, > 8kV HBM	
TJ	130	1.2	C	<50pA	<150	>5 kV HBM, >400 V MM	Full local protection
TJ	130	1.2	E	<10nA	<200	>4 kV HBM, >200 V MM	Full local protection
TJ	130	3.3	PC, B	<50pA	NA	>5 kV HBM, >250 V MM	
TJ	130	3.3	E	<50pA		>5 kV HBM, >400 V MM	Full local protection
TJ	350	4.5	PC	<100pA	NA	>8 kV HBM	Circuit Under Pad
TJ	350	4.5	A	<100pA	<250	>8 kV HBM	Dual diode protection, Circuit Under Pad
TJ	350	4.5	D	<100pA	<560	>8 kV HBM	Dual diode protection & secondary protection, Circuit Under Pad

TJ	350	4.5	B	<500pA	<350	>8 kV HBM	Overvoltage/Under-voltage Tolerant, Circuit Under Pad
TJ	350	4.5	C	<1nA	<560	>8 kV HBM	Full local protection, Circuit Under Pad
TSMC	16	1.8	PC	<500pA	NA	4 kV HBM	
TSMC	40	0.9	B	<10pA	177	5 kV HBM, 260 V MM	
TSMC	40	1.1	B	<10pA	177	5 kV HBM, 260 V MM	
TSMC	40	1.2	B	<10pA	177	5.2 kV HBM, 260 V MM	
TSMC	40	3.3	PC, B	<500pA	NA	4 kV HBM, 300 V MM	
TSMC	65	1	A	<1nA	<100	4 kV HBM	Dual diode protection, Circuit Under Pad
TSMC	65	1.2	PC	<1nA	NA	7 kV HBM	Circuit Under Pad
TSMC	65	1.2	A	<1nA	<100	4 kV HBM	Dual diode protection, Circuit Under Pad
TSMC	65	1.2	A	<500pA	220	4 kV HBM, 400 V MM	Dual diode protection, Circuit Under Pad
TSMC	65	1.8	A	<1nA	<100	4 kV HBM	Dual diode protection, Circuit Under Pad
TSMC	65	1.8	A	<500pA	220	4 kV HBM, 400 V MM	Dual diode protection, Circuit Under Pad
TSMC	65	2.5	A	<1nA	<100	4 kV HBM	Dual diode protection
TSMC	65	2.5	A	<500pA	220	4 kV HBM, 400 V MM	Dual diode protection, Circuit Under Pad
TSMC	65	3.3	A	<1nA	<100	4 kV HBM	Dual diode protection, Circuit Under Pad
TSMC	65	3.3	A	<500pA	220	4 kV HBM, 400 V MM	Dual diode protection, Circuit Under Pad
TSMC	65	5	PC	<1nA	NA	4 kV HBM	
TSMC	65	5	C	<100nA	NA	4 kV HBM	Full local protection
TSMC	130	1	B	<50pA	98	4 kV HBM, 250 V MM	
TSMC	130	1	C	<50pA	180	4 kV HBM, 250 V MM	Full local protection
TSMC	130	1.2	PC	<50nA	NA	4.5 kV HBM, 370 V MM	
TSMC	130	1.2	C	<50pA	180	4 kV HBM, 250 V MM	Full local protection
TSMC	130	1.2	B	<50pA	98	4 kV HBM, 250 V MM	
TSMC	130	3.3	PC	<10nA	NA	4.5 kV HBM, 370 V MM	

TSMC	130	3.3	C	<100nA	132.3	4 kV HBM, 330 V MM	Full local protection, 2 Ohm series resistance
TSMC	130	3.3	B	<50pA	98	4 kV HBM, 250 V MM	
TSMC	130	3.3	C	<50pA	180	4 kV HBM, 250 V MM	Full local protection
TSMC	130	7	PC, B	<1nA	NA	4 kV HBM, 400 V MM	
TSMC	180	1.8	A	<200pA	159	5.5 kV HBM, 200 V MM	Dual diode protection
TSMC	180	1.8	PC, B	<200pA	295.6	5.5 kV HBM, 200 V MM	Overvoltage tolerant
TSMC	180	1.8	C	<200pA	266	5.5 kV HBM, 200 V MM	Full local protection
TSMC	180	1.8	C	<200pA	296	5.5 kV HBM, 200 V MM	Full local protection
TSMC	180	3.3	A	<200pA	159	5.5 kV HBM, 200 V MM	Dual diode protection
TSMC	180	3.3	PC, B	<200pA	288	5.5 kV HBM, 200 V MM	Overvoltage tolerant
TSMC	180	3.3	C	<200pA	288	5.5 kV HBM, 200 V MM	Overvoltage tolerant
TSMC	180	3.3	B	<200pA	301	5.5 kV HBM, 200 V MM	Overvoltage tolerant
TSMC	180	5	PC, B	<5nA	NA	8 kV HBM, 350 V MM	
TSMC	180	7	PC	<50nA	NA	8 kV HBM, 350 V MM	
UMC	65	2.5	PC	<10nA	NA	7.5 kV HBM, 470V MM	
UMC	65	3.3	PC	<10nA	NA	6.5 kV HBM, 400 V MM	
UMC	130	1.2	E	<10nA	118	4 kV HBM, 370 V MM	Full local protection, 2 Ohm series resistance
UMC	130	3.3	E	<10nA	118	4 kV HBM, 370 V MM	Full local protection, 2 Ohm series resistance

About CDM

It is noted that the listed cells do not contain a CDM specification. CDM levels for a stand alone cell are technically not relevant. Notwithstanding this, all ESD solutions provided by Sofics are optimized for CDM performance. The CDM design is based on

- ESD clamps with trigger speed enhancements and specific CDM clamp circuits
- VF-TLP analysis with fast rise time and short pulses
- Evaluation of the sensitivity of the (functional operation) circuitry
- Analysis of the different voltage domains and bus architecture
- General ESD/CDM expertise

The CDM performance of the Sofics' protected pins in actual integrated circuits routinely pass 500V, and 250-300V for high speed pins.

About porting

All cells can be ported to any CMOS process, though the actual numbers (leakage, capacitance) may vary slightly.
For typical behavior, no additional silicon validation is required. Typical behavior includes achieving ESD levels. The porting is based on

- Sofics' measurements on the given process (if available)
- Porting experience of over 50 processes
- PDK data

For optimization of leakage and/or capacitance, an additional silicon validation run may be advisable, depending on the required level and accuraccy.

About Sofics

Sofics (www.sofics.com) is the world leader in IP for robust IC design. Its patented technology is proven in more than 3000 IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/O's, other non-standard I/O's, and high-voltage ICs, including those that require system-level protection on the chip for ESD, EOS, EMC, radiation or other specifications.

Sofics technology produces smaller I/O's than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
    - Enable unique requirements for Latch-up, ESD, EOS
    - Layout, metallization and aspect ratio customization
    - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

Version

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