



Conference paper Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling

EOS/ESD symposium 2001

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Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling

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Abstract - A silicon-proven *multi-finger turn-on* (MFT) design technique that enables ESD width scaling combined with very low dynamic on-resistance is presented in various implementations. It can be applied to (self-protecting) drivers and/or ESD protection design. Using a novel merged ballast circuit design, very compact ESD protection configurations with an ESD area performance up to $5V_{\text{HBM}}/\mu\text{m}^2$ can be realized both in fully silicided and silicide blocked NMOS designs.

I INTRODUCTION

Uniform triggering and current flow in multi-finger devices is key for on-chip ESD protection. So far, various multi-finger *trigger* concepts have been applied to enhance uniform current flow and thus width scalability.

Verhaege *et al.* briefly introduced the basic features of a novel multi-finger *turn-on* (MFT) technique [1]. Various MFT implementations and optimization techniques will be extensively discussed in this paper.

II MULTI-FINGER TRIGGERING ISSUE

The nature of (parasitic) BJT snapback, i.e. the negative differential resistance regime, presents undesired effects in single- as well as multi-finger devices. For inappropriately designed single-finger structures, voltage snapback may result in early local current collapsing accompanied by filamentation and thermal runaway. In order to cope with this issue of poor single-finger ESD performance, sufficient '*micro-ballasting*' needs to be introduced. This can be achieved by implementing silicide-blocked drain and source regions. Another ballast option to maintain fully-silicided IC design, is the incorporation of segmented back-end-ballast (BEB) resistance as shown by Verhaege *et al* [1]. In an extremely 'weak' technology, it was demonstrated that by applying this BEB technique to fully-silicided ggNMOS single-finger devices, the intrinsic ESD performance could be restored from 'zero' to $I_{t2} = 10\text{mA}/\mu\text{m}$.

Satisfying the uniform triggering condition

The major issue for multi-finger devices is that the number of fingers initially driven into snapback is statistically distributed – mostly only one arbitrary finger is triggered. To eventually reach a uniform current conduction state in snapback multi-finger ESD protection devices, the so-called 'uniformity (or homogeneity) condition'

$$V_{t2} > V_{t1}$$

must be fulfilled, cf. Figure 1. This means that the single finger failure voltage V_{t2} must be higher than the parasitic BJT trigger voltage V_{t1} at the onset of snapback.

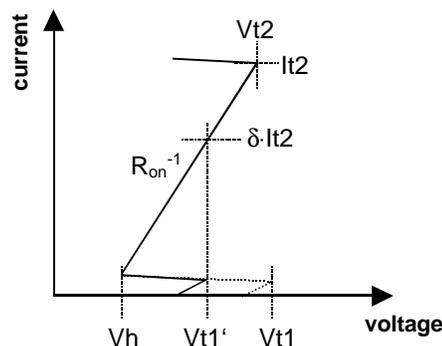


Figure 1 Sketch of a generic snapback IV curve indicating characteristic single-finger parameters: triggering voltage V_{t1} , MFT voltage V_{t1}' , holding voltage V_h , failure voltage V_{t2} , failure current I_{t2} , MFT current δI_{t2} with $0 \leq \delta I_{t2} \leq I_{t2}$. The dynamic on-resistance R_{on} is inversely proportional to the IV slope in the linear BJT high current region.

Figure 2 shows the snapback TLP-IV curves of regular fully-silicided multi-finger ggNMOS transistors (0.18um-CMOS technology) where the gate width was varied from $W = 1x$ to $12x50\mu m$. For these structures, the uniformity condition is not satisfied. Therefore, all structures reveal the same failure level, indicating that only one finger conducts the TLP current until the single segment fails.

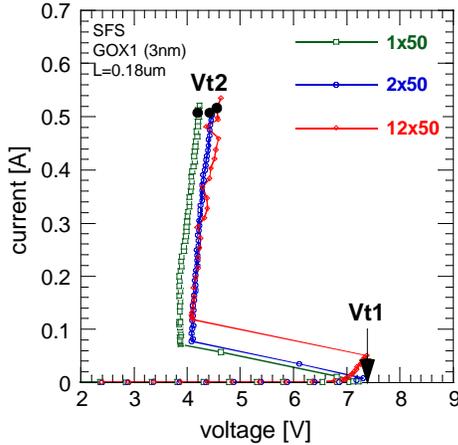


Figure 2 Snapback IV-curves of regular fully-silicided ggNMOS devices ($W=1, 2, 12x50\mu m$) indicating no multi-finger width-scaling behavior of the ESD performance.

To meet the uniformity condition and thus to improve the ESD robustness of these multi-finger devices, one has two options: firstly, increase V_{t2} and/or, secondly, reduce V_{t1} .

Increase V_{t2} to fulfill $V_{t2} > V_{t1}$

V_{t2} can be increased by adding ballast resistance to the structure, e.g. by introducing silicide blocking [2], back-end ballasting [1], or N-well resistor extensions [3], [4] into NMOS-type protection structures. We refer to this type of ballasting as ‘macro-ballasting’ in order to differentiate from the micro-ballasting that is required to reach the single-finger performance target value.

A major drawback of the macro-ballasting approach (or ‘Ron-engineered MFT’, cf. below) is the increase of the clamping voltage caused by the higher dynamic on-resistance as well as higher power dissipation for the same ESD current. Moreover, a significantly larger silicon real-estate is required to provide the ballast resistance. Besides this ballasting area consumption, more area is required for efficient voltage clamping during ESD stress.

Reduce V_{t1} to fulfill $V_{t1} < V_{t2}$

Both ‘static’ and ‘dynamic’ design techniques have been established to reduce the trigger voltage V_{t1} and to ensure uniform ESD current conduction [5]-[7].

For example, using a Zener diode breakdown to pull up a gate (or base) of a NMOS (parasitic npn) device is a static design technique, which is largely independent of other conditions than static voltage bias. In general, when a certain I-V bias is reached, the V_{t1} reduction goes into effect quasi independent of any dynamic parameter. In this respect, adding series on-resistance can also be classified as a static technique to increase V_{t2} .

A dynamic approach is typically based on a RC circuit, which will provide temporary bias to a gate (or base). Well-known designs are the gate-coupled NMOS [6], [7] base coupling (or substrate pumping [8]), and dynamic triggering [6]-[9]. For these approaches dynamic boundary conditions must be fulfilled, which leads to several challenges and issues for successful dynamic trigger implementations. Furthermore, due to the significant capacitance added to the protection structure, these multi-finger triggering schemes disqualify for RF I/O applications.

III MFT PRINCIPLE

In multi-finger turn-on MFT ESD protection devices, a different approach is applied to fulfill the uniformity condition $V_{t2} > V_{t1}$. The generic MFT method is to derive a multi-finger turn-on bias signal from a non-uniform conduction situation. This bias signal is transferred to inactive device segments by transfer circuits to activate gate and/or bulk bias turn-on schemes. This will ensure that the uniformity condition is satisfied after the first triggering event at regular V_{t1} . A modified *MFT uniformity condition* according to Figure 1 could be expressed as

$$V_{t1}' < V_{t2}$$

where V_{t1}' corresponds to the trigger voltage of those fingers that did not trigger initially at V_{t1} – the MFT voltage. Therefore, we also refer to the novel device type as ‘ V_{t1} -engineered MFT’ as opposed to the ‘Ron-engineered MFT’ where multi-finger triggering is reached by pure ballast resistance implementation only.

One distinguishes different turn-on mechanisms:

- *Subsequent turn-on:* bias signals are propagated from finger to finger. Fingers turn on subsequently.

- *Simultaneous turn-on:* the bias signal is fed to all fingers at the same time. Fingers can turn-on simultaneously (if snapback is ‘eliminated’).

These types differ mainly in their transfer circuits to provide the turn-on bias and in the applicability within self-protecting output drivers.

An important feature, as discussed in the next sections, is that MFT designs are static and some feature an ‘auto-timed’ current balancing mechanism:

- *Static auto-on:* the MFT effect is derived from a static bias, which is largely independent of other conditions. When a certain ESD current level is reached in the active device part, the MFT goes in effect. No dynamic boundary conditions exist.
- *Static auto-off:* in some implementations the MFT bias is only present as long as there is non-uniform conduction state. When the device uniformly carries the ESD current, the bias vanishes. This is particularly advantageous in view of hot carrier exposure when a gate biasing technique is used.

IV NMOS MFT IMPLEMENTATIONS

The following sections focus on various MFT implementations.

IV.1 Soft-grounded-gate NMOS MFT

The equivalent circuit of a gate-bulk coupled or soft-grounded-gate NMOS MFT (s-ggNMOS) device is depicted in Figure 3. This particular gate-biasing technique is based on a substrate potential pick-up, which ties the gates to the local substrate (bulk) rather than wiring it hard to ground by metal as in a ggNMOS device. During normal operation, the bulk is safely grounded, hence disabling NMOS action and avoiding interference with the normal IC functionality.

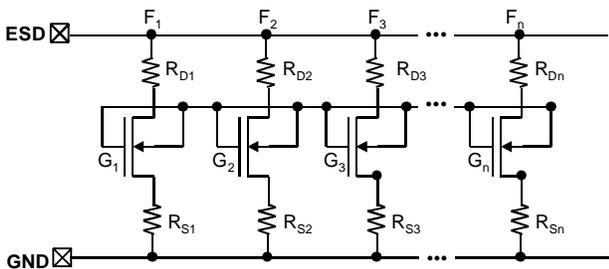


Figure 3 Equivalent circuit of a soft-grounded-gate NMOS MFT for simultaneous gate-biasing and multi-finger turn-on.

In case of an ESD event, however, the drain-bulk junctions of all NMOS transistor fingers are driven into avalanche breakdown and impact generated holes

are locally injected into the substrate thus lifting its potential. Eventually, at a self-bias of approximately 0.8V, the avalanche process turns on the parasitic BJT within one (or more) arbitrary finger(s). During subsequent snapback of the activated device segment, the substrate is further pumped with holes. The resulting positive potential due to avalanche breakdown and snapback operation is applied to the gate and indirectly also to the bulk ties of other fingers.

Due to gate-coupling and bulk-coupling effects, the MFT voltage of inactive device parts is reduced ($V_{t1}' < V_{t1}$) enabling multi-finger turn-on of the entire device. Note, the resistors R_{D1} and R_{S1} might be required for micro-ballasting of single finger as well as macro-ballasting to increase V_{t2} and to further support multi-finger triggering by fulfilling $V_{t1}' < V_{t2}$.

IV.2 Domino-type MFT

Figure 4 depicts the domino-type MFT for subsequent finger triggering. This configuration consists of n NMOS transistor fingers in parallel who will turn-on one after the other in analogy to falling domino blocks.

The drain and source resistors R_{Di} and R_{Si} are implemented for single-finger micro-ballasting and will also support multi-finger triggering by macro-ballasting. The resistors $R_{Si,MFT}$ in each source finger are used to generate a potential for activation of the MFT voltage reduction mechanism ($V_{t1}' < V_{t1}$). If single finger ESD performance is uncritical, only the source resistors $R_{Si,MFT}$ are required to achieve homogeneous current flow in MFTs. The MFT mechanism for the domino-type device is explained in detail in the following.

After one arbitrary finger triggers as indicated by the arrow at finger F_2 , the initial stress current is solely conducted by this device segment. As a result, a source potential V_{Si2} builds up at the internal source node $Si2$ due to the voltage drop across $R_{S2,MFT}$. These source resistor elements can be regarded as ESD current sensors, which are implemented into each finger, firstly, to sense ESD events, and, secondly, to provide the signal to turn on inactive fingers - in the case of the domino-type MFT the adjacent finger. Moreover, these resistors act as regular macro-ballasting elements by increasing the dynamic on-resistance in the single elements. As detailed in section VI, this combined purpose allows extremely area efficient MFT layouts. The potential V_{Si2} is applied to the NMOS gate of finger F_3 by connecting

the gate to the internal source node Si_2 . As long as F_3 is inactive and no current flows through this finger, V_{Si_3} will be zero and thus a positive gate-source bias V_{GS3} will exist. This will eventually drive the finger into NMOS operation, which results in a reduction of the parasitic NPN triggering voltage due to the well-known gate-coupling effect. Note, even for sub-threshold gate bias, generally a significant V_{t1} reduction occurs as will be demonstrated below.

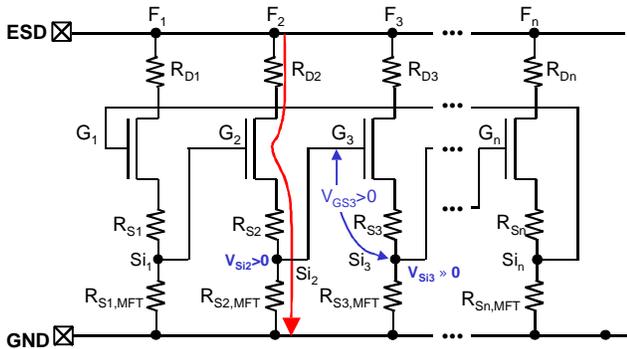


Figure 4 Equivalent circuit of domino-type NMOS MFT (source-gate-coupled) for subsequent finger triggering indicating the function of the device.

By sufficiently decreasing V_{t1} towards the holding voltage, eventually the inactive finger F_3 turns on. The same mechanism transfers the internal source signal at Si_3 to the gate of F_4 , thus triggering this finger. By creating this domino-effect of subsequently triggered fingers, eventually the entire structure is forced into a homogeneous conduction state.

The domino MFT design technique has two major advantages:

- The MFT mechanism is ‘static’ and driven instantly by current, not time. Thus, no timing issues as for instance for dynamic gate-coupling schemes can occur as described above.
- The MFT mechanism is ‘auto-timed’ – it only acts during a limited (i.e. short) time interval, until uniform current conduction is reached. Evidently, in this state, the current is equally distributed to all fingers such that all internal source nodes are on the same potential. As a result, no gate-source bias exists, which prevents the structure from excessive hot-carrier exposure.

Therefore, the MFT technique does not only enhance multi-finger triggering, it also provides a dynamic balancing bias between fingers that would conduct different amounts of current.

Both the MFT implementations as shown in Figure 3 and Figure 4 can only be employed as pure ESD protection clamps because of the gate connection to

ground. Though not described here, domino-type MFT designs can be adopted to make self-protecting NMOS drivers. In the next two sections, other MFT schemes will be presented, which can be applied as self-protecting NMOS drivers as well.

IV.3 NMOS-type MFT

The schematic in Figure 5 shows a different type of gate driven triggering and current balancing MFT. The active approach employs small NMOS transistors N_{gi} . These elements control simultaneously the bias of the common gate line connected to all gates G_i of the ESD-current conducting NMOS fingers N_i in parallel. The advantage of the presented circuitry is that it can be applied in NMOS output drivers since gate bias from a pre-driver stage can be supplied, whereas the ESD triggering elements $R_{Si,MFT}$ and N_{gi} do not compromise regular circuit operation. The principle approach of sensing an ESD conduction state of an arbitrarily triggered finger and of generating a signal for the turn-on of inactive segments is equivalent to the method presented above for the domino-type MFTs.

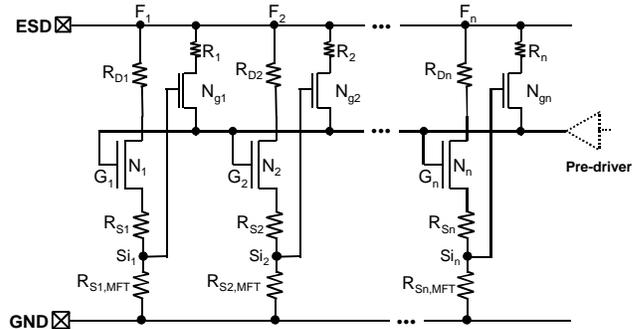


Figure 5 Equivalent circuit of NMOS-type MFT for simultaneous gate-biasing and multi-finger turn-on.

Again, MFT source resistors $R_{Si,MFT}$ are inserted in each source finger to derive a bias signal during ESD current conduction. The potential at the internal source node Si of an initially triggered finger is used to positively bias the gate of the small NMOS transistor N_{gi} . Note, these NMOS devices act as voltage followers, i.e. they transfer the source potential to the common MFT gate as soon as V_{Si} exceeds the threshold voltage V_{th} . Thus, the common MFT gate is simultaneously biased to a gate voltage $V_{G,MFT} = V_{Si} - V_{th}$. This reduces the MFT voltage V_{t1}' of all parasitic BJTs simultaneously as opposed to the subsequent approach of the domino-type MFT. If the snapback effect is removed by gate-coupling, the technique forces all fingers simultaneously into the BJT on-state.

To achieve a sufficient gate bias, $R_{Si,MFT}$ should be designed to provide more than $2 \cdot V_{th}$ internal source voltage for an ESD current well below the failure-level I_{t2} of the single finger. This results in an efficient MFT gate-bias above V_{th} , which ensures a strong gate-coupling effect, i.e. MFT voltage V_{t1} reduction.

During normal operation, regular MOS currents through the NMOS device do not interfere with circuit behavior since only negligible voltages occur at the internal source node.

IV.4 Diode-type MFT

One more MFT approach is depicted in Figure 6. The principle function of simultaneous gate-biasing is identical to the NMOS-type MFT. In this configuration, however, minimum sized diodes $D_1 \dots D_n$ are employed as transfer circuits between the internal source nodes and the common MFT gate line.

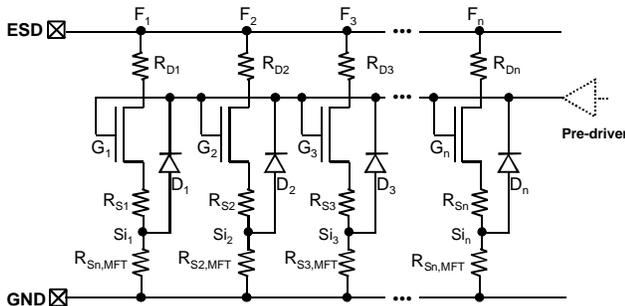


Figure 6 Equivalent circuit of diode-type MFT for simultaneous multi-finger turn-on.

After finger F_i conducts ESD stress current, the corresponding diode D_i becomes forward biased. The other diodes will be reverse biased, thus preventing charge loss from the gate line to ground. In accordance to the NMOS-type MFT, a small diode current can charge all MFT gates simultaneously. In case of efficient gate-bias and smooth transition to the BJT on-state (no snapback!), eventually all inactive fingers will be turned on simultaneously.

As discussed for the NMOS-type MFT, this implementation is also compatible with normal MOS operation and thus can be exploited as self-protecting drivers.

To achieve an efficient gate-coupling effect, again an MFT gate-bias higher than the NMOS threshold voltage V_{th} is targeted. Therefore, the MFT resistor $R_{Si,MFT}$ must provide the diode built-in voltage plus MOS threshold V_{th} , i.e. $V_{Si} = V_{diode} + V_{th}$. Schottky diodes could be used to reduce V_{diode} to ca. 0.3V.

The diode-type MFT maintains only a small gate-source bias in the homogeneous conduction state. This balancing concept was referred to as auto-on/off in section IV.2.

V MFT SIMULATION

In this section, a principle approach for MFT simulations is described.

A generic ESD NMOS model (SPICE) was developed, which includes the parasitic BJT snapback behavior as well as the gate-coupling effect (reduction of V_{t1} with increasing gate-bias) on a behavioral basis.

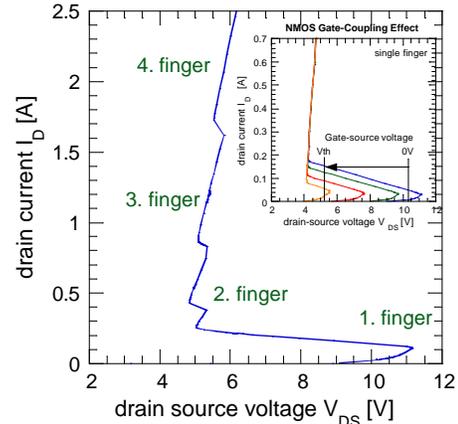


Figure 7 Simulation of 4-finger domino-type NMOS MFT structure indicating current dependent multi-finger turn-on. Inset: simulation of gate-coupling effect for a single NMOS finger.

The model was applied to illustrate semi-quantitatively the functionality of a 4-finger domino-type NMOS MFT. Model parameters were estimated according to a 50um-wide NMOS finger. An essential point for reproduction of the actual multi-finger triggering issue in simulation is Monte Carlo simulation for a dynamical and random alteration of model parameters in accordance to device fluctuations in silicon. As such, initial triggering of an arbitrary finger is simulated, as shown in Figure 7. At a certain current level, the gate of an adjacent finger is sufficiently biased to activate the corresponding device part. MFT operation is sustained for increasing current until all fingers are fully turned on.

The simulation agrees semi-quantitatively with the experimental results presented in the following sections for various MFT incorporations.

VI MFT DESIGN AND OPTIMIZATION

VI.1 MFT Design

In this section, the design of MFT structures – in particular the crucial MFT source resistance $R_{S,MFT}$ – will be addressed.

According to Figure 1, in MFT devices, multi-finger turn-on is reached when the reduced single-finger MFT voltage V_{t1}' is lower than the voltage at second breakdown V_{t2} , i.e. the modified uniformity condition $V_{t1}' < V_{t2}$ must be fulfilled. To accomplish first-silicon success for MFT design under area optimized conditions, it is beneficial to measure the gate-coupling effect, i.e. the MFT voltage V_{t1}' as a function of the gate-source bias. The corresponding data as extracted from static snapback IV curves of an NMOS transistor (7nm gate, 0.18 μ m-CMOS) is presented in Figure 8. Obviously, a significant reduction of V_{t1} occurs already at sub-threshold gate-bias.

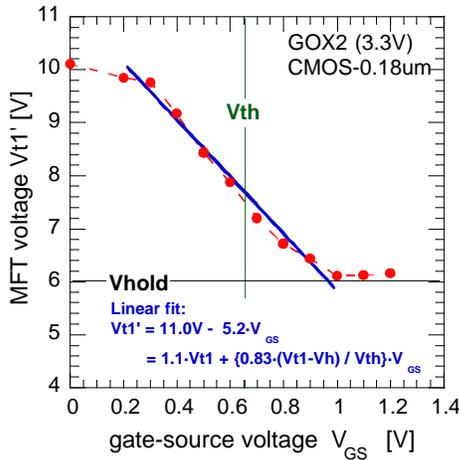


Figure 8 MFT voltage V_{t1}' as a function of the gate-source bias in a 3.3V-NMOS device (0.18 μ m-CMOS) as extracted from static snapback IV curves. A significant V_{t1} reduction is already reached for sub-threshold gate bias $V_{GS} < V_{th}$.

In order to describe this behavior analytically, a linear fit is applied to the curve in the relevant gate-source voltage regime. The linear approximation for $V_{t1}' = f(V_{GS})$

$$V_{t1}' = g \cdot V_{t1} + a \cdot \left\{ \frac{V_{t1} - V_h}{V_{th}} \right\} \cdot V_{GS}$$

contains two parameters, to be experimentally determined from the slope (α) and the y-axis intersection (γ). From the linear fit in Figure 8, the values $\gamma = 1.1$ and $\alpha = 0.83$ are extracted.

The gate-source voltage V_{GS} in a domino-type MFT, cf. Figure 4, is generated by the voltage drop across

$R_{S,MFT}$ at a current-level of $\delta \cdot I_{t2}$ required for turn-on of the next finger, i.e.

$$V_{GS} = R_{S,MFT} \cdot I_{t2} \cdot d$$

The failure voltage V_{t2} at a failure current I_{t2} can be described as

$$V_{t2} = V_h + R_{on} \cdot I_{t2} = V_h + (R_{ballast} + R_{S,MFT}) \cdot I_{t2}$$

Here, $R_{ballast} = R_D + R_S$ corresponds to the sum of ballast resistance at the drain and source side of the single NMOS fingers. Combining the last three equations inserted into the modified MFT uniformity condition $V_{t1}' < V_{t2}$ results in

$$R_{ballast} + R_{S,MFT} \cdot \left\{ 1 + a \cdot d \cdot \frac{V_{t1} - V_h}{V_{th}} \right\} > \frac{1}{I_{t2}} (g \cdot V_{t1} - V_h)$$

For the values of the regular fully-silicided ggNMOS structures in Figure 2 ($V_{t1} = 7.5V$, $V_h = 4V$, $V_{th} = 0.52V$, target value $I_{t2} = 0.5A$ for a 50 μ m-wide device, and $\delta = 0.75$ for subsequent finger triggering at $\delta \cdot I_{t2} = 0.38A$) the previous equation simplifies to

$$R_{ballast} + 4.2 \cdot R_{S,MFT} > 8.5\Omega \text{ for a single finger}$$

Three crucial facts can immediately be derived from this relation:

- The relation directly demonstrates and quantifies one major advantage of MFT implementation compared to regular ballasting approaches: the MFT resistor $R_{S,MFT}$ is approximately a **factor of 4 more efficient** for multi-finger triggering than plain ballast resistance $R_{ballast}$ implementation! This provides tremendous direct area savings since less ballast area is required for scalable multi-finger devices. Indirect area savings can be significant due to superior voltage clamping capabilities accomplished by a lower dynamic on-resistance R_{on} of the protection device. These advantages are experimentally verified and presented in section VII.2.
- The formula provides straight-forward guidelines for MFT resistance design.
- The equation underlines that a safe MFT design with regard to process fluctuations (e.g. BEB resistance values) can be easily realized by a well-defined $R_{S,MFT}$ without increasing the total on-resistance significantly.

VI.2 Poly BEB Implementation

Figure 9 illustrates a concept of a fully functional, metal 1 - routed ESD protection design. Basically, poly resistor arrays are employed to form the segmented drain and source back-end-ballast [1] (BEB). In addition, on the source-side an MFT source-potential pick-up contact is inserted. This splits the resistor into a segmented ballast resistor part R_{Sn} and the MFT source resistor $R_{Sn,MFT}$ in accordance to the MFT schematics in Figure 4, Figure 5, and Figure 6. Even with only poly exploited for BEB, area efficient ESD protection elements can be introduced due to the highly efficient $R_{Sn,MFT}$ resistor.

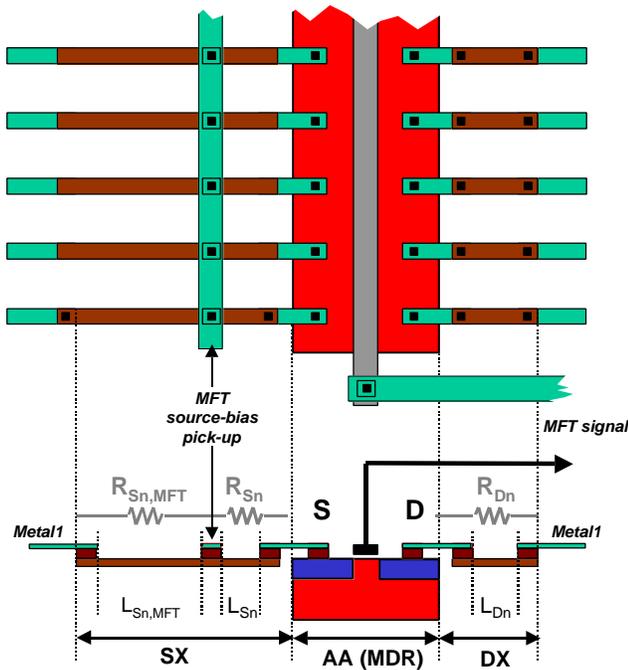


Figure 9 Layout and cross-section sketch of optimized MFT design using poly resistor arrays for segmented back-end-ballast R_{Dn} , R_{Sn} and MFT source resistance $R_{Sn,MFT}$ implementation.

The segmentation concept offers a further option to significantly compact the MFT protection design as discussed in the next chapter.

VI.3 Merged Ballast Circuit (MBC) Technique

Figure 10 shows the sketch of a highly area optimized layout of a domino-type MFT. A novel ballast merging technique is applied which allows us to combine the poly stripe ‘combs’ such that two adjacent drain or source BEB elements, respectively, overlap and occupy the same space. In order to apply this approach, the contact pitch is increased to two times design rule minimum pitch. The authors have

confirmed in silicon that the double pitch does not deteriorate the ESD performance.

Figure 11 depicts a layout comparison of a 4-finger NMOS device with conventional poly-BEB and merged ballast approach. Applying this technique, more than 30% of area reduction is easily achieved.

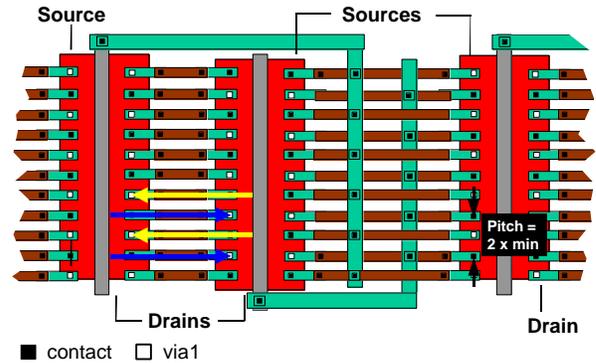


Figure 10 Layout sketch of domino-type MFT demonstrating the merged ballast circuit (MBC) technique used to significantly compact layout: ballast poly stripes of adjacent drain and source fingers, respectively, are combined within the same area.

Combining the advantage of efficient MFT ballasting resistance implementation, cf. section VI, and the merged ballast circuit technique in a 0.18 μ m-CMOS technology, an outstanding **ESD area performance of up to 5V_{HBM}/um²** could be realized. To our knowledge, this value represents a new milestone for NMOS-type ESD protection. Current industry solutions achieve approximately 1-1.5V_{HBM}/um² [10].

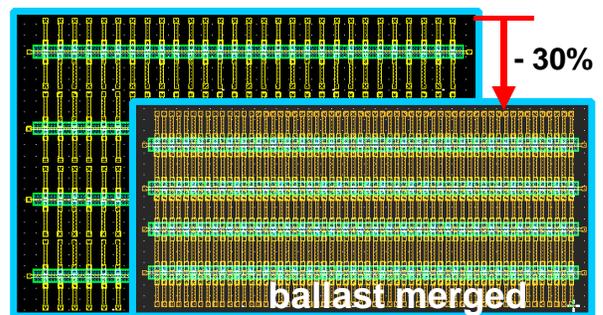


Figure 11 Comparison of 4-finger NMOS with conventional poly with BEB design to NMOS with merged ballast technique of adjacent fingers. Area savings of more than 30% can be achieved.

VI.4 I/O Implementation

Figure 12 compares an original silicide-blocked (bi-directional, over-voltage tolerant) I/O cell design (left) to the corresponding layout applying fully-silicided MBC MFT design (right) as self-protected cascoded NMOS devices and MBC PMOS drivers.

Due to the highly efficient MFT implementations, total area savings of more than 29% are demonstrated within this I/O cell.

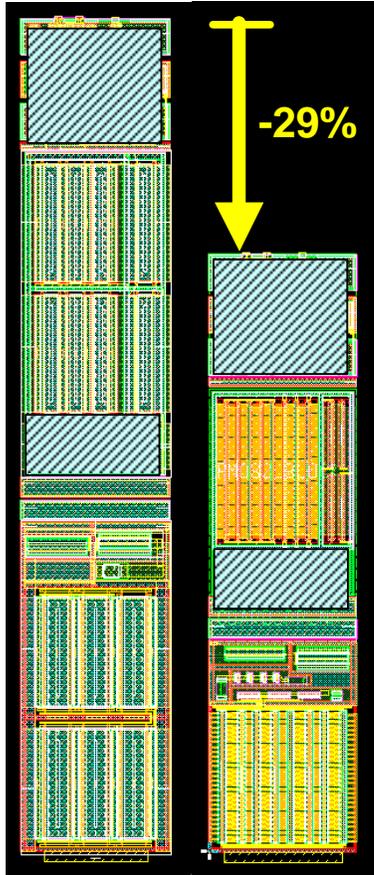


Figure 12 I/O cell of original silicide-block design (left) and fully-silicided MFT design applying MBC (right). The direct comparison indicates dramatic area savings of 29% possible with the new techniques.

VII EXPERIMENTAL RESULTS

All TLP data reported in this publication were measured with a Barth 4002 Transmission Line Pulse (TLP) tester with a pulse duration of 100ns.

The default rise time of the TLP transient edge was set to $t_{\text{rise}} = 10\text{ns}$, which represents the HBM relevant value and the worst-case regarding multi-finger triggering. This setting is important to gain objective

analysis results by largely suppressing dV/dt -triggering effects. An increased dV/dt -triggering sensitivity may be obtained for faster slew rates. The impact of fast rise times by dV/dt -triggering on the MFT behavior is discussed in section VII.5.

VII.1 Soft-Grounded Gate NMOS MFT

Figure 13 depicts TLP measurement data of the soft-grounded gate NMOS MFT in a 0.18 μm -CMOS technology.

The triggering voltage V_{t1} reflects the snapback of an initially triggered finger without trigger voltage reduction. By driving an arbitrary finger into snapback, the turn-on bias for another inactive segment is generated as described in section IV.1. The significantly reduced MFT voltage V_{t1}' is slightly higher than the holding voltage. A second finger can turn on when a sufficient but small voltage drop across the active device segment is provided. By the same effect all fingers are activated successively (cf. inset Figure 13) with increasing current. The resulting uniform conduction state and ideal width scaling are reflected in the failure current of $I_{t2} = 2\text{A}$, which corresponds to a normalized ESD performance of $I_{t2} = 10\text{mA}/\mu\text{m}$.

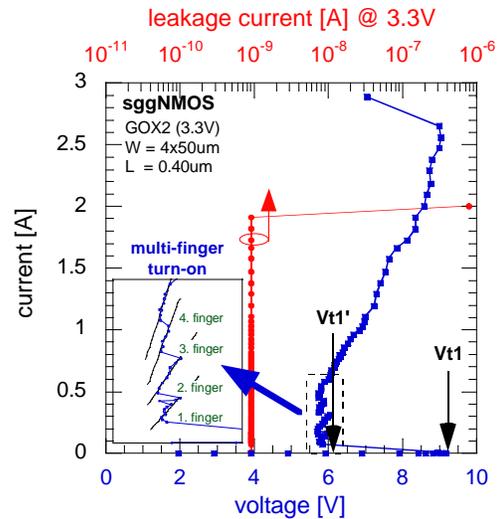


Figure 13 TLP snapback IV curve of a soft-grounded-gate NMOS MFT (7nm GOX2, $W = 4 \times 50\mu\text{m}$, $L = 0.40\mu\text{m}$) including leakage current evolution. Inset: close-up of triggering regime indicating successive finger turn-on with increasing current at a reduced MFT voltage V_{t1}' .

VII.2 Domino-type MFT

Figure 14 shows the TLP measurement results for a domino-type MFT. After initial device triggering at $V_{t1} \approx 7.5\text{V}$, the MFT mechanism reduces the turn-on

voltage of subsequently activated fingers to roughly $V_{t1}' \approx 5.5V$. By this, eventually all 16 fingers are forced into uniform current conduction, which results in an optimum failure current of $I_{t2} = 16 \times 50\mu m \times 10mA/\mu m = 8A$. This excellent result indicates again a perfect linear width-scaling behavior. Moreover, HBM stress tests up to the pre-charge voltage tester limit of 8kV could not damage this device.

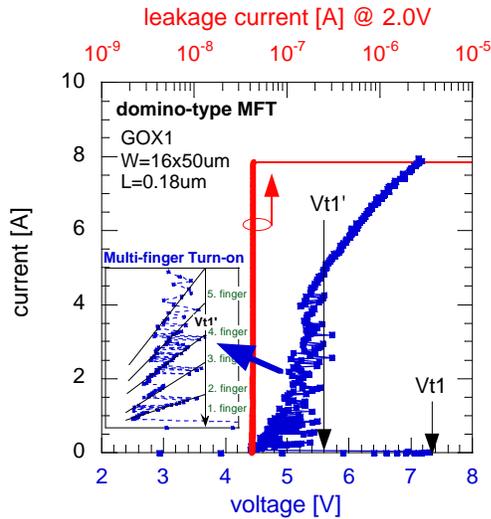


Figure 14 TLP snapback IV curve of a domino-type NMOS MFT (3.5nm GOX1, $W = 16 \times 50\mu m$, $L = 0.18\mu m$) including leakage current evolution. Inset: close-up of triggering regime indicating successive finger turn-on with increasing current at a reduced MFT voltage V_{t1}' .

VII.3 NMOS-type MFT

In Figure 15, TLP analysis data of an NMOS-type MFT (0.18 μm -CMOS) is presented.

Evidently, the trigger spikes of subsequently turned on fingers observed for the previous MFT devices are not visible for this configuration. This fact indicates a very efficient MFT gate biasing and thus gate-coupling effect, which reduces the MFT voltage to the ultimate minimum of roughly the holding voltage, i.e. $V_{t1}' \approx V_h$. Consequently, all fingers go simultaneously and smoothly into the BJT on-state without snapback.

In accordance to the domino-type MFT, again an excellent failure current of $I_{t2} = 8A$ (10mA/ μm) is reached. This verifies again an ideal performance scaling with device width. HBM tests of the NMOS-type MFT could not damage the device for pre-charge voltages of 8kV – the tester limit.

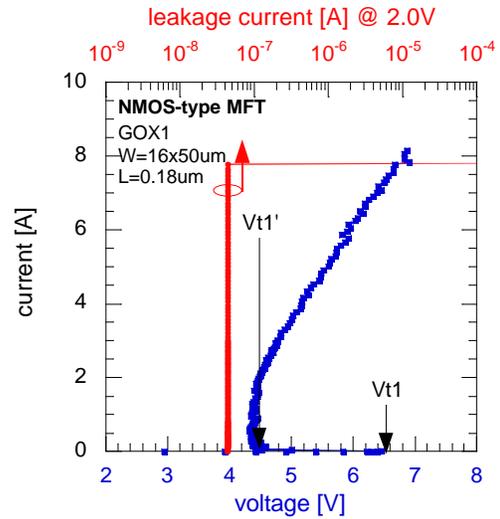


Figure 15 TLP snapback IV curve of a NMOS-type NMOS MFT (3.5nm GOX1, $W = 16 \times 50\mu m$, $L = 0.18\mu m$) including leakage current evolution. No triggering spikes of subsequently triggered fingers are visible due to a minimum MFT voltage $V_{t1}' \gg V_h$.

VII.4 Comparison to Ron-engineered MFT

The results in Figure 16 confirm the V_{t1}' -engineered MFT advantages, cf. section VI, compared to Ron-engineered MFTs. To demonstrate the effective ESD performance difference, the ESD design window is drawn also.

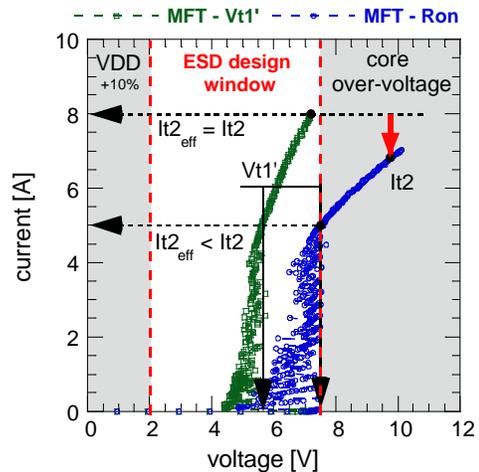


Figure 16 Comparison of TLP IV curves of Ron-engineered MFT and V_{t1}' -engineered MFT ($W = 16 \times 50\mu m$, $L = 0.18\mu m$). The specific ESD design window for this 0.18 μm -CMOS technology is drawn also.

The lower ESD design margin is defined by the operating voltage $V_{DD}+10\%$ safety margin. The upper limit is given by the transient oxide breakdown voltage (or TDDB: time dependent dielectric breakdown). This limit denotes a fundamental value for analytical ESD design. The experimental

procedure for the determination of TDDB by TLP analysis is described in [12].

The Ron-MFT triggering voltage is constant for all fingers, i.e. $V_{t1}' \approx V_{t1}$. Therefore, the voltage across the activated device segment has to build up to a high V_{t1} again to turn on the next finger. The resulting failure-level $I_{t2} = 6.8A$ reveals a sub-linear width scaling behavior: $I_{t2} = 16 \times 50\mu m \times 10mA/\mu m \times 0.85$. Moreover, the larger single-finger ballasting required to satisfy the uniformity condition $V_{t1} < V_{t2}$, causes an extensively increased dynamic on-resistance compared to the V_{t1}' -engineered MFT. Taking into account the core over-voltage exposure above TDDB, this results in a reduced effective failure current of only $I_{t2,eff} = 5A$ (6.3mA/ μm) compared to $I_{t2,eff} = 8A$ (10mA/ μm) for the V_{t1}' -engineered MFT. Obviously, apart from the more efficient $R_{S,MFT}$ resistance realization in MFT's, this result clearly underlines the superior ESD area performance of the MFT protection approach compared to Ron-engineered multi-finger devices.

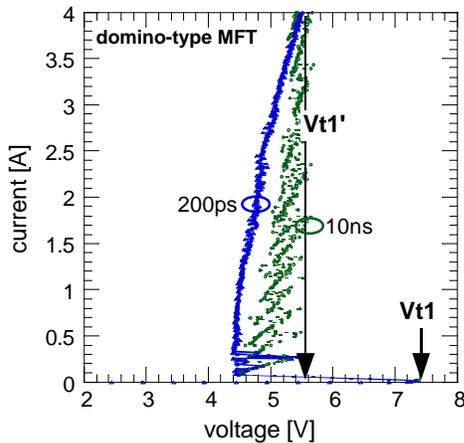


Figure 17 Snapback TLP-IV curves of domino-type MFT for different TLP rise times: $t_{rise} = 10ns$ (de'fault), 0.2ns.

VII.5 MFT at Fast Rise Times

One might assume subsequent turn-on MFT's as critical regarding triggering speed. Figure 17 shows TLP-IV data of a domino-type MFT for two different TLP edge rise times $t_{rise} = 10ns$ and 0.2ns. Obviously, the triggering voltage V_{t1} reveals no rise time sensitivity, which can also be attributed to the specific substrate ring pattern in the test structures where ring ties surround two fingers, respectively. However, it becomes evident that for the fastest rise time of 200ps and a current level above approximately 0.4A no triggering 'spikes' occur anymore, i.e. $V_{t1}' \approx V_h$. This means that dV/dt -effects support multi-finger triggering and eliminate the *issue*

of non-uniform current flow for very fast transients, such as CDM.

The results clearly disprove any triggering speed concern for MFTs.

VIII CONCLUSIONS

The multi-finger turn-on (MFT) technique is presented in conjunction with a highly area efficient merged ballast circuit (MBC) implementation. The MFT shows both 'static' and 'auto-timed' behavior to ensure uniform conduction and balancing of ESD current in multi-finger devices.

Advantages of Multi-Finger Turn-on (MFT) devices:

- MFT devices feature a novel approach to achieve scalable multi-finger ESD performance
- MFT can be accomplished with or without a minimum of ballasting resistance, e.g. introduced by silicide blocked contact-to-gate spacing, or back-end-ballasting. Thus, area consumption associated with ballast resistance implementation is largely reduced
- MFT design enables but does not require fully-silicided ICs
- Extremely compact and area efficient structures can be built:
 - The MFT resistance $R_{S,MFT}$ is approximately 4 times more efficient than regular ballast resistance implementation
 - The Merged Ballast Circuit (MBC) technique allows additional significant area savings
- There are no drawbacks in view of timing and transient interference with normal operation
- Analytical MFT design is straightforward and can be easily incorporated into any CMOS multi-finger protection structure
- Due to a minimum active area (drain-bulk junction), the parasitic capacitance is significantly reduced compared to silicide-blocked ggNMOS. In conjunction with the minimized dynamic on-resistance, this results in a drastic speed increase of self-protecting output-driver MFT devices
- Most MFT designs can be applied without any compromises for output driver stages
- Most MFTs function auto-timed, i.e. the current homogenizing effect is only activated in case of non-uniform current distributions
- In technologies where gate-coupling is not efficient to reduce V_{t1} towards a low MFT V_{t1}' , a bulk or combined bulk/gate-coupled MFT scheme can be applied.

ACKNOWLEDGMENTS

The authors gratefully acknowledge their Sarnoff co-workers Dana Brock for administrative support and Bill Mayweather for management support. The authors also acknowledge the critical review and valuable suggestions by the mentor of this paper Jeremy C. Smith (Texas Instruments, Austin, USA).

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 - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

As is the case with many published ESD design solutions, the techniques and protection solutions described in this data sheet are protected by patents and patents pending and cannot be copied freely. PowerQubic, TakeCharge, and Sofics are trademarks of Sofics BVBA.

Version

May 2011

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