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Outlook on ESD protection approaches for the emerging RF and high speed IC's in nanoscale technology nodes

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Keywords – ESD, CDM, multi-domain, System on Chip, VS-TLP, RF.

Introduction

While CMOS technology continues to evolve to smaller nodes, the demands for ESD protection get more challenging. Figure 2 and Figure 3 present the breakdown voltages for respectively gate-source and drain-source stress of an MOS device in different technology nodes. For both stress cases, the maximum voltage decreases in the advanced technology nodes. This indicates the need for high performance ESD protection structures. For example, the gate oxide thickness in the 65nm node is less than 13 Å, which limits the maximum transient voltage below 4V.

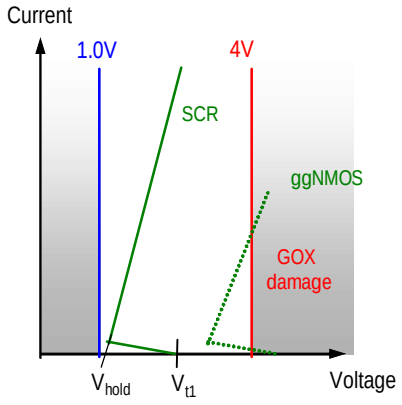

Figure 1: Traditional ESD approaches such as ggNMOS devices can not protect the thin gate oxide in 65nm technology. Silicon Controlled Rectifiers with low holding voltage present a solution.

This low voltage renders the classical ESD approaches useless as illustrated on Figure 1. For instance, to reduce the voltage drop over all the elements in a dual diode approach (See Figure 4), the devices need to be unrealistically wide. Local protection is a must-have. However, due to the increasing speed and ever more stringent demands of the applications, the ESD engineer faces an ever more complex job: ESD protection must go hand-in-hand with the development of high speed IO or RF circuits. Typical, RF Design people tolerate a maximum S-parameter account of the added capacitance of the ESD protection of only 100 fF. This low capacitance value can not be achieved through the use of the traditional ggNMOS protection, for years the workhorse for every ESD protection.

But this rapid decrease of the ESD design window does not only hold for input protection: output protection is as challenging as ever. Meanwhile the ESD specifications shift from HBM/MM towards CDM: extremely fast pulses with current amplitudes well over 10 Amps. Worse yet, there is no well established standard for CDM, nor is there a measurement equipment which can produce reliable and repeatable stress conditions.

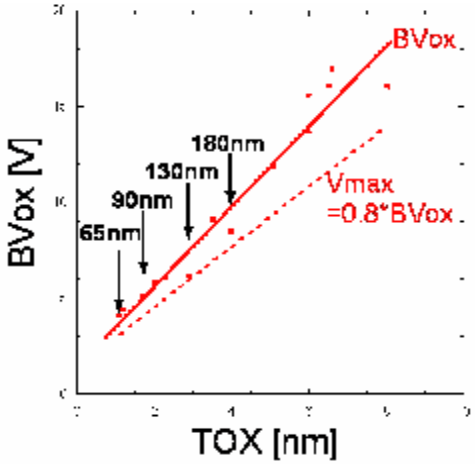

Figure 2: Decrease of oxide breakdown voltages during ESD stress for decreasing physical oxide thickness.

While the ESD engineer tries to find his way between these increasingly more difficult specs, using the newest equipment such as VS-TLP with pulse widths of only a few ns, the application engineers

pushes the boundaries of technology even further, with System-On-Chip (SOC) applications. Here many power domain interfaces create a new weakest link. Traditionally, ESD is all about protection for the I/O circuits. Not anymore: the multiple power supplies and multiple separated grounds give rise to stress cases where core failures are ever more immanent.

The cry for new ESD protection concepts was never as heart felt as it is today. Where ESD used to be a playground where creativity of many engineers created many, sometimes eccentric protection devices and concepts, today, in the very advanced technologies only a few possibilities are still standing. This talk provides an overview of these new challenges as technology reaches into the 45nm node.

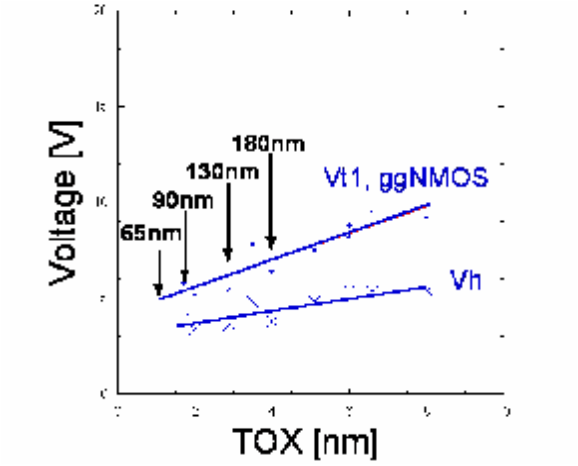

Figure 3: Decrease of trigger and holding voltages of GOX1 NMOS devices during ESD stress for decreasing physical oxide thickness.

The paper has 4 sections. The first section presents a detailed overview of the current ESD-protection approaches and their applicability for the most advanced technologies. The second section provides a look on the new and increasingly more difficult demands that the new applications and systems pose on the ESD protection. The third section discusses the trends in ESD protection requirements: the shift towards CDM, the new measurement equipment possibilities, etc. Finally, the fourth section concludes with a glance into the future.

1. ESD Protection strategies

Different ESD strategies exist, ranging from dual diodes with rail or snapback power clamp, over secondary protection, to full local protection. This section lists the different possibilities and their applicability for very advanced technologies is discussed. To add structure to the discussion, the focus is on the following 6 qualitative figures of merit (FOM).

1. A first figure of merit provides insight in the Scalability of the approach with decreasing Design Window (**SDW**). This FOM quantifies the lower limit: What is the minimum design window needed for the different protection approaches?
2. A second figure of merit presents the Scalability with different Technology Options (**STO**). Is the approach effective for Bulk, SOI, MugFET technologies, …?
3. An important Figure of merit is the ESD performance per Area (**EA**). According to the 2001 ITRS roadmap, the target for HBM performance per area is 4.0-4.5 V/um2 in 2005. After 2001, ESD dropped from the ITRS roadmap; such that the question of its feasibility remains. The higher this value the better, which means that a high ESD performance can be reached in a small area.
4. Fourth figure of merit is the ESD performance per parasitic Capacitance (**EC**). Without giving absolute numbers, how does the capacitance load of each solution look? The higher this value the better, which means that a high ESD performance can be reached with a small parasitic capacitance.
5. Fifth figure of merit is the ESD performance per added series Resistance (**ER**). Some approaches alter the normal operation mode by placing series resistance, either externally to the drivers to limit the voltage over the sensitive node, or internally into the drivers, to enhance their ESD robustness. Clearly, this is disadvantageous for the normal operation. A high value means that the ESD protection can be effective with only a small series resistance.
6. Finally the sixth figure of merit is the Correlation between different ESD Models (**CEM**). Currently high HBM and MM level are required, but the expected CDM level rapidly increases. How does the solution approach answer this shift?

The figures of merit are summarized in Table 1.

TABLE I

Summary of the different figures of merit

FOM	Abbr.	Explanation
1	SDW	Scaling of protection approach with decreasing Design Window
2	STO	Scaling of protection approach with for Technology Options
3	EA	ESD per Area
4	EC	ESD per parasitic Capacitance
5	ER	ESD per added series Resistance
6	CEM	Correlation between different ESD Models (especially HBM versus CDM)

The following subsections evaluate each of the protection approaches using the six figures of merit. Although the discussion focuses on input protection, it can easily be translated to the output protection case.

1.1 Dual diode

Figure 4 shows a typical dual diode protection. For positive stress between input and Vss, the current flows through diode up, Vdd-bus and power clamp. Each of these elements creates a voltage drop stressing the sensitive input node. This poses a limit created by the bus resistance. A 200V MM stress (3A peak current) creates a voltage drop of 3V over a bus resistance of 1 Ohm. This voltage drop consumes almost the whole available design window (4V) for the protection of a thin gate oxide in 65nm CMOS. This does not take into account the voltage drop over the power clamp. Regardless of the type of power clamp used (rail clamp or snapback based), this approach dramatically fails the first figure of merit, SDW. Realistically, at 3A, at least 2V over the diode up, 2V over power clamp and 3V over the bus resistance is assumed, presenting a lower limit of ~7V for this protection approach.

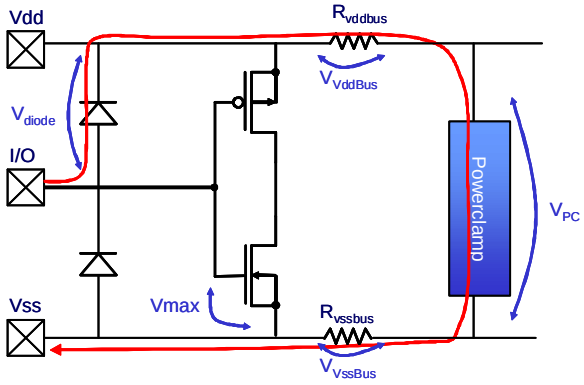

Figure 4: Dual diode protection approach. A large total voltage drop (Vmax) is created over the NMOS input gate for IO-pad to Vss stress cases.

If the critical voltage is below this value, a dual diode approach is not feasible. The availability of metal layers is crucial. In 90nm and 65nm technologies, interconnects (back-end) have a reduced thickness and pitch, which leads to an increase of the resistance and a lower current capability. G. Boselli states that the dual diode approach becomes inefficient for advanced technologies due to the large voltage drop over the P+/Nwell and N+/Pwell diodes [1]. These difficulties can be solved by large metal stacks used for buses, increased oxide breakdown for new high K dielectrics, …

How about the other figures of merit? The impact of different technology (STO) options is limited to the influence on the on-resistance of the protection elements, at least for rail-clamp based power clamp solutions. Whatever technology option is chosen, beit bulk, SOI or other exotic possibilities, MOS operation is always guaranteed, and spice models are available. For snapback clamps (Parasitic bipolar, SCR), the matter is much more complex, since the tuning of the typical snapback voltage and current levels require careful study for each process option. Concerning SOI technologies, recent publications presented the use of SCRs in SOI [2,3], while the snapback of MOS devices in SOI is also still possible. At this moment it remains unclear what will happen in more exotic process options: for MugFET MOS devices for instance, very poor performance has been shown [4], but optimizations are still to be tried out.

ESD performance per area (EA) is typically excellent, especially when many I/O cells are present in the IC. Area optimisation for the power clamp is in general more a concern for rail-clamp based solutions, due to the large MOS width and the large capacitance value needed. Recent publications [5] have shown excellent results with smaller capacitance value, such that the area is mostly determined by the MOS width. For the cited reference, this amounted to an area of 5600 um2 for 2kV HBM. Snapback based protection often reduces the area needed. For 65nm, Diode Triggered SCR (DTSCR) devices [6], shown on Figure 8, of 1000 um2 can achieve an HBM performance above 3 kV. This trend will most likely continue into the 45 nm node. It still remains unclear if this will still be true in advanced SOI technologies, as the reduction of the film thickness reduces the area gain possible when using parasitic bipolar (or SCR) devices. Recent publications [2] show that thickness of the film poses the ultimate limit to the current capabilities of the devices. If the total film thickness is used as a MOS channel, what gain can be found in using the parasitic bipolar?

The ESD per Capacitance (EC) can be very high in this approach. The total junction capacitance coupled to the IO-pad is low because only two junctions (diode up P+/Nwell and diode down N+/Pwell) are coupled to the pad. Moreover, diodes have the highest current capability per area, such that the required junction area and thus the capacitance are low. Furthermore, no resistance is added in the pad, optimal for ER.

For CDM a genuine problem occurs. For efficient CDM protection the voltage over the oxide must be clamped at all times which means local clamp is the best strategy. The resistance and inductance of the bus metal is too high to remove overstress from the oxide during the extremely fast transients (~1ns) and high current regime (+ 10A).

Because of the concerns raised for the first (SDW) and sixth figure of merit (CEM), the end of dual diode protection seems to be in sight. Additional improvements (lower resistive power clamps and diodes, more metal layers of the bus, high K

dielectrics, …) might arguably increase the dual diode approach lifetime up to the 65nm node, but further seems difficult. Only if the circuit designers can find ways to improve the speed of the application using GOX2 devices, dual diode might be around for one or two more technology nodes.

1.2 Secondary protection

A typical secondary protection scheme is shown in Figure 5. For output protection, the secondary stage can consist of self-protective drivers. Because this approach increases the design window, the first figure of merit (SDW) is easily achieved, however, with a serious penalty for normal operation: the series resistance makes it difficult to use for high speed/RF applications. This results in a low ER.

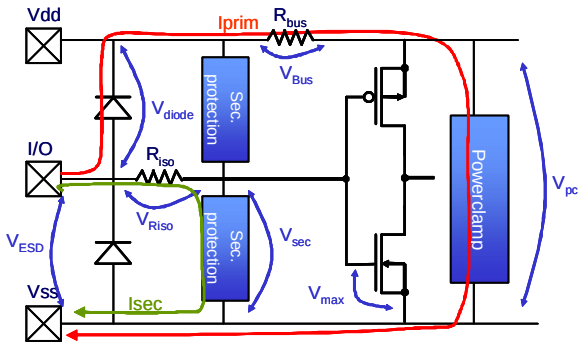

Figure 5: Secondary protection approach including the isolation resistance.

The ESD per area (EA) is very high, since the voltage drop over the diodes, power clamp and bus resistance is not crucial. The result is a current limited design approach for all clamps, except the small secondary protection stage.

ESD per Capacitance or EC-wise, this is a moderate solution: although capacitance is added in the secondary stage, it is limited since the secondary stage is usually very small. In combination with ER, the increased EC worsens the influence on normal operation. There is one notable exception: Active source pumping (ASP) as depicted in Figure 6. In this scheme, the isolation resistor is not placed between the pad and sensitive node, but rather between MOS source and Vss (or Vdd in case of pull transistors). The source of the MOS is pumped high during ESD by a small ASP circuit, usually a diode chain of ~10um wide. The added capacitance is minimal, while the added source resistance can be largely overcome by increasing the drive strength (i.e. the width) of the driver [7].

One of the key strengths of secondary protection is its reliability during CDM stress. Just as in HBM stress cases, the series resistance limits the voltage drop over the sensitive node. For input protection, the displacement current of the sensitive gate can already build up a much needed voltage drop over the series resistor. In order to have efficient CDM protection, a positive current path between substrate and PAD is preferably incorporated in this secondary stage. Charges flowing from, the Vss line through the isolation resistor limit the voltage drop over the oxide. Therefore CEM is expected to be high.

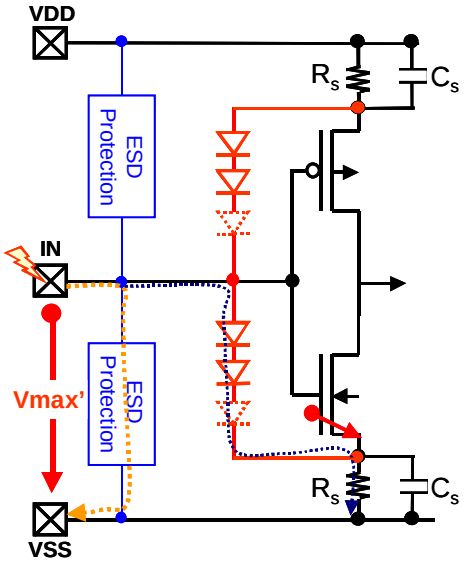

Figure 6: ASP protection approach for input pad

How will this approach evolve through the next technology nodes? In fact, looking only at technology aspects, this is an excellent solution: the design window decrease has no significant influence on its applicability (SDW), and whatever technology options are chosen, some schemes of secondary protection will remain efficient (STO).

However, as elaborated on in the second section, the question remains how IO designers will respond to ESD engineers that place large series resistance. Unless dramatic innovations in design techniques are showing up, this series resistance will not be allowed for most high speed or RF applications. Therefore, secondary protection will be struggling, and the end of secondary protection seems unavoidable. Not because of technology evolution, but rather because the applications change.

1.3 Full local protection

In the previous sub-sections issues are outlined for the dual diode protection approach due to technology scaling and for the secondary protection approach due to application requirements. This sub-section presents the last resort: full local protection (Figure 7).

Obviously, ESD per Area (EA) is high, since ESD clamps are added in all I/O cells. Although this is unwanted, the increased cost can be tolerated, if it enables further technology scaling while providing sufficient ESD protection. The main challenge is related to fitting the ESD protection elements into an

extremely narrow pad pitch of only 30um as is typical required for high pad count IC's. Since this requires multi finger devices, metallization of these structures is a hazard; Moreover, the emerging electro-migration (EM) rules for metal push the calculation of the metal width from ESD to EM based calculations!

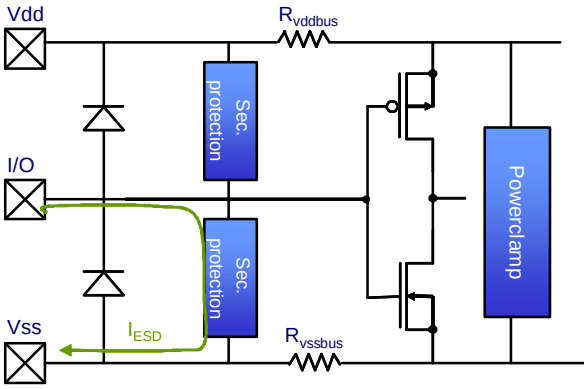

Figure 7: Full local protection approach

ESD per added Resistance (ER) is ok, since no series resistance is added at the IO pad. At first sight, the low ESD performance per added Capacitance (EC) reduces the applicability of this solution. Every junction connected to the pad adds capacitance. Looking at Figure 7, four large junctions are connected to the IO pad: diode up, diode down, ESD clamp 1 and ESD clamp 2. Clever ESD design and layout can save this approach. It is possible to keep the capacitance low through the use of bi-directional ESD devices. In the case of bi-directional SCRs, however, two junctions are connected to the pad, such that this does not lower the parasitic junction capacitance. A possible solution is to merge the ESD clamps 1 and 2 with both diodes. Such a solution has already been proposed by B. Keppens et Al. [8]. To limit the added capacitance, crucial is the ESD performance per perimeter, since increasing the perimeter increases the added junction capacitance.

To keep a good CEM, the CDM level must be high, requiring extremely fast clamps. Thus it comes down to: how to create fast triggered ESD clamps working within a few volts, whatever technology options are chosen. This is the genuine ESD challenge for the next years. For the 65 nm CMOS node, DTSCR devices can solve the issue. High protection levels are achieved (250 V Machine Model), effectively protecting thin gate oxide, within a limited area (<900 um2 per clamp). A measurement example is shown on Figure 9.

When looking at the SDW, the lowest possible limit is the holding voltage of the SCR (Vh < 1.2V). Triggering speeds down to 450 ps are reported [9], suggesting good CDM results can be achieved.

SCRs have the bad reputation of unpredictability when process parameters change (STO) to the extent that people believe SCR operation is incompatible with certain process options (e.g. SOI). This is however unjustified. O. Marichal et al. and C. Russ described in [2,3] how DTSCR and GGSCR [10] devices are successfully implemented in SOI technologies. However an ultra thin SOI film dramatically increases the on resistance of the ESD devices. It remains a crucial question whether the performance per perimeter, including a low enough on-resistance, will remain high enough to have acceptably low junction capacitances.

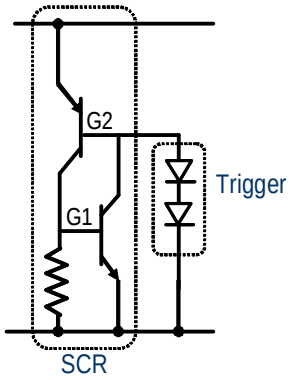

Figure 8: Generic DTSCR ESD protection clamp. The SCR device is triggered by the external diode chain, connected at the G2 junction.

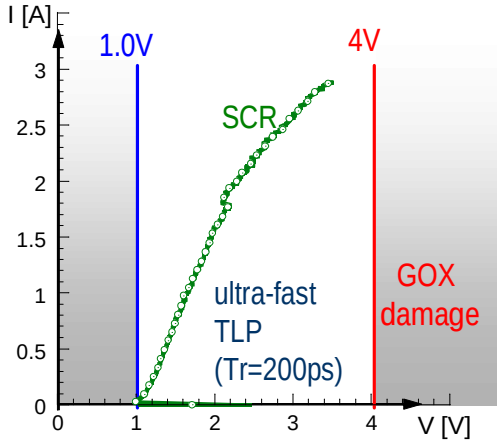

Figure 9: Effective thin oxide protection through the DTSCR, measured for fast rise time (200ps) and parallel gate monitor (GOX1 input in 65nm CMOS).

All in all, the full local protection approach holds the most promises to overcome the scaling challenges. An overview table for the three approaches is presented below (Table II).

TABLE II
Summary of the different figures of merit for the 3 protection approaches

Abbr.	Dual diode.	Secondary protection	Full local protection
SDW	Min 7V	OK	OK
STO	Simple	Simple complex	Complex
EA	High/moderate	Moderate	Low
EC	High	Moderate	Lowest
ER	High	Low	High
CEM	Difficult	Best	Better

2. Advanced applications

As mentioned above, next to technology scaling, the trends for the new applications impose high demands on the ESD protection. Two of these are further highlighted here: High speed applications and the SOC (System-On-Chip) challenges.

2.1 High speed/RF applications

While the frequency of the IO's is rising, a shift is dawning: where ESD used to be about fast transients of high current, it will become about slow transients of high current. With a rise time of ~10 ns, HBM is within the Gigahertz range, although the main energy remains within the Megahertz range, since the total duration is about 1 us. Any signal coming into the chip at this frequency can be labelled "ESD", that is, as long as the normal operation signals are significantly slower or faster. High- and/or low pass filters can be used to detect ESD. But what happens when the frequency of ESD and normal operation are comparable? What is the frequency of ESD? Does the 10ns rise time of HBM present a good standard, or is the much faster rise time of CDM events more appropriate (~100 ps)? A more detailed discussion of the CDM shift is presented in the third section, but at this point it is clear that a frequency range is required to characterize ESD. From relatively slow ESD (MM, rise time ~20 ns, total duration ~1 us) to very fast (CDM, ~100 ps, total duration ~2 ns), the frequency range is calculated as 50 MHz – 10 GHz. This is a large range which explains much of the difficulties for using filters as ESD protection. These filters are mainly useful to protect a chip against one specific ESD model. The low pass filters can easily be used for supply protection since there are no AC signals during normal operation.

For applications above the 10 GHz border, new ESD protection approaches are possible. A high pass filter in series with the input IO blocks every ESD event. For lower frequencies, the reverse is true. Of course these "filters" need to be able to shunt a lot of ESD current.

For applications working with a smaller bandwidth, such as LNA's, this filter principle can be used easily, as was described by [11]. Instead of minimizing the capacitance, the capacitance value is used in the LNA calculation to achieve the desired matching (co-design). This is a very promising technique, as it solves the trade-off between low capacitance and high ESD protection. This means that the ESD per Capacitance (EC) figure of merit, as discussed in the previous section, is less critical for a range of applications. But it is only one example of so called co-design where the ESD protection parasitics are taken into account, and used in the calculations for normal operation performance [12].

2.2 System-On-Chip (SOC)

The trend for more functionality within one application leads to the development of SOC and NOC (Network on chip) applications. Typical for these applications are multiple power domains and long bus routing. For ESD, this trend brings about a shift in focus from IO failures to core failures. Figure 10 shows the root cause of the problem: the interface between two power domains is easily exposed to a high voltage drop due to inter power domain protections and high bus resistances. This is most pronounced during CDM stress where the chip is charged to a high voltage. If a time Δt exists between triggering of 2 power clamps, the interfaces between these two power domains are exposed to a high voltage drop, and core failures are likely. In SOC applications, a multitude of these interfaces exist. With the different domains, different grounds are associated, buffered with anti parallel diodes for noise isolation. Different ground architectures are possible, all having consequences on the ESD performance, especially CDM.

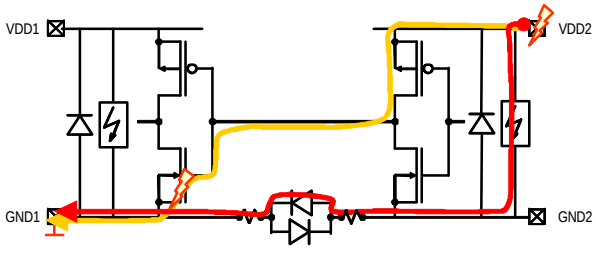

Figure 10: Core failure in multi domain IC's for ESD stress combinations over 2 domains. The total voltage drop over Vdd2-power clamp, anti-parallel diode and bus resistance is higher than the breakdown of the GOX1 oxide and the PMOS breakdown voltage.

This calls for a dramatic shift in focus for ESD protection. In the past, core failures where solved by adequate power clamping. Some techniques to avoid inter power domain interface failures exist, but they are limited in number and in usage [13-15]. ESD is known mostly about adding protection elements in the IO cells. The area increase associated with ESD protection is often translated into IO pitch. But as more functionality is added to the chips, and as SOC brings new territories, the relative importance of small IO cells decreases. Therefore the area specifications at the IO side for ESD protection can be relaxed. Where it is more critical, however, is in the core: in the interfaces between the power domains. Many of these interfaces exist in SOC, and the non-obvious metal routing increases the ESD analysis complexity dramatically. Yet each of those needs to be studied in order to avoid ESD failures. ESD engineers will increasingly need to work within the core of the chip. Finding long signal lines that connect different power domains is a painstaking job, however, it seems at this moment, no other solution exists.

3. The CDM shift

It is clear that CDM is gaining importance. Most field failures today are believed to be associated with CDM. Although there is a long list of publications about CDM, many designers still see it as black magic. There is a need on breakthrough research on the study of high transient (CDM-like) effects. A first step is to include the VS-TLP in the ESD analysis phase.

The VS-TLP provides unique possibilities [16,17]: with rise times as small as 100ps, and a pulse width of a few nanoseconds, an IV curve in the CDM-time domain can be measured for different devices, sub-circuits and full applications. These measurements will never replace the CDM testers, however, since it still consists of a completely different stress case. CDM is a one pin, VS-TLP a two pin test. During CDM the chip is charged up, and every device, every ‘well’ contributes to the overall performance. This is not the case for the VS-TLP test. Yet the major contribution of the VS-TLP is the ability to measure and analyse the high current, high transient behaviour of different current paths. It allows to benchmark different protection devices. It creates a base for comparison of on-resistance, triggering speed, current capabilities and voltage drops, all in a CDM-time domain. These measurements were impossible previously. The new possibilities mark a turning point in the short history of ESD protection. Where HBM and MM used to reign supremely, because no tools were available for adequate analysis of CDM performance, the sceptre can now be handed over to CDM, known for its black magic nature and unexpected failures. But characterisation of products with a CDM level remains problematic despite all VS-TLP efforts. The correlation between socket and non-socket testers remains an issue. Different studies [18-20] have been performed in this respect, generally concluding that socket testers have the advantage of higher test turn over and being more severe according to some, however, correlating less with real world failures as compared to non-socket tests. This makes sense, since the non-socket dead-bug test physically resembles the real world more adequately: the same capacitances (i.e. package capacitance and Vdd-Vss core capacitances) play the same role. For the socket case, the tester capacitance and inductance are involved, averting from the real world. The relevance of socket CDM testing is unclear. For charging of the device, also two methods are applied: pin charging or field induced charging.

Generally, during the charging phase of the CDM test, large package capacitance present a worst case, as it directly relates to the number of charges stored inside the silicon. During the discharging phase however, the larger package capacitance slows down the pulse, relieving part of the “worst” case nature of the large capacitance. This dubious role of package capacitance complicates analytical study even further.

But can the course of industry and specifications within the next years be predicted? Will the nano-physics bring about more boundaries, or will some of the challenges of today fade away? Smaller device dimension increase the trigger speed and allow faster reaction to CDM threats. This has advantages (creating ESD protection to trigger within 1ns will be easier) and disadvantages (the sensitive nodes will also respond sooner to over stress cases).

4. Conclusion

With technology closing into the 45nm node, the ESD protection principles are thoroughly changing. The classical dual diode approach is vanishing rapidly, leaving only full local protection to save the sensitive nodes. For bulk technologies, the DTSCR seems to have a bright future; it has been verified in multiple 65nm technologies, and there is no reason to suspect that it will not be around for then next nodes. For SOI, the DTSCR has also been proven to work, although the area penalty is much higher than in bulk. But what other technology options lie ahead? Maybe high k dielectrics will allow a larger design window? What about bus resistance? Is there still room to improve the back-end such that, although thinner metal lines are used, the resistance can be decreased? And what will the new applications bring? With the frequency shift in sight, co-design promises to be the next big solution approach for RF and high speed interfaces.

Meanwhile, more attention is being drawn by CDM, as exciting new measurement equipment promises to turn the black magic of CDM into an analytical domain, with CDM optimized clamps as expected outcome.

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ESD SOLUTIONS AT YOUR FINGERTIPS

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

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