Conference paper

Using the Voltage and Current Waveforms from VFTLP systems to study transient device behavior

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The Transmission Line Pulse (TLP) test system has long been used as an analysis tool to complement the pass/fail HBM and MM qualification data. Recently a new TLP system (Very Fast TLP-VFTLP) has become available, which uses much shorter pulse durations (1-10 ns) and much faster rise times (100-200 ps) than the conventional TLP system (typically 100 ns and 10 ns respectively). This VFTLP system opens up new possibilities for studying the ESD protection device behavior in the nanosecond time domain, including characterization of turn-on time and voltage overshoot. However, the analysis of the results obtained by a VFTLP requires a deeper understanding. This paper provides an overview of the possibilities, the pitfalls and the constraints, as well as new insights regarding the interpretation of the VFTLP measurement data.

Using the Voltage and Current Waveforms from VFTLP systems to study transient device behavior

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Abstract – The Transmission Line Pulse (TLP) test system has long been used as an analysis tool to complement the pass/fail HBM and MM qualification data. Recently a new TLP system (Very Fast TLP - VFTLP) has become available, which uses much shorter pulse durations (1-10 ns) and much faster rise times (100-200 ps) than the conventional TLP system (typically 100 ns and 10 ns respectively). This VFTLP system opens up new possibilities for studying the ESD protection device behavior in the nanosecond time domain, including characterization of turn-on time and voltage overshoot. However, the analysis of the results obtained by a VFTLP requires a deeper understanding. This paper provides an overview of the possibilities, the pitfalls and the constraints, as well as new insights regarding the interpretation of the VFTLP measurement data.

I. Introduction

For ESD characterization, different levels of analysis can be defined, briefly outlined below.

(1) Level 1: System compliance. System manufacturers that commercialize complete consumer electronic systems (e.g. a complete mobile phone) need to comply to certain technical standards [1-3]. The system level ESD compliance (IEC 61000-4-2) is one of such tests and requires Air & Contact Discharge stress to be applied on the system. These compliance tests are required to ensure functionality during the lifetime of the product, where the system is stressed by the user. A typical waveform and measurement setup is shown on Figure 1 [4].

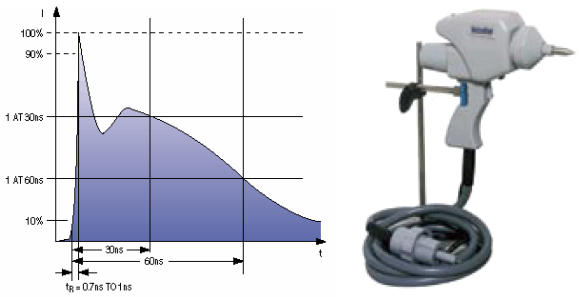

Figure 1: Typical current waveform for contact discharge into a short circuit. The waveform has a fast rise time (<1ns) and high current level (30A for 8kV)

Since the user environment is not controlled, severe ESD stress can occur during the lifetime of the system. Therefore, the system level compliance tests are designed to be equally severe. The current amplitude injected into the system can be as high as 30 ampere for the first current peak for a typical 8kV test.

(2) A second characterization level is related to the components within the system. Every IC in the system is qualified for ESD robustness using the traditional Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM) test equipment [5,6,7]. This IC product qualification ensures that the components can be transported safely from the fabrication plant to the system manufacturer and are protected against Electro-static Discharge events through packaging, handling and mounting during the system construction. Since the system construction typically happens in an ESD-safe (controlled) environment, the stress is much less severe as compared to the system compliance (Level 1). Figure 2 depicts the three main product IC qualification tests.

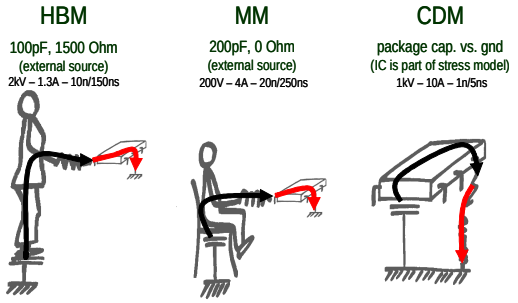

Figure 2: Three main IC qualification test models: Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM).

The main drawback of the first two characterization approaches is the limited amount of data that results from these tests. Both level 1 and level 2 only provide 'Pass'/'Fail' data. 'Pass' means that the functionality of the system has not changed after the ESD stress and 'Fail' means that the system or IC has been damaged. Although a post-stress leakage current measurement can be used to investigate the damage, it is difficult to

learn from such measurements. For a complete understanding, an ESD relevant IV characteristic is required. Such analysis can not be done with standard DC characterization tools such as the curve tracer or parametric analyzer because the long stress time (millisecond time frame) leads to self heating at high current stress levels, destroying the device under different conditions and thus with a different failure mode.

(3) To address this issue, the Transmission Line Pulse ('TLP') tool was introduced by Maloney in 1985 [8], where the device/IC is stressed with rectangular pulses featuring an ESD compatible, short pulse duration (~100ns) and increasing current amplitude. The TLP system creates an IV characteristic with ESD relevant time and current levels [9-11]. An example of such TLP-IV curve is shown in Figure 3. It consists of a number (N) of discrete IV coordinates. To create the 'quasi-static' TLP IV curve, the TLP system defines average voltage and current values. These average values are calculated for each applied stress pulse based on a pre-defined 'Averaging window' in a stable (quasi-static) region of the transient waveforms. An example is shown on Figure 4. Each IV data point of the TLP-IV curve (Figure 3) is created from a voltage-current transient waveform pair, summarizing the so-called 'quasi-static' device behavior. More details about the averaging window is provided in the next chapter.

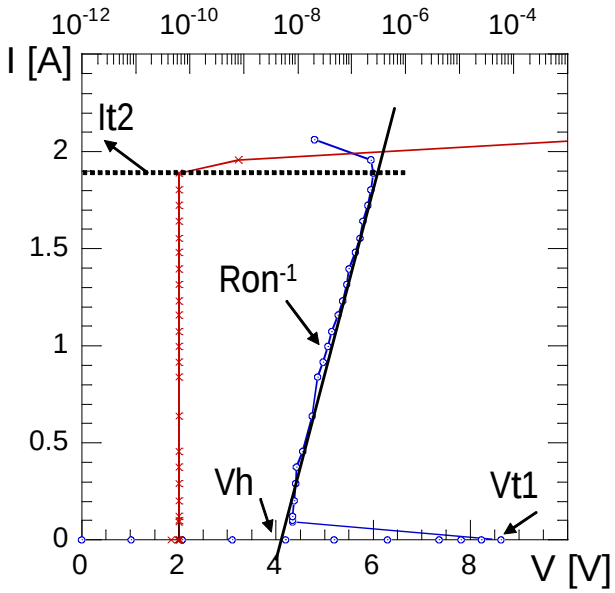

Figure 3: TLP IV characteristic for a ggNMOS device. Important triggering (Vt1), clamping (Vhold, Ron) and failure (It2) parameters can be easily read from the IV curve.

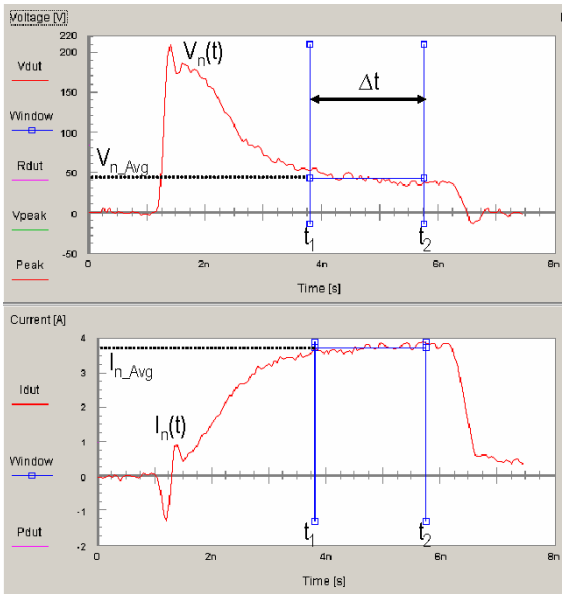

Figure 4: Voltage and current waveforms of a TLP system for a certain stress level. The averaging window is shown. Between the two vertical markers, the average voltage and current are calculated and combined to a single IV coordinate in the TLP IV characteristic.

While the TLP-IV curve adds a lot of important and ESD relevant information about the device under test, the transient behavior, which is basically available from the TLP waveforms (Figure 4) is not used at all.

(4) Finally, the 4th level of ESD characterization solves that problem and allows analysis of the complete transient data of the device. Waveforms such as those depicted on Figure 4 are used to study the transient behavior of the ESD devices. The VFTLP system TDR approach with separate incident and reflected pulses was first introduced for ESD purposes by Horst Gieser in 1996 [12]. Since then numerous studies have been made about this tool [13-17] related to accuracy improvements as well as providing short pulse duration device data [18-25].

This paper first discusses the definition and importance of the averaging window for IV creation and provides a simple method to judge the quality of the averaging window. Next, different methods are provided to analyze the transient device behavior such that the best ESD protection clamp can be selected. Turn-on time, voltage overshoot and dynamic resistance are investigated.

All the measurement data in this paper is created using the Barth Electronics 4012 VFTLP system. However, the analysis can be performed with any (VF)TLP system, provided that the transient waveform data is available. Measurements shown further are based on a High Voltage (HV) DMOS process technology. Silicon Controlled Rectifier devices with different Anode Cathode distance (LAC) are compared. The waveform analysis is performed using a custom designed analysis

tool created in the Agilent Vee Pro development environment [26].

II. The Averaging window

To create a TLP IV characteristic, the transient waveforms voltage $V_n(t)$ and current $I_n(t)$ of the n-th stress point are 'summarized' into an average voltage V_{n_avg} and an average current I_{n_avg} as shown on Figure 4. The averaging window is defined by the two time values (t1,t2) between which the average values are calculated. It is important to realize that the averaging window needs to be selected over a time range where the transient waveforms are stable. The next example shows that a wrongly selected averaging window can misguide design engineers into wrong conclusions.

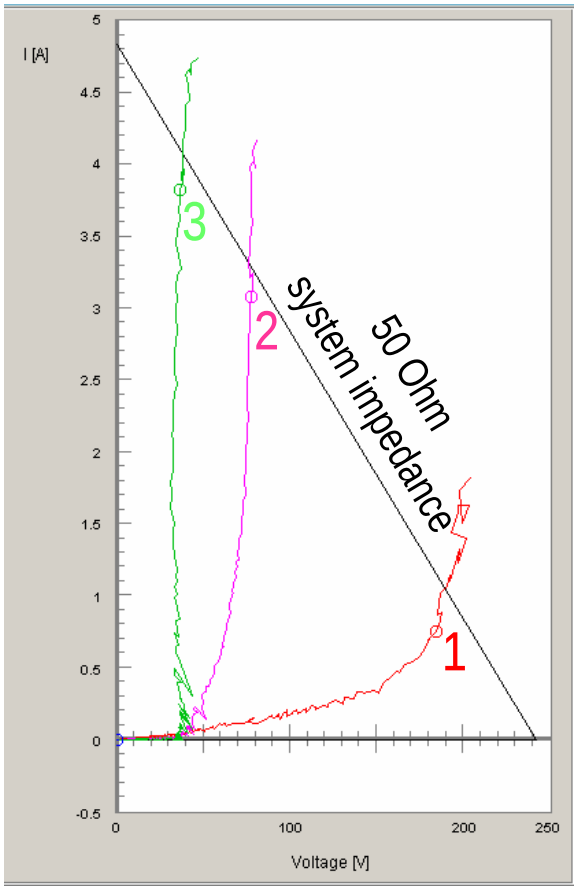

Figure 5: Comparison of three IV curves for SCR devices, all measured using 10ns pulse duration and 100ps rise time. From the curves, it seems that device '3' is the best clamping device since it has the lowest trigger and holding voltage and the highest failure current. But is it really true?

On Figure 5, three IV curves are compared. It seems that device '3' is the best choice for ESD protection. However, contrary to what most people expect, the three curves are all based on the same transient measurement data sets, same device, same test conditions. The only difference between the three IV curves is the selected averaging window.

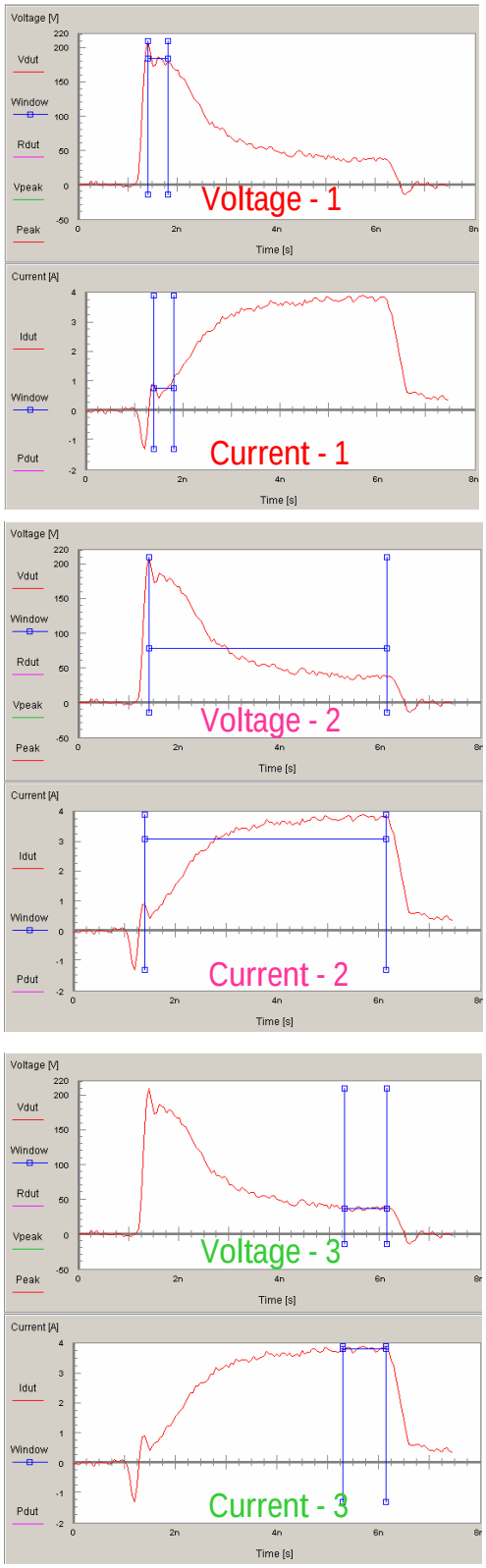

Figure 6: Voltage and current waveforms for an "under designed" SCR device ('4LAC'). Three different averaging windows have been defined: (1) covering the first part of the waveforms, (2) covering a large part of the waveform, (3) covering the tail of the waveforms.

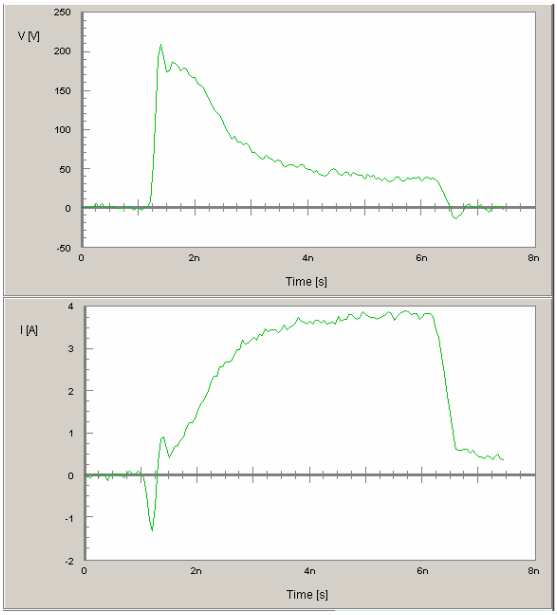

Figure 7: Voltage and Current waveforms from the VFTLP measurement on the SCR device for the selected pulse voltage, corresponding with the load line displayed on Figure 5 (pulse voltage of 121V). Through the use of three different averaging windows, three IV characteristics are created from the same Voltage and Current transient waveforms.

Figure 6 shows the three different averaging windows used to create the IV curves of Figure 5.

- IV curve '1' shows the device behavior for the first nanosecond. Using this averaging window, the IV voltage is exaggerated (overshoot) and the current level is lower.
- IV curve '3' summarizes the transient V(t) and I(t) at the end of the pulse where the waveforms are quite constant. For this averaging window the waveforms reach a 'quasi-static' state.
- Averaging window '2' is the worst option since the averaging window is obviously covering a non-stable transient waveform.

It is easy to judge the quality of the averaging window by eliminating the time from the V(t) and I(t) waveforms and creating an I(V) curve using the transient data of a single waveform pair. Such a virtual IV curve is shown on Figure 8 for the averaging window '2'. On this virtual I(V) curve, represented by the dots on the figure, averaging window problems can be tracked easily. When the voltage and current spreads over a large region, it means that the averaging window is too wide. On Figure 9, for another device, the averaging window is selected in a more appropriate way.

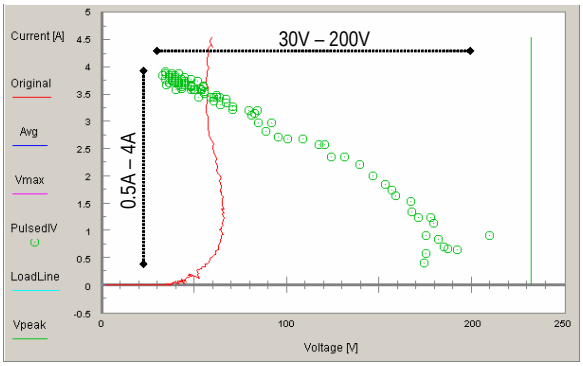

Figure 8: The dots represent a virtual IV curve created from the pulse shown on Figure 6, using averaging window '2'. The IV-dots spread from 30V to 200V and from 0.5A to 4A. Such a big spread in both voltage and current can not be considered as 'quasi-static' behavior. The 'dotted' I(V) generated from the V(t) and I(t) represent a quick way to check the quality of the selected averaging window.

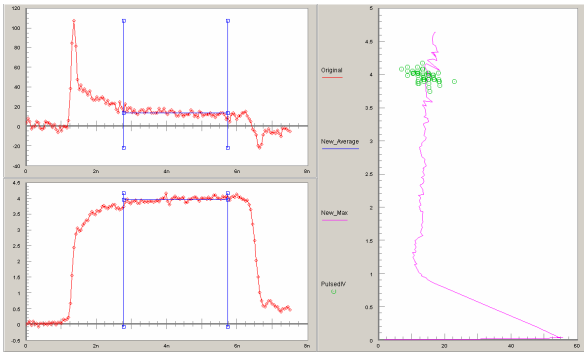

Figure 9: On the left side, the voltage (top) and current (bottom) waveforms are plotted together with an averaging window over a stable region. On the right side, the resulting 'virtual' IV curve, represented by the dots, shows that the average window is indeed selected correctly.

For very short pulses (VFTLP), a too broad or not well chosen "averaging window" easily leads to an IV-curve for which (1) voltage values are overestimated, and (2) current values are underestimated. This results in an IV-curve which is shifted both rightwards (higher voltages) and downwards (lower currents). The consequences are that

- the trigger voltage Vt1 is estimated too high
- the trigger current It1 is estimated too low
- the failure voltage Vt2 is estimated too high
- the failure current It2 is estimated too low.

Due to a "wrong" averaging window also snapback -an important indicator of device triggering- can become invisible. An example of the hidden snapback can be seen for curve '1' on Figure 5. On this curve, no snapback is visible while the voltage and current transients (Figure 7) suggest that a snapback occurs.

There is always a trade off in selecting an averaging window: Selecting a large (delta time) averaging window smoothes the resulting IV-curve by canceling

out the noise on the waveforms but increases the risk of non-quasi-static behavior inside the selected averaging window. On the other hand, selecting a small averaging window introduces more noise onto the IV-curve.

The load line, shown on Figure 5, represents the characteristic TLP system impedance of 50 Ohm, drawn for a certain initial pulse voltage. The IV points (dots on the figure) from the three curves are all related to the same initial TLP pulse voltage and thus exactly follow the characteristic output impedance of the TLP system. In a snapback event, the IV curve follows the TLP load line as is also visible on the virtual IV of Figure 8.

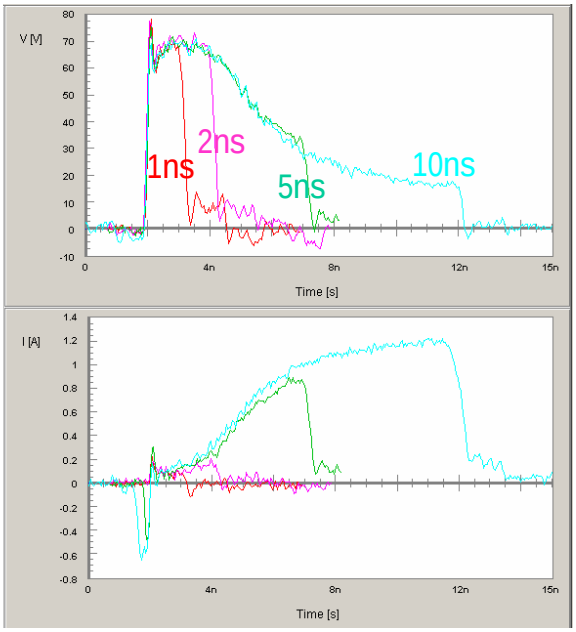

Figure 10: Comparison of voltage and current waveforms for an SCR device, VFTLP stressed with different pulse durations (1,2,5 and 10ns). Pulses for the same initial pulse voltage are compared (Pulse Voltage = 42V). Waveforms are perfectly overlapping as expected. A VFTLP measurement with a 10ns pulse duration can be used to 'replicate' the 1,2 and 5ns waveforms for low current levels.

The next chapters present different ways to compare ESD clamp devices, using the transient voltage and current waveforms, such that the most optimal device can be selected.

III. Transient waveform comparison of devices

The transient voltage and current waveforms can be compared for different pulse widths. On Figure 10, waveforms for a "deliberately slow" SCR device ('4LAC'), stressed with different pulse durations are plotted on the same graph. A fixed pulse voltage is used for all pulse durations shown in the plot. The pulse voltage corresponds to the charging voltage applied at the TLP cable. The initial parts of the transient waveforms are overlapping perfectly as shown on the figure.

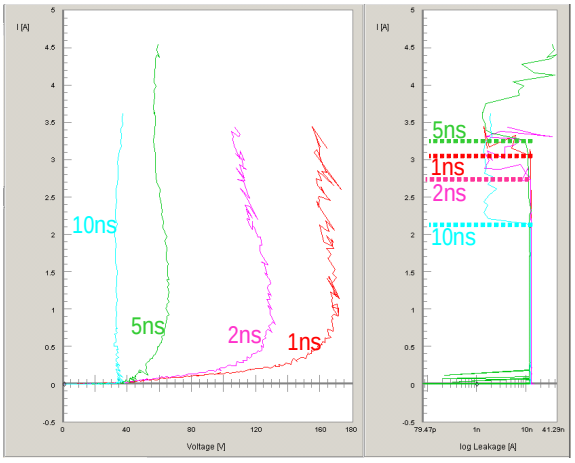

Figure 11: TLP IV curves for the same SCR device, measured using different VFTLP pulse durations (1,2,5 and 10ns). From the curves, it seems that the device behavior is completely different for different pulse widths. This is explained by the slow reaction time.

This means that the 10ns transients can be used to investigate the device behavior for the 1ns timeframe as well, as long as the device does not reach the failure current. On the graph it is also clear that the device trigger time is quite large. The device requires more than 5ns to reach a stable 'holding voltage'. Only for the 10ns pulse a quite stable part can be defined at the end of the pulse waveform. For the other pulse widths, any averaging window covers non-quasi-static behavior.

On Figure 11, the IV and leakage curves are plotted for the same SCR device, stressed with different VFTLP pulse durations. At first sight, the IV-curves on Figure 11 suggest that the failure current It2 for 5ns (~3.3A) is higher than the It2 for shorter pulse durations (1 ns: 3A, 2 ns:2.8A). However, though they are very typical for VFTLP, these results are somewhat deceptive. When comparing the same device for different short pulse durations it is physically impossible that a shorter pulse duration leads to a lower failure current. Indeed, the beginning part of the short pulses (1 ns, 2ns, …) should be exactly the same as the beginning part of the longer pulse duration (5 ns) as is evident from Figure 10 and Figure 12. Therefore, the longer pulse duration always represents a more severe kind of stress, and typically results in a lower It2.

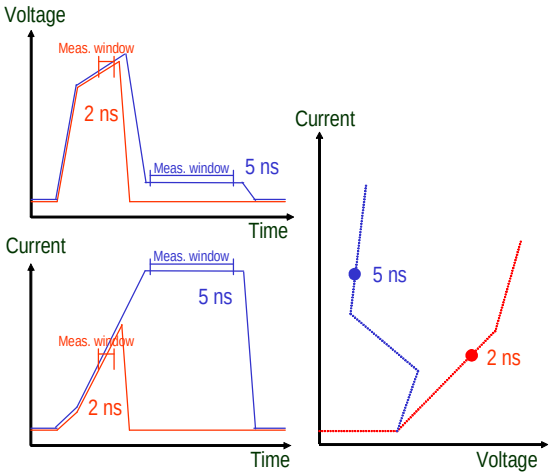

Figure 12: Schematic representation of VFTLP waveform measurements for a 2ns and 5ns pulse on the same device, with the same stress condition (same pulse voltage on the TLP cable). When the device trigger turn-on time is large (slow device), the IV characteristics differs completely for different pulse widths. In this example, the averaging measurement window is defined at the end of the pulses, leading to completely different IV data points.

Figure 12 provides a schematic representation of the problem of defining an averaging window for slow snapback devices. In the example, the device reaction time is larger than 2ns. This means that the measured average voltage at the end of the 2ns pulse is much higher than the average voltage in the case of the 5ns pulse width. Contrary, the current level is smaller for the 2ns pulse because the device is not turned on yet. This same behavior is confirmed on the IV characteristics (Figure 11) of the '4LAC' device stressed with VFTLP stress using different pulse durations (1,2,5 and 10ns). It2 values obtained from different averaging windows cannot be compared without caution.

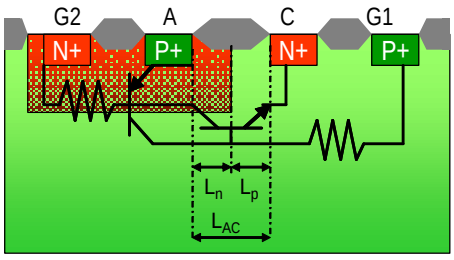

Figure 13: Basic SCR cross section used for the analysis of the SCR trigger behavior. Three variations are compared, each with a larger LAC - anode cathode spacing. The Reference device 'Ref' uses the process Minimum Design Rule ('MDR') value, while '2LAC' uses two times this MDR value and '4LAC' use four times this MDR value. For a larger anode cathode spacing the trigger speed is lower.

In the following example, three SCR devices, processed in the same HV DMOS process technology, are compared. All three SCR's are triggered at the Nwell/Pwell breakdown voltage. The only difference between the three devices is the anode cathode spacing. The 'REF' device uses the Minimum Design Rule (MDR) distance between Anode and Cathode. For the '2LAC' and '4LAC' devices this distances is doubled and 4 times as large respectively.

Theoretically, the SCR device with the largest Anode Cathode spacing should be the slowest device since the speed of the parasitic bipolar NPN and PNP devices reduces with a larger base width. A slower SCR device leads to larger trigger voltage, larger holding voltage, and possibly reduced It2 failure current [27].

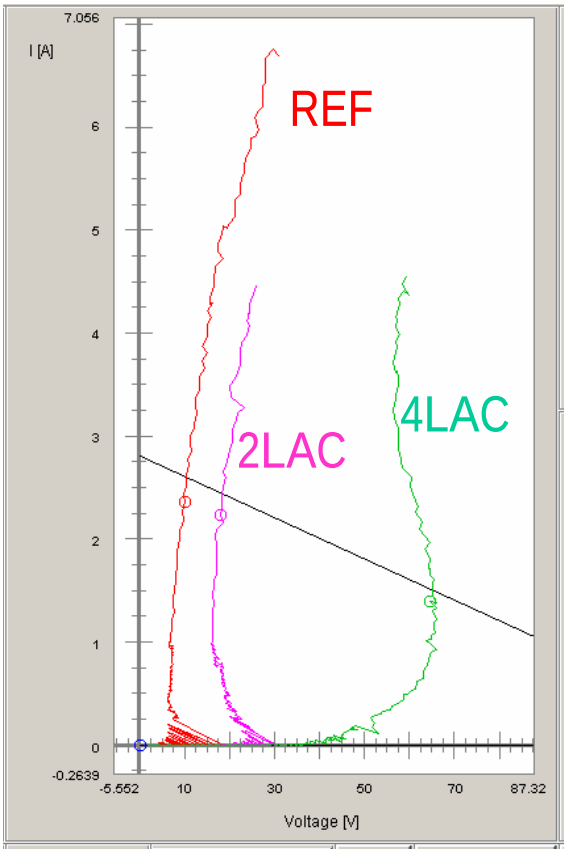

Figure 14: TLP IV curve comparison of three SCR devices constructed with ever increasing anode cathode spacing 'LAC'. The dots on the curves and the load line represent data for an initial TLP pulse voltage of 70V. The corresponding voltage and current waveforms are plotted on Figure 15. The device with the smallest LAC ('REF') has the lowest trigger and clamping voltage and highest failure current.

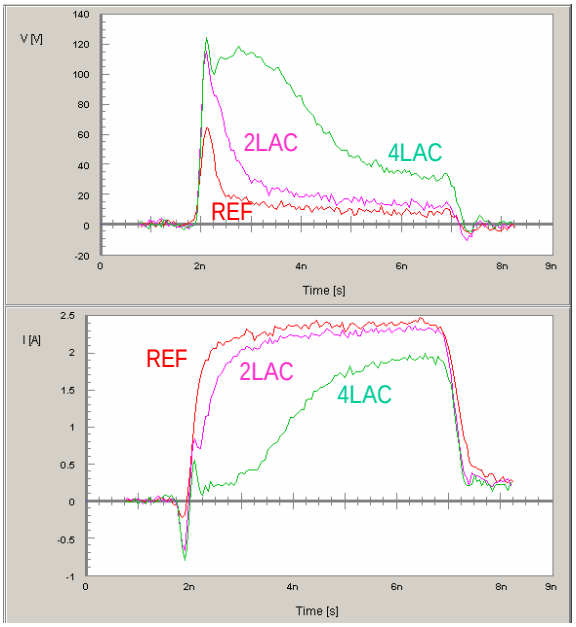

Figure 15: Voltage and current transient waveforms for three SCR devices stressed at the same initial pulse voltage. From the transient voltage and current waveforms a number of conclusions can be made: The transient overshoot voltage (initial part of the pulses) and the holding voltage (at the end of the pulses) increase with the anode cathode spacing. Also the time between triggering and clamping is larger for the 4LAC device.

The IV curves shown on Figure 14 and the waveforms on Figure 15 confirm the theory. The '4LAC' device clearly has the highest trigger voltage and holding voltage. From the waveforms it is evident that the time required to trigger the device into a low clamping voltage is larger for the device with larger LAC. While the '4LAC' device requires more than 2ns to trigger into the clamping state, the 'REF' device is turned on in less than 500ps. This is a very low value considering that the SCR does not use a dedicated external trigger circuit.

Important to note is that the trigger time is not a fixed number for a device. The trigger time is strongly dependent on the applied stress amplitude as shown on Figure 16. Voltage and current waveforms for different applied TLP stress voltages are compared. At higher TLP stress currents, the time between triggering and clamping is reduced. This is visible in the leftward shift of the rising edge of the current transient waveform for higher pulse stress voltages. This trend can lead to window effects if the failure mode of the protected node is strongly time dependent. This 'window' effect means that the device can for example survive a single 3000V HBM stress event but fails at 2000V when a complete step stress test is performed.

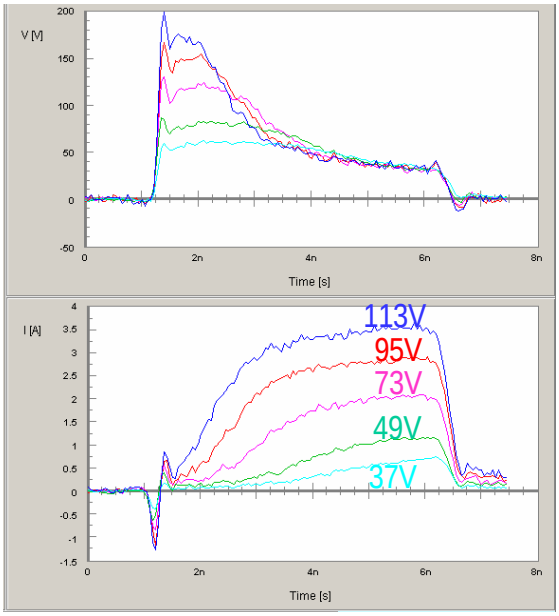

Figure 16: Voltage and current transients for a '4LAC' SCR device for different applied stress pulse voltages. On the transients it is clear that the trigger time or turn-on time is not a fixed number but rather depends on the applied stress current.

IV. Dynamic clamp resistance

Another way to compare the device clamping behavior is to use the transient or dynamic resistance R(t) = V(t) / I(t). An ideal ESD clamp (Figure 17) has an infinite resistance during normal operation to limit the leakage and signal loss. On the other hand, during ESD, the ideal clamp has zero resistance and thus no voltage drop. The ideal clamp can change from the high impedance mode to the low impedance mode without delay. The ideal clamp can be compared to a 'lightning fast' switch: open during normal operation, closed during ESD stress.

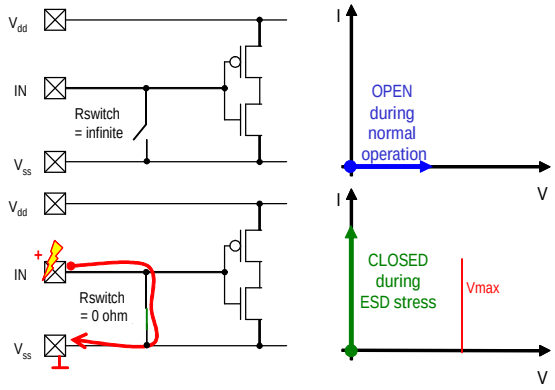

Figure 17: The ideal ESD clamp is represented as a switch. (1) During normal operation (above), the resistance is infinite. No leakage current flows from IN to VSS. (2) During ESD stress, the switch acts as a short circuit (R=0 Ohm), shunting all ESD current without voltage drop.

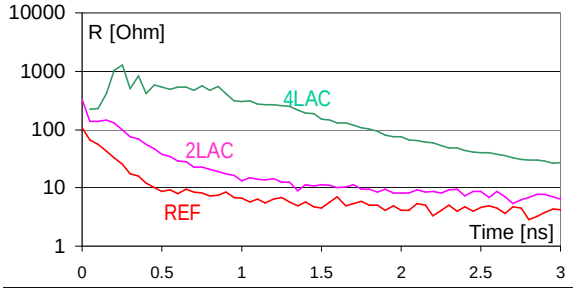

Figure 18: Dynamic resistance plot (logarithmic vertical scale) for three HV SCR devices with different anode cathode spacing. At the start of the timescale, the device triggering has just started. This is visible as a high impedance. Further down in the time, the resistance drops and saturates to a value around 10 Ohm. It is clear that the 4LAC device is the worst ESD clamp since the dynamic resistance stays high for a long time, leading to a large and long transient voltage overshoot.

Of course an ideal ESD clamp does not exist. All actual clamps introduce an amount of leakage current during normal operation. This can be easily checked through the use of a parametric analyzer. The resistance during ESD can be derived from the TLP-IV characteristic, provided that the averaging window covers a stable region in V(t) and I(t) transient waveforms. Defining the 'delay' between the high impedance state and the low impedance state is more difficult. With the right tool and complete voltage and current transient waveforms a dynamic resistance plot can be generated, plotting the R(t) = V(t) / I(t) for all time sample points.

The plot on Figure 18 presents this data for three SCR devices with different anode cathode distances. The device ('REF') is the best ESD protection clamp since the dynamic impedance drops to a lower value and is able to perform this voltage reduction faster than the two other devices ('2LAC' and '4LAC'). A larger dynamic resistance leads to a higher transient voltage drop over the ESD protection clamp. This is dangerous for sensitive devices in parallel with the ESD clamp.

The transient voltage overshoot is studied in more detail in the next chapter.

V. Transient voltage overshoot

When an ESD stress pulse is applied to a device, the parasitic capacitance (and/or test board capacitance) is charged up. The transient voltage level rises as long as the device is not triggered into the on-state. Once the device is triggered, the voltage drop over the capacitor and device can be reduced.

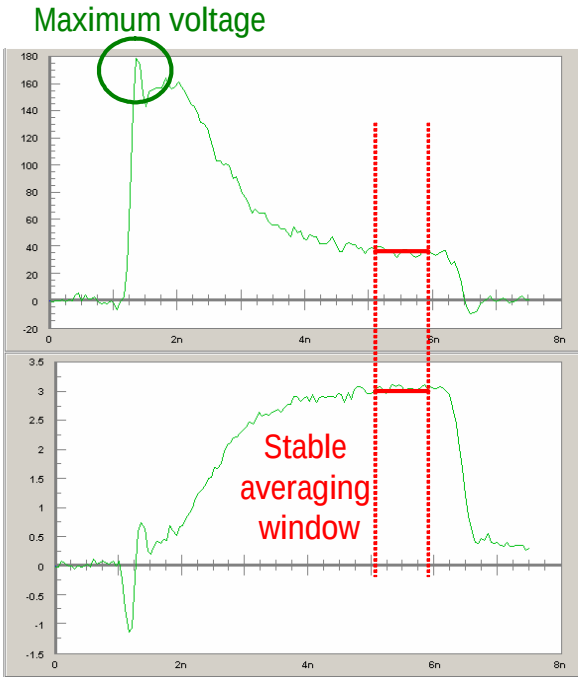

Figure 19: Voltage and current waveforms for a 4LAC device. Two IV characteristics are defined: (1) an averaging window definition at the end of the pulse where the voltage and current values reach a stable, quasi-static behavior. (2) the maximum voltage, depicted by the circle versus the average current from within the selected window.

For ESD clamps, a time difference can be defined between the moment the trigger condition is reached and the moment the clamp is triggered into the low ohmic state. The transient voltage and current waveforms can be used to investigate this turn-on time.

The VFTLP IV curve actually summarizes the current and voltage behavior of the device under test towards the end of the pulse, by averaging the current and voltage waveforms for different pulse voltages. However, in many cases the failure of the device under test is due to overshoot of the voltage, which happens at the beginning of the pulse, and which is not included in the derived IV-curve. Therefore another plot is proposed: Voltage overshoot ($V_{overshoot}$) versus pulse voltage (V_{pulse}). This provides more insight into the clamping speed of the device under test. By comparing different devices, and different rise times, in a $V_{overshoot}$-V_{pulse} plot, the ESD designer can learn about the device behavior during the initial moments of the ESD pulse.

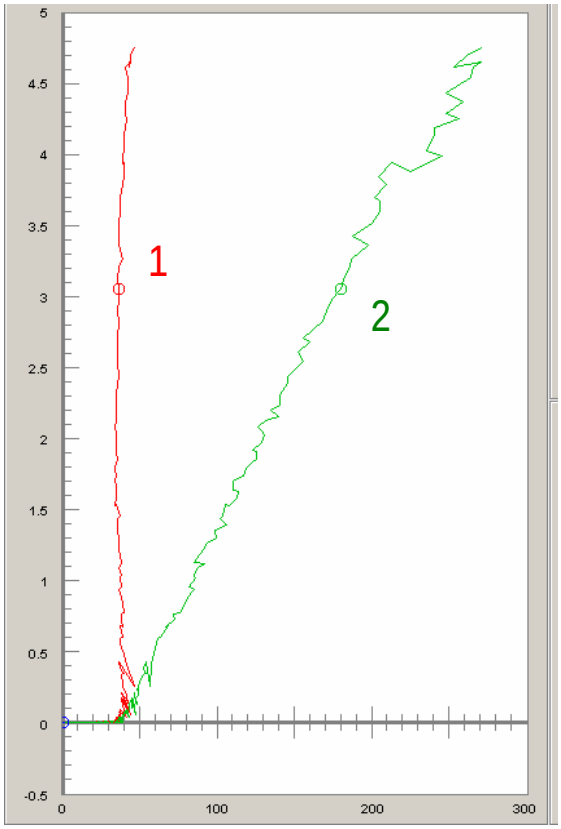

Figure 20: Generation of IV curves based on transient waveforms displayed in Figure 19. (1) using a stable averaging window at the end of the pulse, (2) using the maximum voltage as a function of the average current defined in the stable region. This curve '2' presents the overshoot voltage measured for each current stress level.

An example (Figure 20) of the $V_{overshoot}$ curve ('2', Maximum voltage as a function of average stress current) is generated for an SCR with 4 times minimum design rule dimension for the anode cathode spacing. This 4LAC device is considered a slow ESD device as was already evident from other benchmarks provided above (slow resistance change, higher holding voltage).

The curve ('2') is compared to curve ('1') which represents the IV characteristic using the stable averaging window at the end of the pulse as shown on Figure 19. From curve ('2') it is obvious that the maximum voltage is strongly dependent on the stress current applied. According to the theoretical explanation given above, the voltage overshoot is expected to be lower for faster devices.

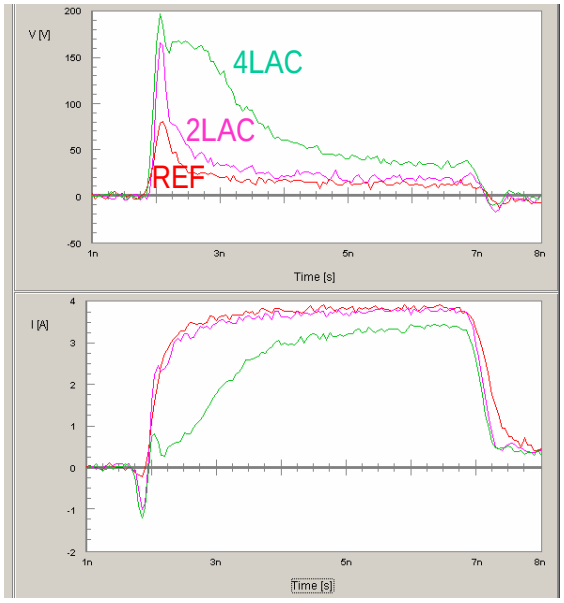

Figure 21: Voltage and current waveforms for three SCR devices with increasing Anode-Cathode spacing, measured using VFTLP at a fixed pulse voltage and 5ns pulse width. The fixed pulse voltage ensures that the devices are stressed with the identical (incident) stress pulses such that the behavior can be compared correctly.

This is confirmed on Figure 21 and on Figure 22 where SCR device 'REF' (minimum Anode Cathode spacing) and SCR device '2LAC' (double Anode Cathode spacing) are compared to the '4LAC' device. From the waveform comparison on Figure 21, the difference in voltage overshoot (for the same initial pulse voltage at the TLP system) is clearly visible. The maximum voltage of the 'REF' device is 3 to 4 times smaller than the maximum voltage for the '2LAC' and '4LAC' devices respectively.

Because the average current used for the vertical axis of curve ('2') on Figure 20 is strongly linked to the selected averaging window, a more neutral way to plot the overshoot voltage is shown on Figure 22. Through the use of the pulse voltage as the x-axis, the voltage overshoot can be compared for different devices for exactly the same applied stress, independent of the selected averaging windows.

An important aspect requires clarification. Most TLP systems contain some form of inductance between the V/I sensors and the device under test. This inductance shows up in the transient voltage waveforms as a peak voltage (L.di/dt) in the beginning of the pulse. Therefore it is important that this system related overshoot is removed (through calibration) before the transient voltage overshoot is used.

The voltage overshoot can be used during ESD design window calculations to incorporate trigger time issues. Typically ESD engineers compare the quasi-static IV characteristic of ESD clamps to a pre-defined ESD design window. However, from the measurements provided in this paper, it is obvious that this can cause

problems for calculations with slow triggered devices. For example, consider a sensitive node in the studied HV DMOS technology that fails at 100V and needs parallel ESD protection. Based on the regular IV curve, using the averaging window (curve '1' on Figure 20), the 4LAC device is believed to protect the sensitive node easily up to 4A. However, this is not a correct assumption since the transient voltage overshoot at about 1.3A can damage the sensitive node (curve '2'). From Figure 22, it is clear that only the 'REF' provides an effective protection.

It should be studied how important the factor time is for the breakdown of the sensitive node (e.g. gate oxides). Studies from e.g. Gieser and Wu [12, 23] show that it is not only electric field which causes breakdown, but electric field during a certain amount of time.

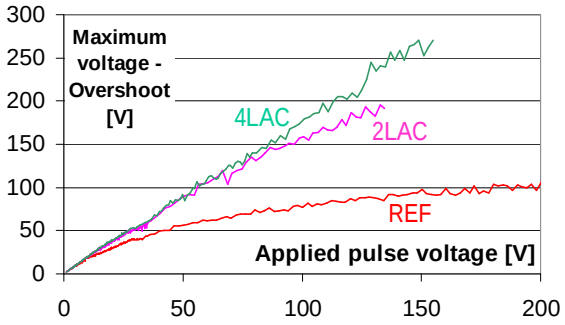

Figure 22: Voltage overshoot (maximum transient voltage) versus pulse voltage characteristics generated for the three SCR devices, measured with 5ns VFTLP.

Conclusions

The VFTLP system provides the test engineer with massive amounts of new data for each of the measured devices. However, without the correct analysis methods and tools, the data can easily be interpreted wrongly. The most important aspect is related to the IV averaging window. This paper shows that the common 25% to 75% averaging window is a bad choice for VFTLP pulse durations below 10ns due to the non quasi-static behavior of most devices in this timeframe.

The paper discusses different transient TLP waveform analysis methods to compare the ESD devices such as the transient voltage overshoot, the clamp dynamic resistance as a function of time and the turn-on time represented by the voltage overshoot.

Finally, the use of the 'Voltage overshoot curve' can be used to provide more accurate estimations for the effective protection level in the case slower ESD protection clamps are used.

References

[1] IEC 610004-2, 1996.

[2] IS0 10605,2001.

[3] IEC 801-2, 1991.

[4] http://www.maxim-ic.com/appnotes.cfm/an_pk/639

[5] ANSIESD STM5.1-2001 or JESD22-A114C.01.

[6] ANSIESD STM5.2-1999 or JESD22-A115-A.

[7] ANSIESD STM5.3.1-1999 or JESD22-CIOIC.

[8] T. J. Maloney, N. Khurana, "Transmission Line Pulsing techniques for Circuit Modeling of ESD Phenomena", Proc. of the EOS/ESD Symposium 1985

[9] Henry, L.G., "Transmission Line Pulse Testing of the ESD Protection Structures of ICs.- A Failure Analysts Perspective.", 2000

[10] Keppens, Bart, "Contributions to standardization of transmission line pulse testing methodology", 2001

[11] Barth, John, "TLP Calibration, Correlation, Standards, and New Techniques", 2002

[12] Gieser, Horst A., "Very-Fast Transmission Line Pulsing of Integrated Structures and the Charged Device Model", 1996

[13] Grund, Evan, "Snapback Device Studies Using Multilevel TLP and Multi-impedance TLP Testers", 2005

[14] Maloney, Timothy J., "Using Coupled Lines to Produce Highly Efficient Square Pulses for VF-TLP - abstract", 2006

[15] Tremouilles, David, "Transient Voltage Overshoot in TLP testing - Real or Artifact?", 2005

[16] Wolf, Heinrich, "Capacitively Coupled Transmission Line Pulsing CC-TLP – A Traceable and Reproducible Stress Method in the CDM-Domain", 2003

[17] E. Grund and R. Gauthier, "VF-TLP Systems Using TDT and TDRT for Kelvin Wafer Measurements and Package Level Testing," Proceedings of EOS/ESD Symposium 2004

[18] Ashton, Robert A., "Extraction of Time dependent Data from Time domain Reflection Transmission Line Pulse measurements", 2005

[19] Bychikhin, S., "Investigation of ESD Protection Elements Under High Current Stress in CDM-Like Time Domain Using Backside Laser Interferometry", 2002

[20] Moens, Peter, "Effects of Hot Spot Hopping and Drain Ballasting in Integrated Vertical DMOS Devices under TLP stress", 2004

[21] Wolf, Heinrich, "Transient Analysis of ESD Protection Elements by Time Domain Transmission Using Repetitive Pulses", 2006

[22] Wolf, Heinrich, "Analyzing the Switching Behavior of ESD Protection Transistors by Very Fast Transmission Line Pulsing", 1999

[23] Wu, J., "Breakdown and Latent Damage of Ultra-Thin Gate Oxides under ESD Stress Conditions", 2000

[24] H. Wolf, H. Gieser, W. Wilkening, "Analyzing the Switching Behavior of ESDProtection Transistors by Very Fast Transmission Line Pulsing", Journal of Electrostatics, Vol. 49, 2000

[25] H. Hyatt, et al., "TLP Measurements for Verification of ESD Protection Device Response", Proc. of the EOS/ESD Symposium 2000

[26] http://www.home.agilent.com/BEdut/nav/-536900532.536905620/pd.html

[27] C. Russ, et al., "GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes", Proc. of the EOS/ESD Symposium 2001.

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Our service and support

Our business models include

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  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

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