Conference paper

Characterizing the Transient Device Behavior of SCRs by means of VFTLP Waveform Analysis

EOS/ESD symposium 2007

New insights regarding the interpretation of the VFTLP IV-curve and the fast transient current and voltage waveform data are presented. These insights are used to determine the design factors affecting the turn-on time and triggering behavior of SCRs in a 90 nm bulk CMOS technology.

Characterizing the Transient Device Behavior of SCRs by means of VFTLP Waveform Analysis

Geert Wybo, Stefaan Verleye, Benjamin Van Camp, Olivier Marichal.

Sarnoff Europe, Brugse Baan 188A, B-8470 Gistel, Belgium,
phone: +32-59-275-915; fax: +32-59-275-916; e-mail: gwybo@sarnoffeurope.com

Abstract – New insights regarding the interpretation of the VFTLP IV-curve and the fast transient current and voltage waveform data are presented. These insights are used to determine the design factors affecting the turn-on time and triggering behavior of SCRs in a 90 nm bulk CMOS technology.

I. Introduction

With the introduction of nanoscale technologies, CDM protection has gained significant importance for the semiconductor industry. A new TLP system (Very Fast TLP - VFTLP), which uses much shorter pulse durations (1-10 ns) and much faster rise times (100-200 ps) than the conventional TLP system (typically 100 ns and 10 ns respectively), is used as an analysis tool. This VFTLP system opens up new possibilities for studying the ESD protection device behavior in the nanosecond time domain, including turn-on time characterization [1-6].

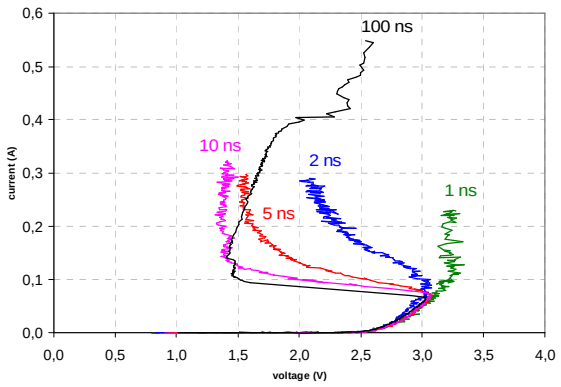

Figure 1: TLP IV-curves for different pulse durations (measured by VFTLP 1 ns, 2 ns, 5 ns, 10 ns pulse duration/100 ps rise time, and conventional TLP 100 ns pulse duration/200 ps rise time) for the 1.2 V reference DTSCR (with gate monitor).

However, due to the different construction of the system and the rather non quasi-static nature of the load response for very fast and short pulses, the analysis of the results obtained by a VFTLP requires a different method than is the case for the conventional TLP. This paper presents new insights regarding the interpretation of the VFTLP IV-curve and the fast transient current and voltage waveform data. These insights are used to determine the design factors affecting the turn-on time and triggering behavior of SCRs in a 90 nm bulk CMOS technology.

The next section will give a brief overview of the VFTLP measurement results interpretation. In Section III a fast transient analysis technique will be proposed. The design parameters influencing the SCR turn-on time and fast transient overshoot are studied in Section IV. In Section V the results of this work are summarized.

II. VFTLP Waveform Analysis

Figure 1 shows the IV-curves of the reference 1.2 V domain DTSCR (with gate monitor) measured for 1 ns, 2 ns, 5 ns, 10 ns (VF-TLP) and 100 ns (TLP) pulse durations. At first sight, the shorter the pulse duration is, the lower the failure current I_{t2} of the SCR. However, the interpretation of the measurement results is not that straightforward [11]. The IV-curve is constructed by averaging the current and voltage waveforms for each pulse into one IV-point of the IV-curve. The averaging window is typically taken towards the quasi-static region of the pulse, and does not take into account the first part of the pulse. For shorter pulse durations, by definition, the averaging window will take more into account the non-quasi-static region of the pulses. Because, in that region, the SCR has not yet fully triggered, the IV-curve will automatically shift towards higher voltages and lower currents. Therefore, care has to be taken when interpreting and comparing IV-curves measured for different pulse durations. The IV-curve itself, and its parameters, like I_{t2}, are dependent on the pulse duration. This effect becomes even stronger for stress pulse durations in the same order as the time needed for the device to settle into the quasi-static state. This explains why a shorter stress time can result in a lower I_{t2} as compared to a longer stress time, even if all other stress parameters, such as rise time and pulse voltages, are equal. This does not mean that the device is weaker for shorter stress durations. In order to fully understand the triggering behavior of the device under test, it is absolutely necessary to interpret the voltage and current waveforms [7][11]. For example, when comparing the turn-on time of devices, it is important to compare the waveforms for the same pulse voltage, rather than for the same (average) current. Due to the fact that the current VFTLP systems allow an easy selection of one waveform for a particular (average) current, rather than

for a particular (same) pulse voltage, turn-on times are sometimes measured and compared for curves at the same current. This is not entirely correct. E.g. a 'slow' device will have a much longer turn-on time, and a much lower average current, when stressed with the same pulse voltage, compared to a 'fast' device. When one compares at the same average current, it means that for the 'slow' device the stress level is much higher, rendering the comparison irrelevant. In addition to comparing the voltage and current waveforms of different devices regarding the turn-on time, a more elaborate fast transient analysis technique is developed in the next section. This technique will solve the issues associated with the currently frequently used ('quasi-static') IV-curves for fast transient analysis.

III. Fast Transient Analysis Technique

With conventional (100 ns) TLP testing, the well-known quasi-static IV-curve is generated. This IV-curve is typically used by ESD protection design engineers for characterizing and analyzing the clamping behavior of tested devices. The TLP IV-curve reveals the protection device parameters, like V_{t1}, I_{t1}, V_h, R_{on}, V_{t2} and I_{t2}, which provide useful information with regard to the clamping capability of the device under test. The TLP IV-curve is typically constructed by averaging the voltage and current waveform values towards the end of the pulse, i.e. when the device is fully triggered and has reached its so-called quasi-static state (**Figure 2**). This TLP IV-curve is useful when developing an ESD protection strategy for HBM and MM-like ESD stress pulses, during which a device typically fails due to the energy content of the pulse. However, when facing CDM ESD stress, the devices typically fail due to the voltage overshoot, rather than the energy content of the pulse.

In order to characterize and study the capability of a device for limiting the overshoot, both in terms of absolute voltage and duration, a new analysis technique, called the fast transient analysis technique, needs to be introduced. Some new kind of plots, different from the conventional quasi-static TLP IV-curves, needs to be constructed in order to visualize and characterize the overshoot limiting capabilities of devices. In a similar fashion as for the quasi-static IV-curve, one can construct the so-called '*transient IV-curve*', by plotting the maximum value of the voltage waveform versus the corresponding value of the current waveform, for increasing pulse voltages. This corresponds to taking an infinitely small averaging window towards the beginning of the pulse, centered on the maximum of the voltage waveform (**Figure 2**). Such a 1-point window, capturing the maximum voltage reached, is relevant when studying the voltage overshoot limiting capability of a device.

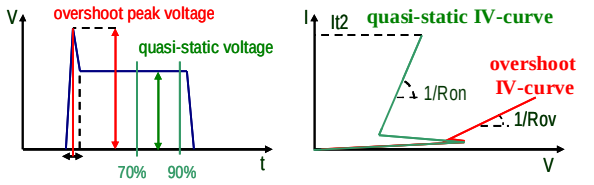

Figure 2: Principle of the construction of the quasi-static IV-curve and the transient overshoot IV-curve. The IV-curve also shows that the dynamic overshoot resistance R_{ov} during turn-on is larger than the dynamic on-resistance R_{on}.

Of course, the voltage and current waveforms should be aligned in time, so that the maximum voltage point and the corresponding current point really correspond to one another in the time domain. This is not necessarily the case for the voltage and current waveforms stored by a commercial VFTLP system. By taking a 1-point window for the transient IV-curve, instead of an averaging window, noise becomes a potential issue for the IV-curve. However, in all cases, an IV-curve is obtained which is still remarkably well-shaped and which is not too much distorted by the noise. The overshoot limiting capability of a device is then characterized by a new device parameter, derived from the transient IV-curve, called the '*dynamic overshoot resistance*' R_{ov}. The meaning of the dynamic overshoot resistance R_{ov} is similar to the meaning of the well-known dynamic on-resistance R_{on}, obtained by conventional TLP characterization. R_{on} determines the dynamic resistance of the device when the device has reached its low-impedance state during ESD discharge. In order to determine the total voltage drop V_{device} over the device during ESD discharge one uses the following formula:

$$V_{device} = V_h + R_{on} \cdot I_{ESD} \quad \textbf{(Equation 1)}$$

The ohmic voltage drop $R_{on} \cdot I_{ESD}$, caused by the dynamic on-resistance, is the voltage drop which has to be added to the built-in voltage or holding voltage V_h of the device, in order to obtain the total voltage drop V_{device} over the device. The meaning of the dynamic overshoot resistance R_{ov} is similar. The term '*dynamic*' does not refer to the transient character of the pulse during overshoot, but refers to the fact that this resistance is accountable for the ohmic part of the total device voltage during ESD discharge. The dynamic overshoot resistance R_{ov} is the resistance during device turn-on, and more particularly at the moment when the voltage reaches its maximum. Because this resistance will determine the actual voltage overshoot (which will possibly cause gate oxide failure), there is a need to name it, and to determine it. ESD designers engineer their devices for V_{t1}, V_h, R_{on} and I_{t2}, when developing a conventional HBM and MM ESD protection strategy. In the same fashion, now one will have to engineer for a lower R_{ov}, because the focus of the ESD protection strategy shifts towards overshoot reduction, especially when designing a CDM protection strategy.

Figure 3 shows the conventional quasi-static IV-curve (green) versus the transient overshoot IV-curve (red) for a Nwell diode (LAC = 0.20 µm) in a 90 nm bulk CMOS technology (both for a pulse duration of 10 ns, and a rise time of 100 ps). It is clear that the dynamic overshoot resistance R_{ov} (9.7 Ohm) is much larger than the dynamic on-resistance R_{on} (2.4 Ohm). Both resistances have been calculated by constructing the trend line according to the root mean square method. The ultimate goal of the ESD protection designers will not only be to reduce R_{on}, but to bring at the same time the transient overshoot IV-curve as close as possible to the quasi-static IV-curve, as to limit the voltage overshoot.

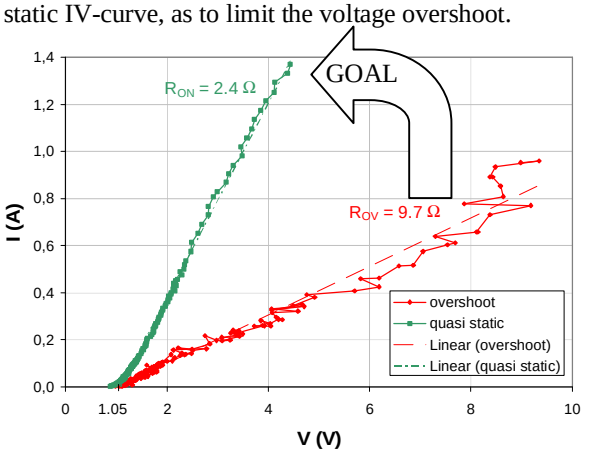

Figure 3: The quasi-static IV-curve (green) and the transient overshoot IV-curve (red) for a NWell diode in 90 nm bulk CMOS (10 ns/ 100 ps).

Commercial VFTLP systems currently construct a '*transient*' IV-curve in which the voltage value is the maximum voltage value of the voltage waveform (averaging window towards the beginning of the pulse), but in which the corresponding current value is obtained by averaging the current waveform during an averaging window towards the end of the pulse (e.g. 70%-90%). This is not entirely correct, because in that way the transient overshoot IV-curve will change depending on the pulse duration. Fundamentally, the overshoot generated by a device does not depend on the duration of the pulse. The overshoot is determined by the dV/dt of the pulse (rather than the rise time) and the turn-on time of the device. Therefore, the transient overshoot IV curve should be independent of the pulse duration. When taking the average current value towards the end of the pulse, the current value will be much lower for a 1 ns pulse than for a 10 ns pulse. In the 1 ns case, the device will be not triggered or be less triggered as compared to the 10 ns case. Therefore, it is also fundamentally wrong to compare two devices (IV-curves) at the same current level, when the current values are taken towards the pulse end. For the slower device, this would mean a much higher stress level. For objective comparison, one should compare at the same pulse voltage.

Therefore, a second useful plot for analyzing the fast transient behavior of devices is introduced: the plot of the overshoot peak voltage versus the pulse voltage (**Figure 4**). Again the overshoot peak voltage is obtained by a 1-point value, rather than an average value. In fact, it would make sense to use an averaging window for determining the overshoot values. It has been observed that a gate oxide does not necessarily fail purely due to the absolute value of the voltage peak, but that the duration of the voltage peak also plays a role. For thin gate oxides (tox < 2nm), this effect becomes particularly visible for overshoot peak durations less than a few 100 ps. However, taking into account an averaging time window for the overshoot peak would complicate things unnecessarily. It would prove very difficult to estimate the boundaries of the time window for integration, and also different voltages would have a different 'weight' on the oxide, so that a weight factor should be introduced for integrating the voltages. Satisfactory results have been obtained by using the absolute value of the voltage peak, rather than to calculate the (weighed) area under the peak. Therefore, this technique will be further used in this paper.

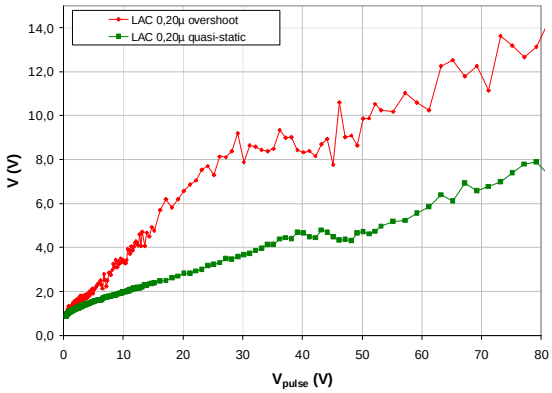

Figure 4: A second useful curve for studying the fast transient behavior of devices in an objective way: the plot of the transient overshoot peak voltage versus the pulse voltage (NWell diode in 90 nm bulk CMOS 10 ns/100 ps).

When studying the fast transient behavior of devices, one needs to focus on the device parameters which result in a lower dynamic overshoot resistance R_{ov}, and as such lower the transient overshoot peak voltage V_{ov}. In all cases studied, a linear relationship is obtained for the transient overshoot peak voltage V_{ov} versus the pulse voltage V_{pulse} (for pulse voltages which make the device trigger).

$$V_{ov} = A + B \cdot V_{pulse} \qquad \textbf{(Equation 2)}$$

In order to limit the transient overshoot peak voltage V_{ov} of the device, one needs to understand which device parameters determine the coefficients A and B in the above equation. This will be the topic of the next section.

IV. Design Factors Affecting Turn-On Time of SCRs in 90 nm Bulk CMOS

The methods described in the previous section are applied to study the design factors affecting the turn-on time and the triggering behavior of SCRs in a 90 nm Bulk CMOS technology. Different DTSCR (Diode Chain Triggered SCR) design variations have been characterized by using a Barth Electronics 4012 VFTLP system. All measurements have been done with a 10 ns pulse duration and a 100 ps rise time, unless otherwise stated. The waveform analysis of the obtained VFTLP data and waveforms was performed by means of a customized software tool, developed in the Agilent VEE Pro environment.

It is a well-known fact that the anode-cathode spacing (LAC) and well resistances of the SCR body module play a key role in determining the turn-on time of the SCR [7]. [10] showed the influence of these both parameters. [9] showed, $t_{on} = \sqrt{t_1 t_2}$, with $t_1 = W_{n1}{}^2 / 2D_p$, and $t_2 = W_{n2}{}^2 / 2D_n$, where W_{n1}, W_{p1} are the base widths of the pnp and npn, respectively, and D_p and D_n are the hole and electron diffusion coefficients, respectively.

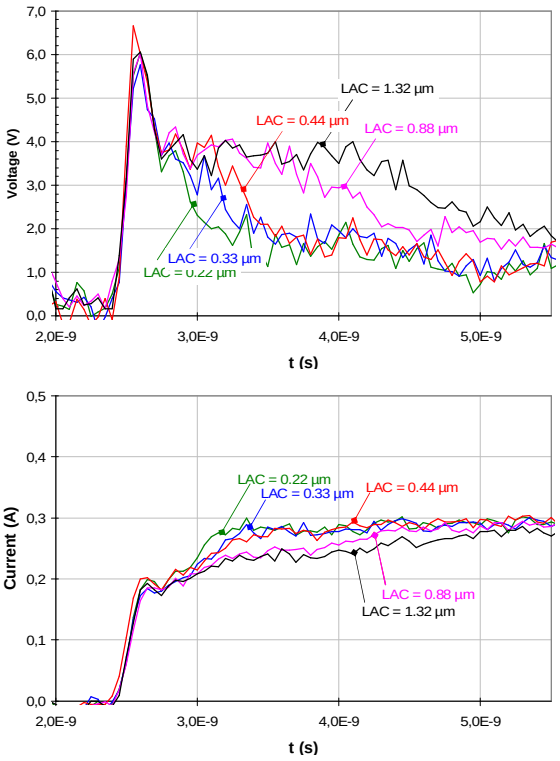

Figure 5: Voltage and current waveforms for the 1.2 V DTSCR with different anode-cathode spacings of the SCR body module (measured by VFTLP 10 ns pulse duration/100 ps rise time; Vpulse = 9 V).

On the test chip, DTSCRs with different LAC spacings have been implemented. The waveforms for a pulse voltage of 9 V are shown in **Figure 5**. These confirm the influence of the LAC spacing, and quantify the triggering speed.

The pulse starts at 2.5 ns and after 5.5 ns all LAC variations are more or less fully triggered, and the current waveforms are approximately the same after this time. This means that the difference between the SCR variations is only relevant during the turn-on phase, and therefore, would not be visible in the quasi-static IV-curve, which does not take into account the first part of the waveforms. This confirms the analysis done by previous authors [10]. The question is: Are the LAC and well resistances the only parameters that determine the turn-on time, or are there other ways to reduce the turn-on time?

This paper focuses on two methodologies, which have the potential of triggering SCRs faster, and/or limiting the voltage overshoot: engineering the SCR trigger and engineering the SCR body. The latter is done by applying localized triggering and substrate current injection. Both methodologies are interrelated, because part of the SCR body is part of the trigger chain, and vice versa.

A. SCR Trigger Engineering

One of the elements which play a major role during device turn-on is the trigger path of the SCR [13]. Therefore, it is investigated what the different trigger parameters are that speed up the SCR turn-on, and limit the voltage overshoot. When considering DTSCR devices, the trigger chain consists of a string of diodes. Therefore, the diode construction and parameters, with regard to the voltage overshoot are investigated. Secondly, also the interaction of the trigger diode string and the SCR itself is investigated. Moreover, because the trigger path of every type of externally triggered SCR contains at least one (internal) diode, all factors limiting the diode overshoot will also be beneficial in limiting the overshoot of any SCR.

The diode overshoot during forward stress is governed by the physics during the forward recovery process. For Nwell diodes, these physics consist of the injection of holes into the well, the diffusion of the holes towards the cathode, the N+/NWell barrier lowering and the injection of electrons from the cathode into the well, resulting into the conductivity modulation of the well [12][14]. The different diode parameters, such as the anode-cathode spacing LAC, the diode width W, the well doping, the N+ and P+ diffusion geometry, the STI depth and the diode construction in general, will have an influence on the forward recovery process. These influences will be looked upon in more detail in this section.

Figure 6 shows the transient IV-curves for the NWell STI diode for different LAC variations, as well as the quasi-static IV-curves.

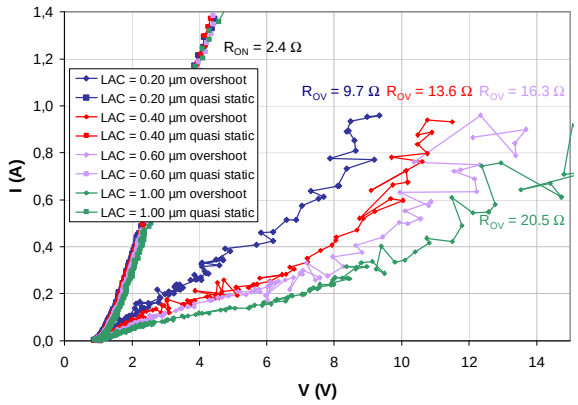

Figure 6: The transient IV-curves for the NWell STI diode LAC variations versus the quasi-static IV-curves (VFTLP 10 ns/ 100 ps).

It can be seen that the dynamic overshoot resistance R_{ov} increases for increasing diode anode-cathode spacings LAC, while the influence on the dynamic on-resistance R_{on} is minimal. For the diode with anode-cathode spacing LAC = 0.20 µm, the resistance during turn-on is 9.7 Ohm, while for the diode with anode-cathode spacing LAC = 0.40 µm, the dynamic overshoot resistance has increased to 13.6 Ohm. The increase of the overshoot for increasing anode-cathode spacings LAC is also shown in **Figure 7**, which shows the corresponding voltage waveforms for a pulse voltage of 8V. The maximum voltage over the diode for an anode-cathode spacing LAC = 0.20 µm is limited to 2.7 V (blue curve), while the maximum voltage for an anode-cathode spacing LAC = 0.40 µm is 3.8 V (red curve) (both for a pulse voltage V_{pulse} = 8 V).

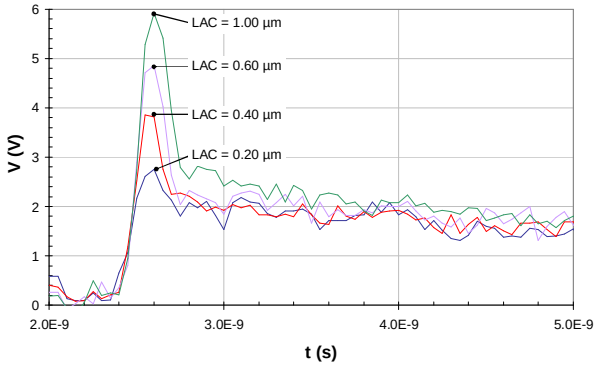

Figure 7: The corresponding voltage waveforms for the NWell STI diode LAC variations (VFTLP 10 ns/ 100 ps) (V_{pulse} = 8 V).

Another parameter, which will have a determining influence on the forward recovery process and the maximum voltage V_{ov} during turn-on, is the diode perimeter or diode width W.

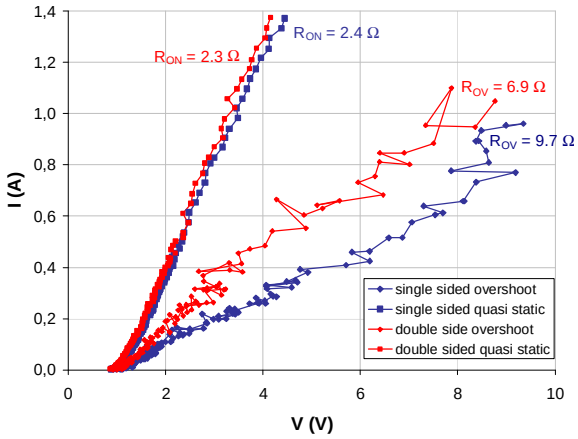

Figure 8: The transient IV-curves for the NWell STI diode perimeter variations versus the quasi-static IV-curves (VFTLP 10 ns/ 100 ps) (LAC = 0.20 µm).

Figure 8 shows that, as expected, the perimeter of the diode plays an important role for limiting the voltage overshoot. In general, making the width of the trigger chain larger, including the width of the internal SCR diode, will be beneficial for limiting the voltage overshoot during turn-on. Doubling the width of the MDR LAC diode, by making the diode double-sided, results in a decrease of the dynamic overshoot resistance of 2.8 Ohm (**Figure 8**).

A third parameter investigates the influence of the length of the diffusions (besides the width) on the diode overshoot for NWell STI diodes. The influence of the length of the N+ diffusion, the P+ diffusion, and/or the well length will be discussed.

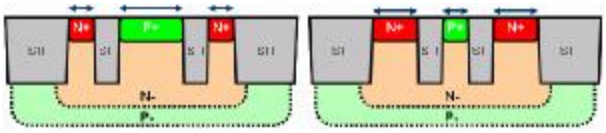

Figure 9: Changing the size of the N+ diffusion for the NWell STI diode is done by increasing the length of the N+ diffusion. Changing the size of the P+ diffusion is done by increasing the length of the P+ diffusion.

Figure 9 shows how the size of the N+ diffusion for the NWell STI diode is changed by increasing the length of the N+ diffusion. A ‘large’ N+ diffusion corresponds to a N+ diffusion for which the length is three times the standard length (= contact width + 4* active area coverage over contact) used for the control structure. A ‘large’ P+ diffusion corresponds to a P+ diffusion for which the length is six times the standard length used for the control structure.

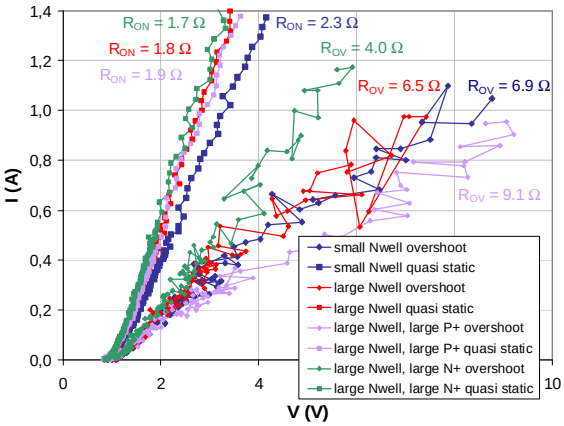

Figure 10: The transient IV-curves for the NWell STI diode variations in which the size of the N+ diffusion, P+ diffusion, and NWell was changed, versus the quasi-static IV-curves (VFTLP 10 ns/ 100 ps).

Figure 10 shows that a larger N+ diffusion is beneficial for reducing the dynamic overshoot resistance R_{ov} (green curve). **Figure 10** also shows that a larger P+ diffusion is detrimental for reducing the diode overshoot (purple curve). It is expected that for Pwell diodes enlargening the P+ diffusion is beneficial, as well as shortening the N+ diffusion.

Furthermore, the influence of the well type on the overshoot is investigated. This is done by comparing PWell diodes versus NWell diodes, regarding dynamic overshoot resistance R_{ov}.

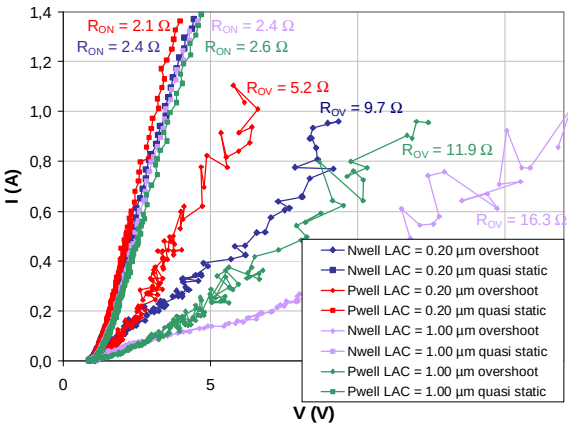

Figure 11: The transient IV-curves for the NWell and PWell STI diode variations, versus the quasi-static IV-curves (VFTLP 10 ns/ 100 ps).

Figure 11 shows that PWell diodes are less resistive during overshoot than NWell diodes (with the same anode-cathode spacing LAC). Most probably this is due to the differences in well doping, and the differences in minority carrier mobility. This result should be taken into account when considering G1 or G2 triggered SCR devices.

Finally, whether the dynamic overshoot resistance can be further decreased by using a different type of diodes, i.e. gated diodes, is examined.

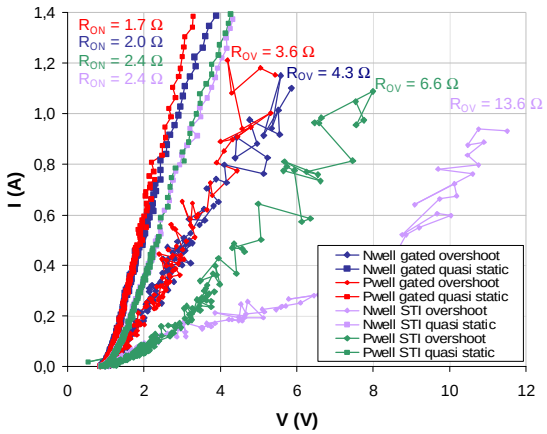

Figure 12: The transient IV-curves for NWell and PWell gated diodes (single sided; LAC = 0.40 µm) versus STI diodes (single sided; LAC = 0.40 µm), versus the quasi-static IV-curves (VFTLP 10 ns/ 100 ps).

Figure 12 compares gated diodes and STI diodes (single sided; LAC = 0.40 µm) regarding overshoot. It is shown that gated diodes significantly reduce the overshoot. For Nwell diodes the dynamic overshoot resistance R_{ov} is reduced to 4.3 Ohm by gating them. For Pwell diodes the dynamic overshoot resistance R_{ov} is reduced to 3.6 Ohm. These values are approximately two times the dynamic on-resistance R_{on}.

For diodes in the SCR trigger path, the findings of this section can be summarized as follows: PWell diodes are less resistive than NWell diodes during turn-on; both types of diodes have the smallest overshoot for the smallest anode-cathode spacing; both types of diodes have the smallest overshoot for the largest perimeter; NWell diodes can be made less resistive by enlargening the length of the N+ diffusion, and shortening the length of the P+ diffusion; both types of diodes can be made less resistive by gating them. Combining all these factors into a diode optimized for overshoot reduction is expected to lower the dynamic overshoot resistance towards the value of the dynamic on-resistance. These optimized trigger diode chain will ultimately result in a much decreased overshoot.

Now that single diodes have been investigated, the question remains: what about the voltage overshoot generated by a diode chain consisting of N diodes in series? Is the maximum voltage during turn-on over a chain of N diodes equal to N times the maximum voltage over 1 diode during turn-on (assuming that the pulse voltage V_{pulse} is the same in both cases)? Assuming that the dynamic overshoot resistance of N diodes in series ($R_{ov(Ndio)}$) is equal to N times the dynamic overshoot resistance R_{ov} of 1 diode, one can easily show that:

$$V_{DUT(Ndio)} \cong V_{DUT} \cdot \frac{1+50/R_{OV}}{1+50/(N \cdot R_{OV})} \quad \textbf{(Equation 3)}$$

with:

$V_{DUT(Ndio)}$ = maximum voltage over N diodes during turn-on

V_{DUT} = maximum voltage over 1 diode during turn-on

In order to obtain the above equation the built-in voltages of the diode and the diode chain have been neglected. This means that the equation will not be valid for transient overshoot peak voltages which are comparable to the diode built-in voltage.

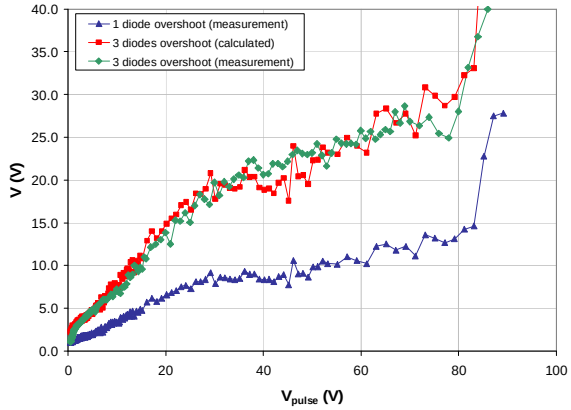

Figure 13: Maximum voltage during turn-on for 1 diode (blue curve), for 3 diodes in series (calculated; red curve), and for 3 diodes in series (measured; green curve).

Figure 13 shows a remarkable confirmation of equation 3. The blue curve shows the transient overshoot peak voltages during turn-on for 1 diode (NWell LAC=0.20 µm; see also **Figure 4**). The red curve shows the calculated values of the overshoot peak voltage for a chain of 3 diodes. The calculation is based on the measurement results for 1 diode (blue curve) using Equation 3. The green curve shows the measured transient overshoot peak voltages during turn-on for 3 diodes (NWell LAC=0.20 µm). There is a striking confirmation of the calculated values (red curve). This proves: (a) that the assumption about the series dynamic overshoot resistance of N diodes, being equal to N times the dynamic overshoot resistance of 1 diode, is right; (b) that the turn-on of N diodes in series is a synchronous process, not a sequential process. This is an important finding. It means that the 'second' diode does not have to 'wait' for the 'first' diode to turn on. All series diodes turn on at the same time. If there would have been a 'waiting time' this would mean that the individual maximum voltages over each diode would have been shifted in time, resulting in a lower combined maximum voltage. On the other hand, the duration of the combined peak would take longer. In case the individual maximum voltages over each diode would be shifted in time, equation 3 would prove incorrect, and the measured curve would not overlay the calculated curve.

Now that the maximum overshoot peak voltage generated by a diode chain is investigated, what about the maximum voltage generated by a DTSCR?

Before the SCR body is able to trigger, a critical amount of charge has to be injected into the SCR body. This amount of charge is provided by the trigger chain. Does this mean that the overshoot of an SCR is by definition equal to that of its trigger chain? Or can the SCR triggering be sped up to such a degree that the SCR itself nibbles on the actual maximum voltage during turn-on, resulting in an even further decreased overshoot?

Because the SCR body is triggered by a certain amount of charge density, the turn-on time of the SCR is not a constant, but is highly dependent on the pulse voltage. This can easily be seen by comparing the voltage waveforms shown in **Figure 14** to **Figure 16**. For lower pulse voltages the overshoot generated by the DTSCR is the equal to the overshoot generated by its diode trigger chain (including G1-Cathode diode of SCR) (**Figure 14**). During the first phase, when the diode string is not yet triggered, the voltage waveform of the diode chain and the DTSCR necessarily overlay each other. During a second phase, the diode chain becomes low resistive due to conductivity modulation of its well. The voltage drops and the trigger starts to conduct more current, but the charge density provided by the conducting diode chain is still too low in order to trigger the SCR itself. In a third phase, there is enough charge injected into the SCR body, so that the SCR body triggers. The voltage over the SCR starts to drop below the voltage of the trigger diode chain (control structure).

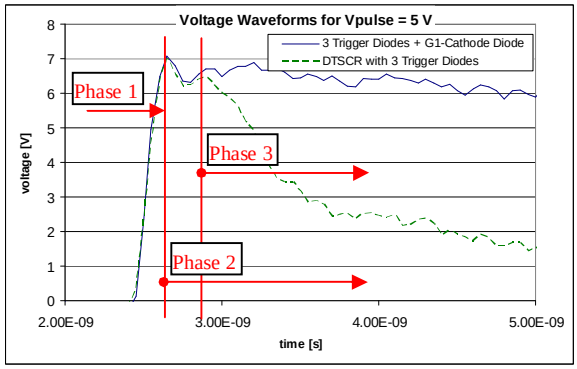

Figure 14: Voltage waveforms for the DTSCR with 3 trigger diodes (green curve) versus the control structure (3 trigger diodes + G1-Cathode diode; blue curve) for a pulse voltage of 5 V. Initially, the diode chain is not yet triggered (phase 1). During a second phase (phase 2), the diode chain is turned on. In a third phase (phase 3), there is enough charge injected into the SCR body, so that the SCR body is triggered.

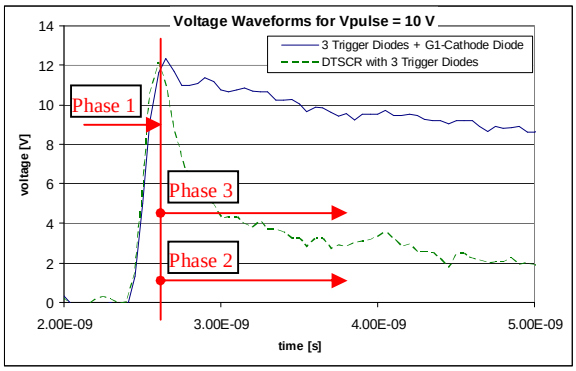

Figure 15: Voltage waveforms for the DTSCR with 3 trigger diodes (green curve) versus the control structure (3 trigger diodes + G1-Cathode diode; blue curve) for a pulse voltage of 10 V. The SCR body triggers as fast as the diode chain.

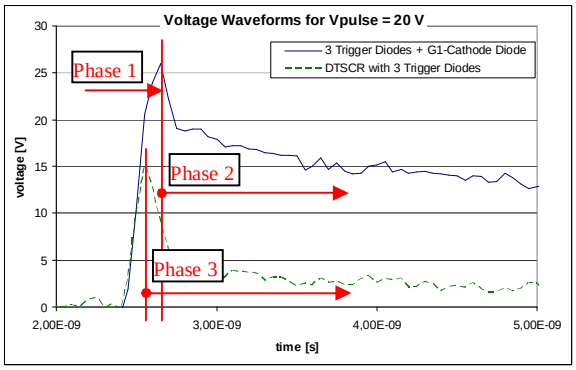

Figure 16: Voltage waveforms for the DTSCR with 3 trigger diodes (green curve) versus the control structure (3 trigger diodes + G1-Cathode diode; blue curve) for a pulse voltage of 20 V. The SCR body triggers even when the diode chain is still in its high-resistive state.

For higher pulse voltages, the diode chain, is able to inject sufficient charges into the SCR body, in order to trigger the SCR, even when the diodes are still in their high-resistive state. While the voltage over the trigger chain (control structure) itself would still rise, the SCR triggers fast enough and starts to bite into the overshoot peak. This is shown in **Figure 15** and **Figure 16**.

For a pulse voltage of about 10 V, phase 2, during which the diodes are low-resistive, and phase 3, during which the SCR is low-resistive, start at the same time. The SCR triggers as fast as the time needed for the forward recovery of the diodes. However, there is still no reduction in overshoot peak voltage due to the SCR action (**Figure 15**).

For pulse voltages above 10 V, the SCR action starts to considerably reduce the voltage peak (**Figure 16**). In this case, phase 3, the low resistive state of the SCR, starts before the forward recovery phase of the diodes (phase 2).

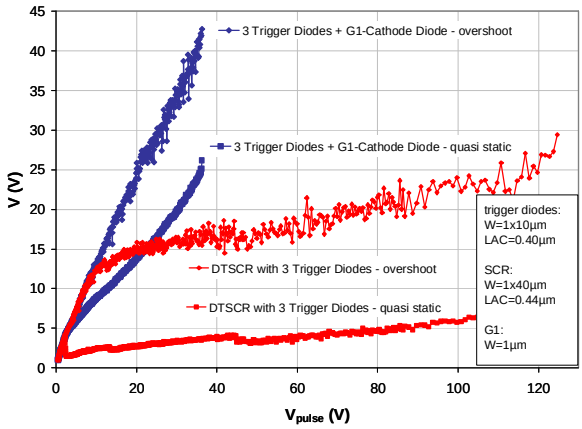

Figure 17: Overshoot peak voltage as a function of pulse voltage for the DTSCR with 3 trigger diodes (red curve) versus the control structure (3 trigger diodes + G1-Cathode diode).

Figure 17 compares the overshoot peak voltage as a function of pulse voltage for the DTSCR with 3 trigger diodes (red curve) versus the control structure (3 trigger diodes + G1-Cathode diode; blue curve). It is clear that the overshoot peak voltage is not only determined by the trigger chain, but that the SCR itself has a large impact on the overshoot peak voltage reduction. This opens the door for further SCR optimization, such as SCR body engineering.

B. SCR Body Engineering

In the previous section, methods for reducing the diode and diode chain overshoot have been presented. The DTSCR shown in the previous section is certainly not optimized with regard to the trigger chain. It has been shown that the use of NWell diodes with a larger perimeter, NWell diodes with a larger length of the N+ diffusion, or gated NWell diodes, or a combination of the above, will each reduce the voltage overshoot drastically. The internal SCR diode forms an integral part of the SCR trigger chain. Therefore, these findings should also be taken into account when designing the SCR body. Besides engineering the internal SCR diode, this section focuses on techniques for speeding up the SCR by engineering the body of the SCR itself. Two techniques are applied: localized triggering and substrate current injection.

1. Localized Triggering

An SCR triggers when sufficient current is injected in both the NPN and the PNP base regions. It is assumed that the SCR triggers locally, meaning that the primary enabler for triggering is not absolute current, but current density. Afterwards, the current will spread over the full device width. Therefore, two layout variations are compared in order to investigate whether injecting all trigger current in one spot, i.e. locally increasing the current density, speeds up triggering.

These variations are shown in **Figure 18**. In the top layout, all trigger current is injected in a G2 tap with very limited dimensions. The bottom layout has a wide G2 tap.

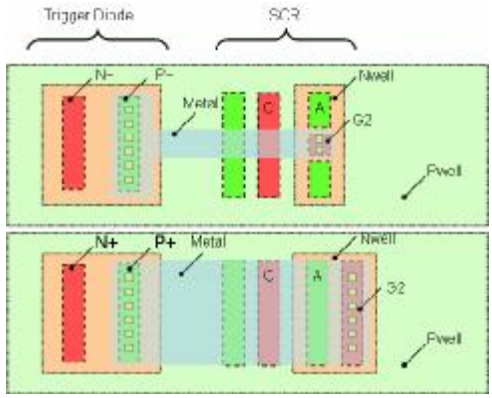

Figure 18: Speeding up the turn-on of the SCR body module by injecting the trigger current locally (top). The control structure with the conventional layout is also shown (bottom).

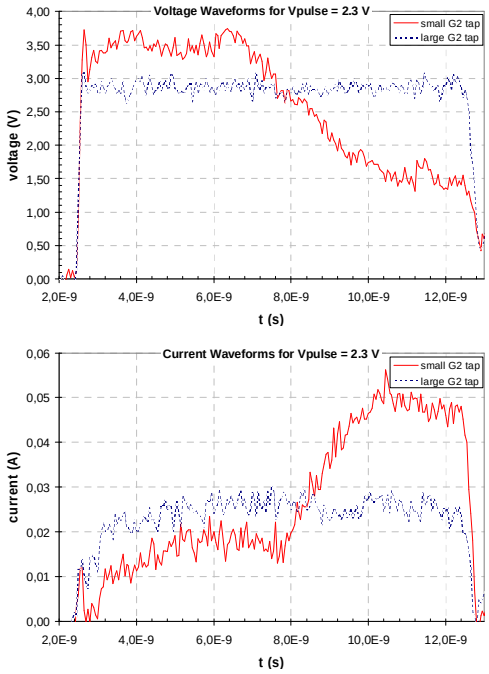

Figure 19: Voltage waveforms (top) and current waveforms (bottom) for the 1.2 V DTSCR with localized triggering versus conventional triggering (measured by VFTLP 10 ns pulse duration/100 ps rise time/2.3 V pulse voltage).

Figure 19 shows the voltage and current waveforms at a pulse voltage of 2.3 V for both layout variations shown in **Figure 18**. The variation with the small G2 tap triggers at much lower absolute current (~15 mA), while the control structure remains in off-state, although the absolute injected current is higher (~25 mA). The control structure eventually triggers at a trigger current of about 80 mA (**Figure 1**). For both structures the guard ring was placed at the same distance, rather close to the SCR body. Of course, in the case of sizing the SCR gate, there exists a trade-off between the overshoot peak voltage and the trigger speed.

2. Substrate Current Injection

In order to investigate the influence of substrate current injection, the placement of a diode up or holding diode with regard to the SCR body (schematic of **Figure 20**) is examined. The diode acts as a current injector. Two layout versions of this schematic are drawn, shown in **Figure 21**. By decreasing the spacing between the diode and the SCR (layout b), the injected substrate current will increase. Therefore, the required trigger current decreases, which is expected to result in a smaller turn-on time of the SCR.

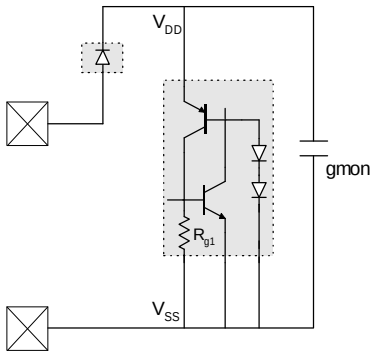

Figure 20: Schematic of the SCR with diode up.

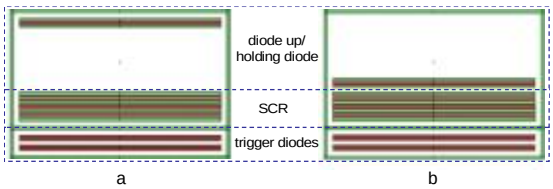

Figure 21: Two layout variations of the schematic in Figure 20. In the left figure the diode up/holding diode-SCR spacing is ~17 µm, while in the right figure the spacing is only ~2 µm.

The IV curves are shown in **Figure 22**. The trigger current for layout (b) is a lot lower than for layout (a). This can easily be explained as follows: the holding diode injects current in the substrate through the inherent PNP. In the case of layout (a), this injected current is shunted to ground through the guard ring, which is placed close by. Only a small fraction of the current will flow to the SCR. For layout (b), however, a much larger portion of the injected current reaches the SCR, such that it will aid the triggering, resulting in a lower trigger current. In the current and voltage waveforms (**Figure 23**) it is also apparent that for the same pulse voltage, layout (b) results in triggering of the SCR, while in layout (a) the device remains in off-state. This again shows that placing the holding diode or diode up close by, helps to trigger the SCR.

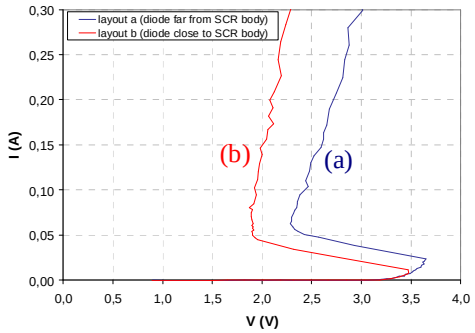

Figure 22: IV curve of layouts (a) and (b). In layout (a), the diode is placed far away from the SCR body. In layout (b), the diode is placed close to the SCR body.

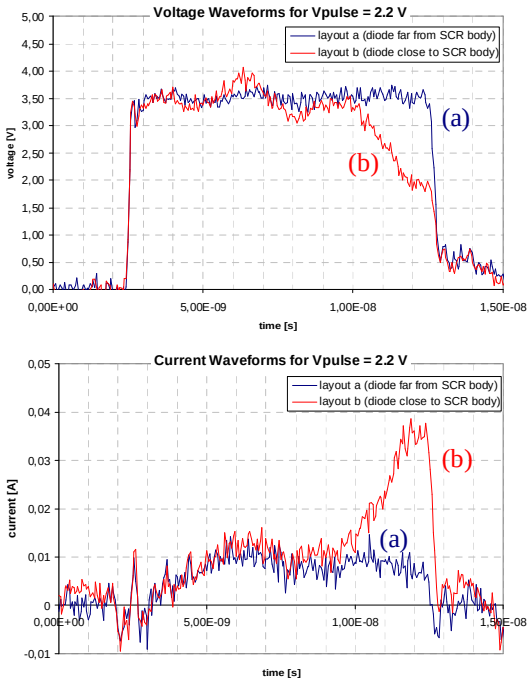

Figure 23: Voltage waveforms (top) and current waveforms (bottom) of the layouts (a) and (b) for a pulse voltage of 2.2 V.

V. Conclusion

When analyzing the triggering behavior of the SCR using the VF-TLP, it is more important to look at the current and voltage waveforms, rather than at the quasi-static IV-curve. The transient IV-curve, showing the dynamic overshoot resistance, and the overshoot versus pulse voltage curve are used for visualizing and analyzing the overshoot limiting capabilities of devices. These techniques are applied in studying layout variations of the SCR body and trigger, in order to show that the turn-on time is not only governed by the anode-cathode spacing and well resistances. Several techniques for optimizing the trigger chain are proposed. Furthermore, two SCR body engineering techniques, which decrease the turn-on time, are proposed:

1. Localized Triggering
2. Substrate Current Injection

Finally, it is shown that the characteristics of the applied pulse, such as the pulse voltage, influence the turn-on time. Therefore, the turn-on time is not a fixed property of the device itself.

VI. Acknowledgements

The authors acknowledge the financial support of the Flemish Government through the IWT050294 project for research on "Nano Physics Beyond Normal Operation".

The authors would also like to thank Akram Salman from AMD for mentoring the paper and for providing comments that helped in adding more value to the data presented.

VII. References

[1] T. J. Maloney, N. Khurana, “Transmission Line Pulsing techniques for Circuit Modeling of ESD Phenomena”, Proc. of the EOS/ESD Symposium, 1985.

[2] Barth, John, et al., "TLP Calibration, Correlation, Standards, and New Techniques", IEEE Transactions on Electronics Packaging Manufacturing, 2001.

[3] Gieser, Horst A., et al., "Very-Fast Transmission Line Pulsing of Integrated Structures and the Charged Device Model", Proc. of EOS/ESD Symposium, 1996.

[4] Ashton, Robert A., "Extraction of Time dependent Data from Time domain Reflection Transmission Line Pulse measurements", Proc. of the International Conference on Microelectronic Test Structures (ICMTS), 2005.

[5] Wolf, Heinrich, et al., "Transient Analysis of ESD Protection Elements by Time Domain Transmission Using Repetitive Pulses", Proc. of the EOS/ESD Symposium, 2006.

[6] Wolf, Heinrich, et al., "Analyzing the Switching Behavior of ESD Protection Transistors by Very Fast Transmission Line Pulsing", Proc. of the EOS/ESD Symposium, 1999.

[7] Li, Junjun et al.; “Improved Wafer-level VFTLP System and Investigation of Device Turn-on Effects”, Proc. of the EOS/ESD Symposium, 2005.

[8] C. Russ, et al., “GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes”, Proc. of the EOS/ESD Symposium, 2001.

[9] S.M. Sze, “Physics of Semiconductor Devices, Second Edition”, John Wily & Sons.

[10] J. Di Sarro, et al., “Study of Design Factors Affecting Turn-On Time of Silicon Controlled Rectifiers (SCRs) in 90 and 65 nm Bulk CMOS Technologies ”, Proc. of the IRPS Symposium 2006.

[11] B. Keppens, et al., “Using the Voltage and Current Waveforms from VFTLP Systems to Study Transient Device Behavior”, Proc. of RCJ Symposium, 2006.

[12] R. Kolessar, “Physical Study of the Power Diode Turn-on Process”, Proc. of the IEEE Industry Applications Society Annual Meeting, 2000.

[13] M.P.J. Mergens, et al., “Advanced SCR ESD Protection Circuits for CMOS / SOI Nanotechnologies”, Proc. of the Custom Integrated Circuits Conference, 2005.

[14] J. Willemen, et al., “Characterization and Modeling of Transient Device Behavior under CDM ESD Stress”, Proc. of the EOS/ESD Symposium, 2003.

About Sofics

ESD SOLUTIONS AT YOUR FINGERTIPS

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

Version

May 2011

Sofics BVBA
Groendreef 31
B-9880 Aalter, Belgium
(tel) +32-9-21-68-333
(fax) +32-9-37-46-846
bd@sofics.com
RPR 0472.687.037