Conference paper

CDM analysis on 65nm CMOS: Pitfalls when correlating results between IO test chips and product level

EOS/ESD symposium 2008

Unlike HBM and MM, CDM robustness is highly dependent on IC layout and packaging. Therefore, IC companies mimic IC IO rings on IO-TEG test chips to select the most appropriate CDM protection concepts (correlation from IO-TEG to final IC's). This publication highlights pitfalls for this approach. Ensuring consistent substrate and Vss connections drastically improve the correlation.

CDM analysis on 65nm CMOS: Pitfalls when correlating results between IO test chips and product level

Teruo Suzuki[(1)], Kenji Hashimoto[(2)], Nobuyoshi Isomura[(1)], Noboru Yokota[(2)], Olivier Marichal[(3)], Bart Sorgeloos[(3)], Benjamin Van Camp[(3)], Bart Keppens[(3)]

(1) Macro Development Dept., Technology Development Division, Fujitsu VLSI Limited
1844-2, Kozoji-cho 2-chome, kasugai-shi, Aichi 487-0013. Japan
TEL: +81-568-51-8234 / FAX: +81-568-51-7669
E-Mail: suzuki_teruo@fvd.fujitsu.com
(2) SYSTEM LSI TECHNOLOGY & PRODUCT DEPT., Technology Development Division,
Fujitsu Microelectronics Limited
(3) Sarnoff Europe BVBA, Brugse Baan 188A, B-8470 Gistel, Belgium

This paper is co-copyrighted by Fujitsu Microelectronics Limited, Fujitsu VLSI Limited, Sarnoff Europe and the EOS/ESD symposium

50 Words Abstract - Unlike HBM and MM, CDM robustness is highly dependent on IC layout and packaging. Therefore, IC companies mimic IC IO rings on IO-TEG test chips to select the most appropriate CDM protection concepts (correlation from IO-TEG to final IC's). This publication highlights pitfalls for this approach. Ensuring consistent substrate and Vss connections drastically improve the correlation.

I. Introduction

The CDM robustness of IC's is very important in advanced applications and process technologies. While the continuous scaling of process technologies has enabled all kinds of new consumer and industrial applications, it has also increased the ESD vulnerability of the core and IO devices dramatically. New protection devices and concepts are developed to ensure ESD robust product releases.

Due to the rising cost in design and fabrication it is extremely important to evaluate the ESD properties of these device concepts before they are included into a final IC product. The first-time-right IC release is mandatory in the fast changing Consumer Electronics (CE) market where being late on the market by half a year can make the difference between high margin profits and selling below cost. Surely, adequate ESD protection is one of the items on the checklist of the quality department to be fulfilled before releasing the product.

As soon as a new process technology is available, the ESD development team starts to qualify the concepts. In a very early state (first ESD-TEG test chip), Human Body Model (HBM) and Machine Model (MM) properties can be quantified. However, because the CDM robustness is highly dependent on the full IC layout, package and bonding type, the actual CDM robustness can only be qualified on a final product [1-3]. To overcome this 'chicken-and-egg' paradox, IC companies tend to mimic IC IO rings on a so-called IO-TEG test chip in order to select the most appropriate CDM protection concepts and devices (Figure 1). Sometimes, a difference in CDM results is observed between the IO-TEG and the real product. This publication highlights some of the pitfalls for correlating the IO-TEG results to the full product results. Ensuring consistent substrate and Vss connections can drastically improve the correlation.

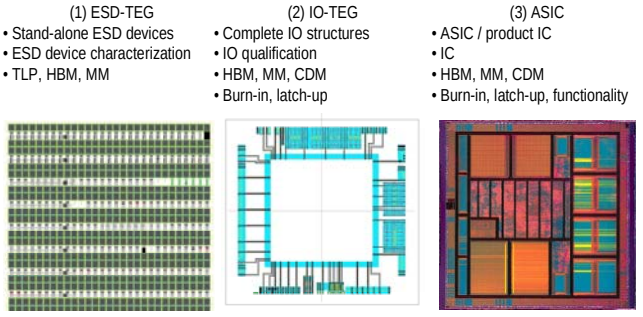

Figure 1: Three development stages in the creation of ESD robust ASIC's. (1) The ESD-TEG is used for optimizing stand-alone ESD devices and for characterization of the process technology, (2) The IO-TEG combines IO structures and ESD protection for IO qualification purposes and (3) The IO structures are used in the final ASIC. For HBM, MM, CDM measurements packages of QFP120, QFP208 and PBGA208 are used respectively. Chip size is 4.2 mm x 4.2mm.

First the advanced 65nm technology, selected ESD devices and the test equipment are introduced. In the next section, the CDM measurement results of the IO-TEG are presented together with the results of a final product with the same ESD structures. Further, in section four, failure analysis results provide an explanation for the large difference in test results. Finally, the paper concludes with basic guidelines for IO-TEG implementation to improve the correlation of CDM results between an IO-TEG and real product IC's.

II. Technology, Devices and Equipment

This study presents data based on Fujitsu's state-of-the-art 65nm technology using bulk wafers (P/P- substrate; 11-Cu layers, Ultra-low K). The core devices have a minimal gate length of 50nm and a gate oxide thickness of 1.0nm. Measurements on 90nm and 130nm low-resistive Epi wafers (P/P+ substrate) are included in the discussion to highlight the influence of the substrate resistance on the resulting CDM performance.

While the technology covers IO structures for 1.8V, 2.5V and 3.3V, this publication has a focus on the most challenging domain: 1.2V (core protection). The core breakdown is determined through measurements on the ESD-TEG, leading to a design window depicted in Figure 2, right side.

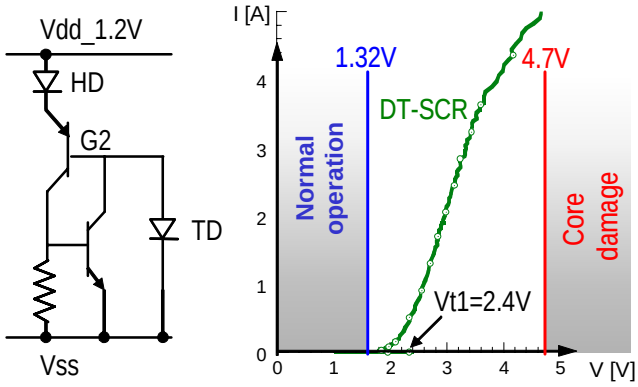

Figure 2: (left side) 1.2V core protection device based on Diode Triggered Silicon Controlled Rectifier (DT-SCR) with one holding diode and one trigger diode. (right side) The ESD design window is determined by TLP measurements on gate monitor structures, inverter totem-pole devices and stand alone MOS transistors on the 65nm ESD-TEG test chip. Multiple pulse stress testing and process variations are accounted for. The TLP IV curve of the DT-SCR device fits the ESD design window with Vt1=2.4V; Vh=1.7V; It2=4.2A and Ron=1.3Ohm. The clamp achieves >8kV HBM and >400V MM with parallel monitor structures.

The selected core protection is based on a Diode Triggered SCR (DT-SCR) [4] with one trigger diode connected between G2 (Nwell tap) and ground and one holding diode connected between VDD and Anode, shown on Figure 2, left side. The device layout is optimized for a low voltage Vt1 trigger voltage, fast triggering, maximum ESD robustness per area and lowest voltage drop at high currents. The SCR is constructed as a double-sided device with a width of 37um to ensure a power cell width of 45um. Due to the strong SCR performance in this 65nm technology, the power clamp occupies an area of only 30.14um x 45um, including the trigger and holding diodes and the reverse Vss-Vdd diode.

VF TLP data is show below on Figure 3 (IV curve and leakage). In this study, VF TLP measurements are performed with a 10ns pulse width and a fast rise time of 100ps. To determine the influence of SCR trigger speed the most important factor is the rise time which was set to the most aggressive setting (100ps). The pulse width has no real influence on the failure of the sensitive gate oxide due to the low voltage clamping of the protection device.

From the IV curve it is clear that a VF TLP curve with an averaging window at 5ns-8ns does not provide additional information over regular 100ns TLP measurements, except maybe the higher It2 value when the clamp is measured in stand-alone mode. VF TLP measurements are mainly interesting to study the turn-on transient behavior. Therefore, separate waveforms are included in Figure 4 and Figure 5.

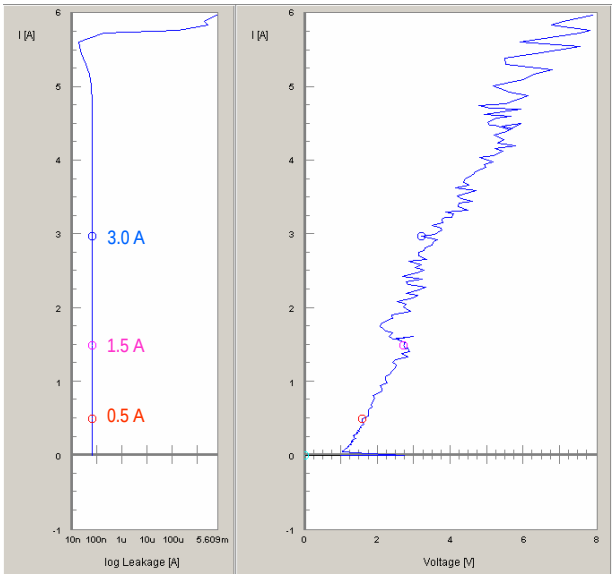

Figure 3: VF-TLP curve (10ns pulse width – 100ps rise time) for the DT-SCR device without holding diode. A thin oxide gate monitor device is connected in parallel with the SCR to study the effectiveness of the protection concept under the worst case stress test. Starting from 1.4A the noise in the voltage waveform creates more variation in the IV curve. The corresponding waveforms are shown on Figure 4 and on Figure 5.

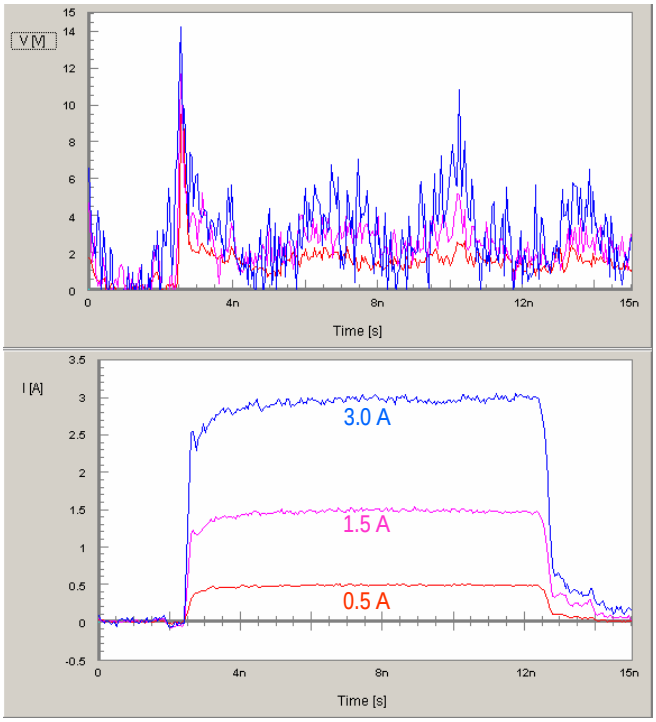

Figure 4: Voltage and Current waveform data for the Diode Triggered SCR (DT-SCR) under 10ns VF TLP stress. Different lines depict increasing current stress levels (0.5A to 3A). On Figure 5, the voltage waveform data is shown with more detail to highlight the turn-on information.

The voltage waveforms are copied again on Figure 5 to highlight the turn-on information. Despite the high voltage overshoot (>12V) the parallel gate oxide monitor was not damaged even at 3A. The data represents a worst case situation as there is no parallel capacitance (parasitic core capacitance) or resistance (parasitic core leakage pad) between pad and ground on the ESD-TEG test chip. Such parasitic elements drastically reduce the voltage overshoot in real IO circuits [5]. VF TLP measurements on the IO-TEG could not yet be performed because the IO-TEG bond pad pitch did not match the 50 Ohm RF needle configuration.

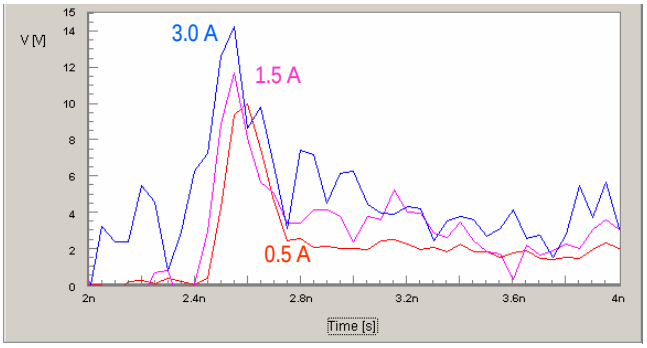

Figure 5: Voltage waveform data for the DT-SCR under 10ns VF TLP stress. Different lines depict increasing current stress levels (0.5A to 3A). The waveform data is shown between 2ns and 4ns to highlight the turn-on information. Despite the voltage overshoot to >12V, the parallel thin gate oxide monitor is not damaged during the test.

Measurement results on an ESD-TEG and two IO-TEG versions are compared to results on an analog ASIC product IC. The different IO-TEG's and the analog IC are depicted schematically on Figure 6. The main difference between the three cases is the Vss connection between the different domains. In the first IO-TEG case {1}, the different domains are completely separated from each other, while in the IO-TEG case {2}, a wide, low resistive Vss ring is inserted connecting all the Vss pads together. The third case is an Analog IC {3} where the Vss connections for the digital IO's are all connected together. The Analog IO's have a separate analog Vss bus but this bus is connected through anti-parallel ('back-to-back diodes') to the digital Vss grid.

The divider cells are inserted into the IO-TEG case {1} to rule out a positive influence of a large parasitic capacitance between Vdd and Vss for small IO domains during HBM testing. Such separated layout represents the worst-case scenario [6]. Clearly, when all the domains are connected together, the increased Vdd-Vss capacitance slows down the rising edge of ESD pulses applied at Vdd and IO's pads. This means that the resulting ESD data cannot be guaranteed for small Vdd-Vss domains.

Measurement results are obtained with the following equipment:

- HANWA HED-C5002 [FI-CDM (JEDEC)]
- Barth Electronics 4002 [TLP]
- Barth Electronics 4012 [VF TLP]
- HANWA HED-S5256A [HBM, MM]
- Keytek MK2 [HBM, MM]

The next sections of the paper provide the CDM results and failure analysis pictures and a discussion on the non-obvious results.

III. Measurement results

The measurement results on the different TEG's are depicted below in Table 1.

The measurements on the ESD-TEG include standard HBM and MM qualification to select the optimal design and layout. The DT-SCR achieves more than 8kV HBM and over 400V MM when tested in stand-alone configuration on the ESD-TEG. Four cases are compared below where CDM results differ quite drastically for the same core protection cell.

Failure analysis (IR-Obirch and SEM) is used to interpret the results and to rule out any 'false positives' during CDM testing where an effective ESD protection is interpreted as ineffective due to a measurement artifact.

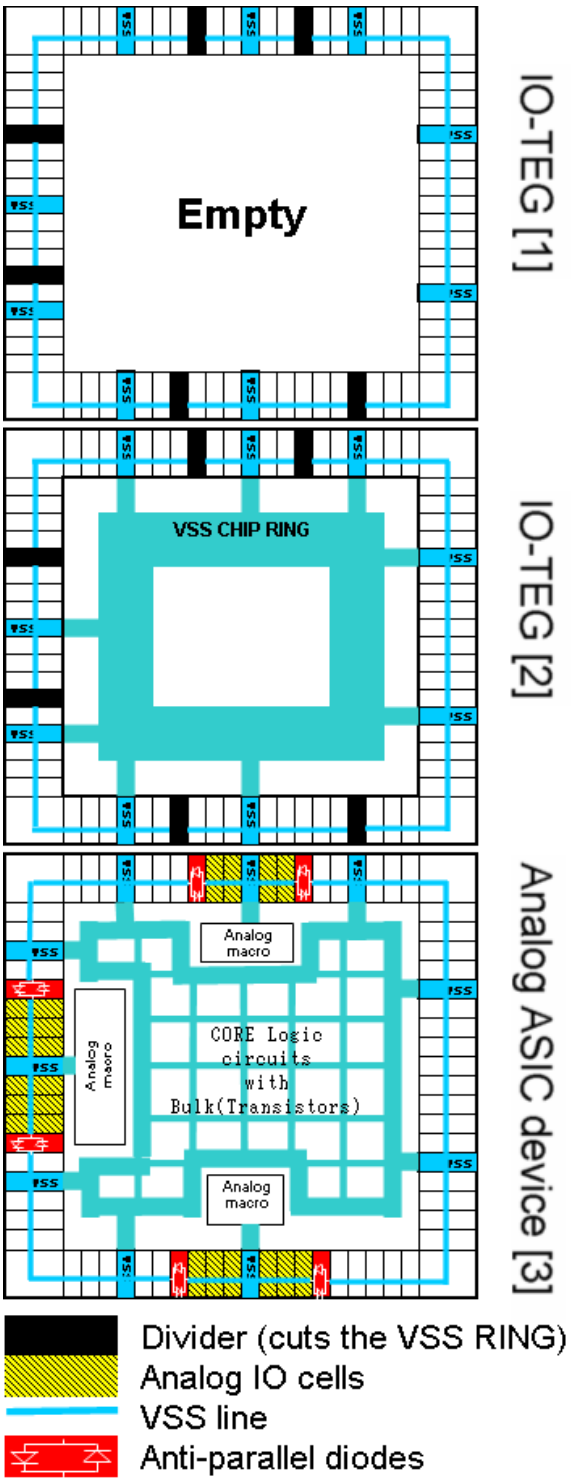

Figure 6: Different IO-TEG's {1} and {2} and ASIC {3} configurations used in the study to correlate CDM results of the DT-SCR core protection. In the IO-TEG [1] (top), different IO and core domains are created that are completely separated from each other. The Vss bus line is interrupted at the 'divider' cells (depicted in black). The IO-TEG [2] is identical except that an additional low resistive Vss ring is created shorting all Vss cells together. In the ASIC [3] case separate analog domains (dashed) exist but the Vss lines (analog and digital) are connected through the use of 'anti-parallel' diodes.

ESD-TEG - DT-SCR with sensitive monitor					QFP208
TLP	4.2 A				
HBM	> 8kV [MK2] // >4kV [Hanwa]				
MM	> 400V				
IO-TEG {1} – separated domains - Stand alone DT-SCR power clamp					QFP120
CDM [+]	750V		CDM [-]	1000V	
Ipeak [+]	4.5 – 5.4 A	@ 1000V	Ipeak [-]	5.8 – 6.8A	@ 1250V
IO-TEG {1} – separated domains - DT-SCR power clamp and LV IO's					QFP120
CDM [+]	>1500V		CDM [-]	250V	
Ipeak [+]	8.0 – 8.9 A	@ 1500V	Ipeak [-]	3.3 – 3.6A	@ 500V
IO-TEG {2} with VSS connection - DT-SCR power clamp and LV IO's					QFP208
CDM [+]	>1500V		CDM [-]	>1500V	
Ipeak [+]	10.5 – 11.7 A	@ 1500V	Ipeak [-]	7.9 – 9.2A	@ 1500V
Analog ASIC device {3} - DT-SCR core protection and sensitive core					PBGA208
CDM [+]	>1500V		CDM [-]	>1500V	
Ipeak [+]	8.7 – 9.6A	@ 1500V	Ipeak [-]	10.9 – 13.0A	@ 1500V

Table 1: HBM, MM and CDM results for the DT-SCR protection cell for different configurations and different TEG test chips. Each of the results is explained with failure analysis data below. The package type is mentioned on the right side: 'QFP208', 'QFP120' and 'PBGA208' have been used in this study.

IV. Failure analysis and discussion

The first case (Stand alone DT-SCR on the IO-TEG with completely separated domains) has a CDM failure at +1000V (+750 pass) and at -1250V (-1000V pass). IR-Obirch pictures (Figure 7) of the failed sample show a conductive path between adjacent bond pads. The stressed bond pad is the Vdd pad on the right side, visible on Figure 7-B (zoom in).

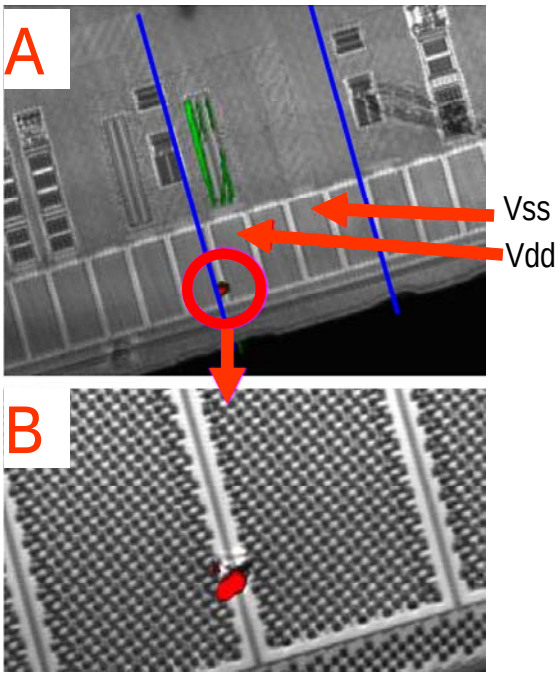

Figure 7: IR-Obirch picture (overview on top 'A', zoom below 'B') showing the failure location of the stand-alone DT-SCR power clamp on IO-TEG [1]. From the picture it is obvious that a conductive path has formed between the neighboring bond pads. A lack of a low resistive current path for CDM charges stored in the adjacent IO domain creates a voltage drop between the bond pads large enough to break down the ILD oxide.

The bond pad on the left side is connected to another (separated) IO domain. Because there is no direct connection (except through the substrate) the CDM charges from the adjacent domain have no way to reach the grounded (Vdd) bond pad. The adjacent bond pad remains charged up until the breakdown voltage of the ILD oxide is reached.

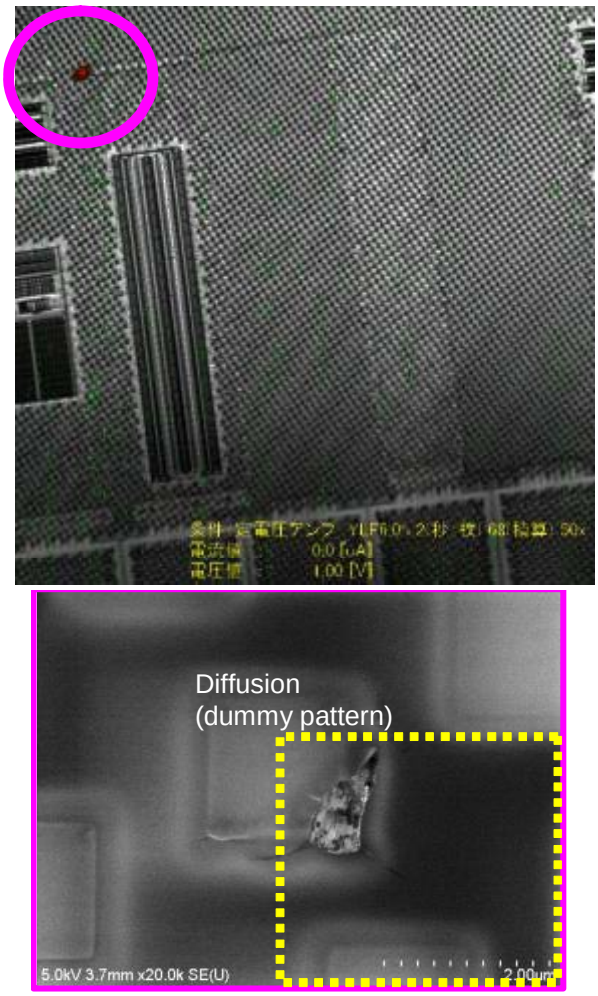

Figure 8: Metal 1 to Substrate oxide breakdown during CDM stress on IO-TEG {1} with separated domains. The metal line (depicted with the dashed line) is stripped before the failure analysis. This metal 1 line is connected to the grounded Vdd pad. The CDM charges in the underlying substrate have no low resistive path to the grounded bond pad.

Similar failure cases are found on other tested samples where the oxide between metal-1 and the underlying substrate is damaged. The insertion of active dummy patterns (to prevent CMP related process issues) below Metal 1 lines reduced the breakdown voltage. Such a failure is depicted on Figure 8. A schematic cross section is provided in Figure 9.

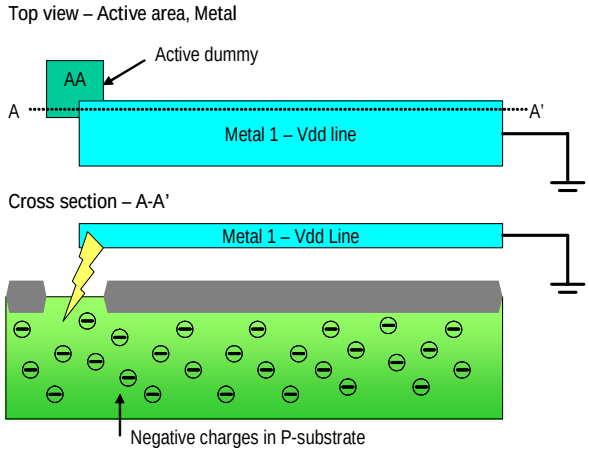

Figure 9: Metal 1 to Substrate oxide breakdown during CDM stress on IO-TEG {1} with separated domains. The metal line (depicted with the dashed line on Figure 8) is connected to the grounded Vdd pad. The CDM charges in the underlying substrate have no low resistive path to the grounded bond pad.

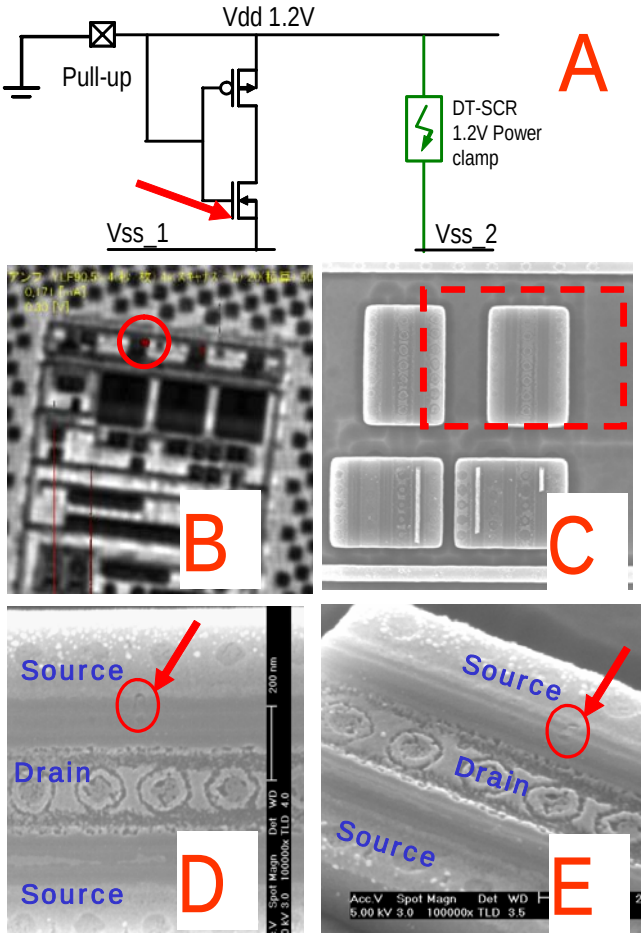

Figure 10: Failure inside a 1.2V core area during -500V CDM stress. Failure analysis (IR-Obirch 'B' and SEM 'C', 'D' and 'E') leads to a failed gate-source overlap GOX rupture in a small pull-up (W/L NMOS = 3.2um/0.06um) configuration, because the negative charges at Vss_1 have a high resistive path to Vss_2 as can be seen on the schematic 'A'.

The second case (DT-SCR core protection inside a LV IO domain, separated from other IO domains on IO-TEG {1}) has a very low negative CDM value of -

250V (-500V fail). The failure analysis (IR-Obirch and SEM analysis) is depicted on Figure 10.

IO-TEG {2} with an additional low resistive Vss ring yields much higher and consistent values (1500V pass) for the same stress cases. Since the wide Vss bus is the only difference between both IO-TEG's {1} and {2}, it is clear that a consistent Vss and substrate ground connection can drastically improve CDM performance by providing low resistive paths for CDM charges stored in unrelated power domains.

The same conclusion is obvious from the last case {3}, where an analog ASIC is created with Vss and substrate connections covering the whole IC. The results show high CDM robustness, even for the small separated analog domains. For these domains, the inter domain connections are ensured through anti-parallel diodes between the Analog Vss and digital Vss lines. A CDM current waveform is depicted on Figure 11. 6 samples were measured with resulting peak currents between 10.9A and 13A.

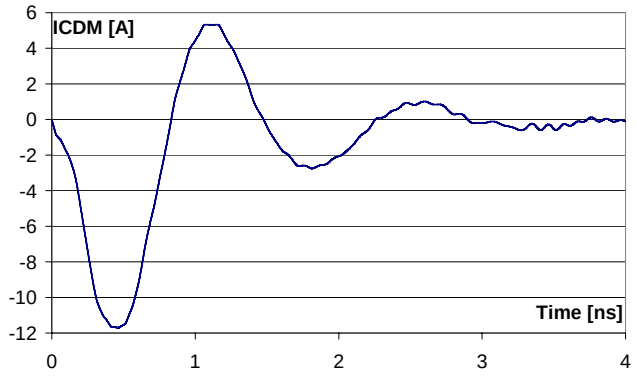

Figure 11: Current waveform during negative CDM stress (1500V) on the analog ASIC (case {3}). Peak current measured on 6 samples varied between 10.9A and 13A. No failure is detected after the applied CDM stress.

To verify the conclusions, additional measurements are performed on other technology nodes (90nm, 130nm) and different starting material such as high ohmic (P/P-) substrate and low ohmic (P/P+) substrate wafers. Further, another power clamp concept (RC-triggered MOSFET) is used. The summary of these measurements is provided in Table 2, below.

Measurements on 65nm bulk wafers (high ohmic P/P- substrate) show a similar behavior: Lower than expected CDM results on the IO-TEG with separated domains can be improved through the inclusion of a wide VSS connection bus, similarly to IO-TEG case {2}.

Measurements on 90nm and 130nm on Epi wafers (low-ohmic P/P+ substrate) show a consistent high CDM performance despite the use of separated domains in the IO-TEG, in line with the conclusion from Sowariraj [7] about the influence of the substrate resistance ("Circuits on high ohmic substrate are more vulnerable to CDM damage"). This result highlights the fact that measurements on IO-TEG test chips with separated domains without VSS connections can still yield high CDM performance as long as there is a low ohmic current path between the different Vss domains. Such low-ohmic path can consist of a wide Vss bus as in the case of IO-TEG {2} in this study, a consistently placed Vss grid as in the ASIC {3} configuration or through the low-ohmic substrate as demonstrated on the 90nm and 130nm IO-TEG results.

65nm P/P-wafer – HIGH ohmic substrate					
IO-TEG separated domains - RC-triggered MOSFET clamp and LV IO's					
CDM [+]	1250V		CDM [-]	500V	
Ipeak [+]	8.4 - 9.4A	@ 1500V	Ipeak [-]	5.3 - 6.4A	@750V
IO-TEG with VSS connection - RC-triggered MOSFET clamp and LV IO's					
CDM [+]	>1500V		CDM [-]	>1500V	
Ipeak [+]	10.8 -12.6A	@ 1500V	Ipeak [-]	8.7 - 9.8A	@1500V
90nm P/P+wafer – LOW ohmic substrate					
IO-TEG – separated domains - RC-triggered MOSFET clamp and LV IO's					
CDM [+]	>1500V		CDM [-]	>1500V	
Ipeak [+]	10.0 -11.9A	@ 1500V	Ipeak [-]	8.3 - 9.9A	@1500V
130nm P/P+wafer – LOW ohmic substrate					
IO-TEG – separated domains - RC-triggered MOSFET clamp and LV IO's					
CDM [+]	>1500V		CDM [-]	>1500V	
Ipeak [+]	10.6 -12A	@ 1500V	Ipeak [-]	9.1 – 10.8A	@1500V

Table 2: CDM results and peak current levels for IO-TEG test chips implemented on different technology nodes (65nm, 90nm, 130nm), different substrate materials (high and low ohmic) and using another power clamp concept (RC-triggered MOSFET). All samples are packaged in a QFP208 package.

Conclusion

This paper presents data on pitfalls (false positive) that prevent IC makers to guarantee CDM robust IC's based on IO-TEG characterization. Measurements on Fujitsu's advanced 65nm process technology from the ESD-TEG and two IO-TEG's are compared to a full product ASIC implementation. This comparison provides insight on CDM performance correlation issues. Specific IO-TEG layout details can drastically influence the CDM performance estimations that lead to a wrong conclusion (inefficient core protection clamp). However, ensuring consistent substrate and Vss connections along the IO-TEG test chip drastically improves the correlation and provides useful and consistent CDM data for product implementations. Measurements on low-ohmic substrates confirm the story: High CDM performance can be achieved when low resistive connections exist between distant locations in the substrate.

Acknowledgements

The authors wish to thank Dr. Akram A. Salman for his kind mentoring of the publication. The authors would like to thank the DEVICE ANALYSIS CENTER at FUJITSU for the PFA analysis, and Masayoshi Kojima for ESD testing support.

Also the authors express deep gratitude to Haruyoshi Takaoka from Fujitsu VLSI Limited, Shoji Ichino from Fujitsu Microelectronics Limited and Koen Verhaege from Sarnoff Europe for supporting the analysis project and the publication of the results.

References

[1] T. Maloney, “Designing MOS Inputs and Outputs to Avoid Oxide Failure in the Charged Device Model.”, EOS/ESD Symposium, pp. 220-227, 1988

[2] T. Brodbeck, “CDM Tests on Interface Test Chips for the Verification of ESD Protection Concepts”, EOS/ESD Symposium, pp. 1-8, 2007

[3] T. Brodbeck, et al., “Influence of the device package on the result of CDM tests”, EOS/ESD Symposium, pp. 320-327, 1998.

[4] M. Mergens et al., ”Diode-Triggered SCR (DTSCR) for RF-ESD Protection of BiCMOS SiGe HBTs and CMOS Ultra-Thin Gate Oxides.”, IEDM, pp. 515-518, 2003.

[5] K. Watanabe et al., “New Protection Techniques and Test Chip Design for Achieving High CDM Robustness”, EOS/ESD Symposium 2008

[6] T. Suzuki, “A study of relation between a power supply ESD and parasitic capacitance”, EOS/ESD Symposium, pp. 290-297, 2005.

[7] M.S.B. Sowariraj et al., “Study of the influence of package parasitics and substrate resistance on the Charged Device Model (CDM) failure levels – possible protection methodology”, 2004 http://de.scientificcommons.org/m_s_b_sowariraj

About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

As is the case with many published ESD design solutions, the techniques and protection solutions described in this data sheet are protected by patents and patents pending and cannot be copied freely. PowerQubic, TakeCharge, and Sofics are trademarks of Sofics BVBA.

Version

May 2011

Sofics BVBA
Groendreef 31
B-9880 Aalter, Belgium
(tel) +32-9-21-68-333
(fax) +32-9-37-46-846
bd@sofics.com
RPR 0472.687.037