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Conference paper

Comprehensive tool for on-chip ESD protection design to achieve first-time-right success

IP-Based SoC Design 2008

Industry experts attribute up to 33% of all IC product losses to be caused by Electrostatic Discharge (ESD), a high current, short duration annoyance. The induced failures can occur anywhere from semiconductor fabrication to field application and represent millions of dollars in real losses each year. To prevent such failures, ASIC designers add on-chip ESD protection circuitry, provided by the foundry, included in the IO library or developed in-house. In the past designers could rely on a simple but effective protection device inherent in a NMOS transistor. This ESD 'clamp' could be used for almost all protection cases. However, due to technology scaling and due to the recent increased use of complex, sensitive analog interfaces, the selection of the optimal ESD protection clamp becomes ever more difficult. This work presents an interactive ESD design environment to cope with this complexity. The toolset provides immediate feedback on the consumed silicon area, ESD robustness, capacitive loading and induced leakage and is based on ESD protection switches that are silicon and product proven in 8 CMOS generations (0.5um down to 40nm). The simulations predict full chip ESD protection levels. The tool is currently in use at leading semiconductor companies to effectively reduce the ESD related failures.

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Comprehensive tool for on-chip ESD protection design to achieve first-time-right success

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Abstract :

Industry experts attribute up to 33% of all IC product losses to be caused by Electrostatic Discharge (ESD), a high current, short duration annoyance. The induced failures can occur anywhere from semiconductor fabrication to field application and represent millions of dollars in real losses each year. To prevent such failures, ASIC designers add on-chip ESD protection circuitry, provided by the foundry, included in the IO library or developed in-house. In the past designers could rely on a simple but effective protection device inherent in a NMOS transistor. This ESD 'clamp' could be used for almost all protection cases. However, due to technology scaling and due to the recent increased use of complex, sensitive analog interfaces, the selection of the optimal ESD protection clamp becomes ever more difficult. This work presents an interactive ESD design environment to cope with this complexity. The toolset provides immediate feedback on the consumed silicon area, ESD robustness, capacitive loading and induced leakage and is based on ESD protection switches that are silicon and product proven in 8 CMOS generations (0.5um downto 40nm). The simulations predict full chip ESD protection levels. The tool is currently in use at leading semiconductor companies to effectively reduce the ESD related failures.

Keywords – ESD, HBM, Design tool.

Introduction

Electrostatic Discharge (ESD) is the sudden discharge of a charged body and is known to anyone as the 'shock' one feels when touching the car on a cold winter day or touching a doorknob after walking over a carpet. Most readers have been introduced to ESD on high-school during experiments such as rubbing a glass rod with a cat fur. Due to tribo-electric (friction) and induced effects objects collect electrical charges. When the object then touches another object at a different potential, charges are redistributed. Such re-distribution occurs quickly (duration of microseconds, rise time of a few nanoseconds) and easily represent a current amplitude of 1-10 ampere, depending on materials, humidity, speed of contact and separation as the main factors.
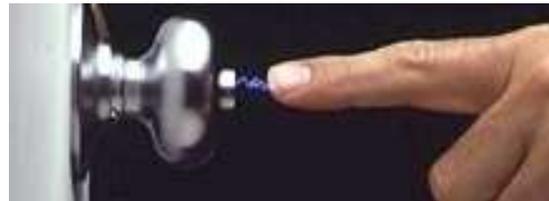

Figure 1: Electrostatic Discharge in real life when touching a doorknob. While it is mostly harmless for a human, its finger and the door knob, the same event causes millions of dollars loss in the semiconductor industry every year.

While this is a general physical phenomenon, these ESD events still cause much havoc in the semiconductor industry. According to different authors the total cost to the semiconductor industry due to unexpected ESD failures is huge. [1-2]

To counter the large annual losses, the industry has first set-up ESD control programs to prevent the build-up of charge in the semiconductor production and assembly plants. Further, OEM and system makers include ESD protection elements on the PCB board, next to sensitive IC's. Finally, they also demand a level of protection on the IC's. Therefore, IC designers include on-chip clamp devices and run compliance tests such as Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM) test programs before releasing the IC on the market [3-5].

On-chip ESD protection used to be simple when the basic semiconductor transistors could be easily adapted to sustain and protect all kinds of ESD stress combinations. However, for some time now, the ggNMOS device has lost its key role for ESD protection and a myriad of new ESD clamp approaches have been created [6]. A rapid rise of the number of ESD protection device patents to over 100 applications per year clearly shows that new solutions were needed. Today, in mainstream to advanced CMOS, IC designers must customize the ESD protection approach for each IO type.

To support IC designers during the complex creation of their next hopefully high-volume produced ASIC, various tools have been developed in the past. All kinds of simulators, EDA tools and verification capabilities have been added to the toolset to ensure that the ASIC indeed will function as expected. Until recently there was no tool available for optimizing ESD protection networks on the chip. Sure, top IDM (Integrated Device Manufacturers) have long developed internal automation software for ESD [7-8] but these are unavailable for the fabless community partly because the tools rely on company owned proprietary ESD clamp solutions and in-house technical knowledge. Sarnoff Europe, an on-chip ESD protection IP provider is changing that unbalanced situation. In his 2004 paper [8] M. Streibl from Infineon summarized it nicely: "ESD

hardness of a full chip is no longer limited by the protection strategies but by the degree of correct implementation of the rules in a complex chip."

This publication provides information about an ESD design tool that supports IC designers in their ESD decisions. First, the general tool approach is detailed. Next, in section 3, the ESD design window concept is explained. Section 4 provides a view on the protection definition approach for IO's. Finally the paper concludes with achieved measurement results following successful implementation into semiconductor products.

1. ESD design tool – generic approach

A typical ASIC consists of one or more functional core circuits, a number of inputs, outputs and bidirectional IO's. A simplified generic IC is depicted in figure 2. ASIC's with multiple power domains are discussed further down.

ESD stress can occur between any two pins. To cover all these stress combinations on-chip ESD protection clamps are included between all the IO's and the supply nodes (VDD and VSS/GND). Also, in parallel with the functional core a protection element is added. All of the ESD elements need to be carefully defined into an ESD protection network to ensure that the device passes the ESD qualification tests. Many different approaches and ESD clamp types exist, each with specific benefits
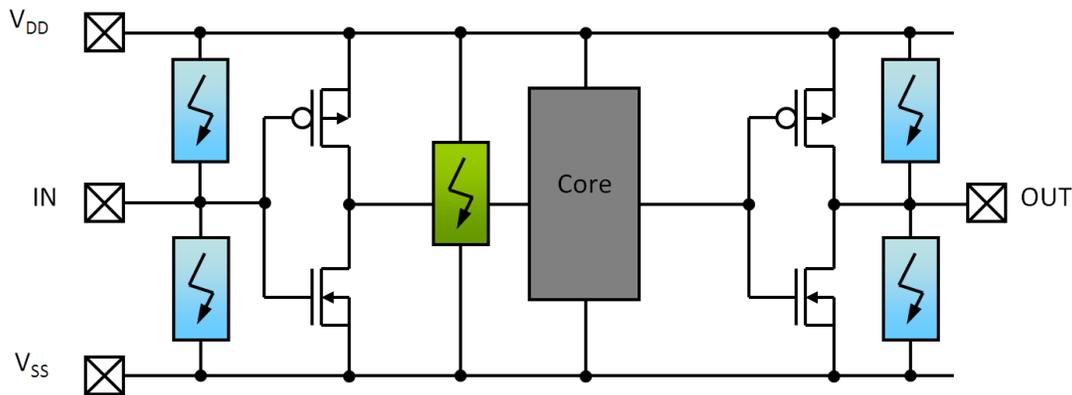

Figure 2: Generic single supply ASIC with symbolic representations of the ESD protection elements. Each of the ESD clamps can be optimized to trade-off between normal operation behavior (leakage, capacitance, matching) and ESD protection level.
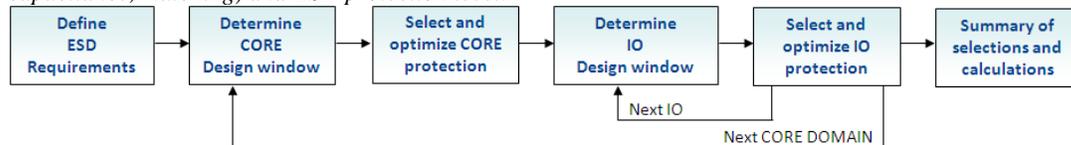

Figure 3: Generic, full chip ESD design flow chart as included into the TakeCharge ESD design tool. After the ESD requirements are entered, a first power cell protection is tackled followed by iteration for all of the IO's in the voltage domain. This is repeated until all voltage domains are protected. Finally, inter-domain cases are studied.

and problems. Some clamps, for instance, tend to consume considerable silicon area or introduce a huge resistance and capacitance loading of the IO's.

The ESD design tool consists of a clearly defined sequence or flow chart, depicted in Figure 3. The IC designer is forced to follow the step wise approach. This ensures that no part of the ASIC remains unprotected. First, the ESD requirements are entered into the 'ESD specification' window shown on Figure 4. HBM and MM requirements are translated to their respective peak current level based on a first set of experimental data performed in the selected foundry node. Next, a first power domain is tackled, including its IO's. In the example, the 65nm CMOS technology includes 3 voltage options that are optimized consecutively (1.2V, 2.5V and 3.3V). Finally, inter domain interfaces are investigated. Such interfaces are a growing ESD issue for advanced multi-power domain IC's. Specific solution approaches are included in the tool.

The power domain optimizer is handled in the 'Power protection' screen (Figure 5). The IC designer selects the clamp type and size. Moreover, the effect of the bus resistance on the power clamp repetition rate can easily be calculated with the 'bus resistance' wizard. The simulation results are immediately available through the use of simplified models (Sequential Linear Interpolation) for the ESD clamp behavior. The calculation results are available in graphical and table format. The user can proceed to the IO protection definition only after the power cell selection is finalized.

2. ESD design window concept

Over the course of the years many different IO types have been introduced such as digital buffers, differential signaling and analog interfaces. Each of the IO types requires its own protection approach. To summarize the requirements, ESD engineers use a so-called ESD design window, depicted on figure 6.
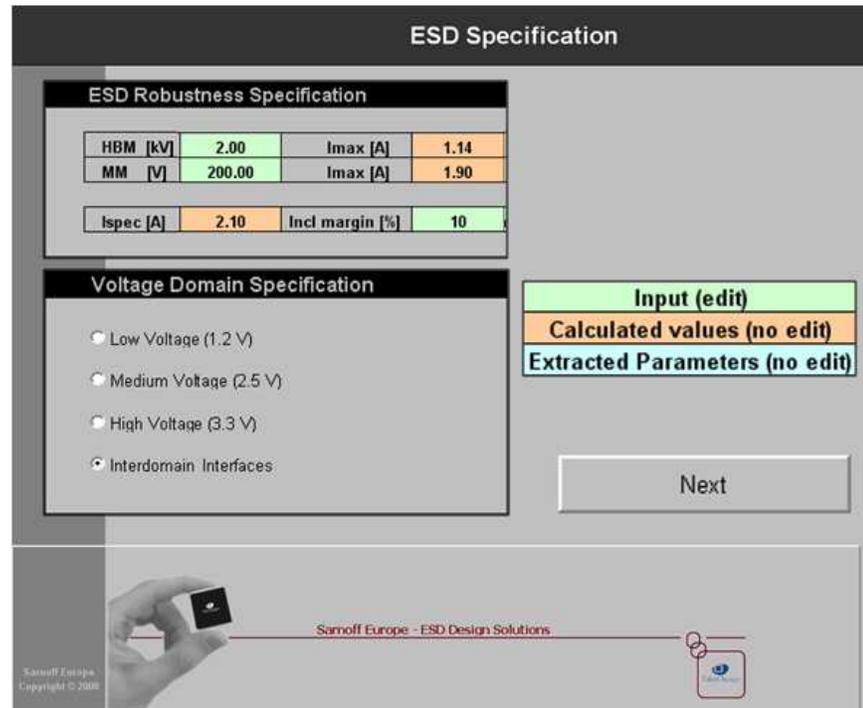

Figure 4: ESD specification window in the ESD tool. HBM and MM values are translated into corresponding ESD peak current values based on experimental data.
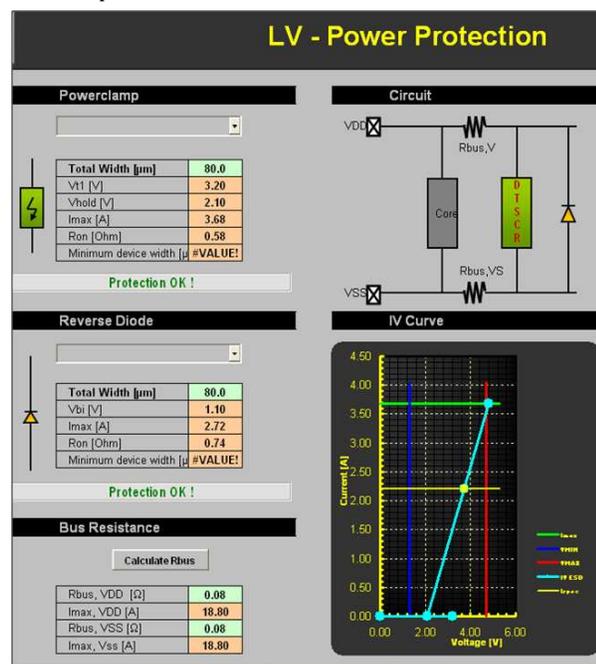

Figure 5: Power protection optimization screen. The example shows the protection selection for a thin oxide / core domain in a proprietary 65nm CMOS technology. Layout parameters of the power cell, reverse diode and the trade-off between the bus resistance on the repetition rate can easily be assessed.
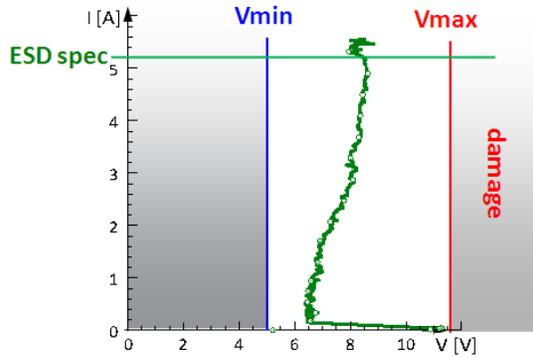
Figure 6: ESD design window concept depicted for a 5V clamp for a HDMI application. The white area between the vertical 'Vmin' and 'Vmax' lines and the horizontal 'ESD spec' line defines the ESD design window. If the clamp voltage goes beyond the Vmax line the sensitive elements connected to the IO pad risk being damaged. If the clamp conducts current below the Vmin line a latch-up risk exists. If the clamp fails below the ESD spec current level the ESD requirements will not be met. In this example 5A translates to 8kV HBM.

The ESD clamp selection must consider the following parameters:

- Normal operation signal voltage swing. ESD protection elements should remain off for all signal conditions during normal operation. This is called **'transparency'** of the ESD solution. It translates to a minimum Vt1 trigger voltage of the protection device – depicted as 'Vmin' on Figure 6. It is typically 10% - 50% above the Vdd level.
- Tolerated leakage. Each ESD clamp approach introduces an amount of leakage. It somehow translates back to the amount of ESD semiconductor junction area connected to the pad. Smaller ESD solutions have lower leakage. This also is considered in the **'transparency'**. Typically ASIC customers will define maximum amount of leakage at a certain IO voltage and temperature.
- ESD protection requirement. ESD clamps must be able to withstand a certain amount of ESD current without being damaged themselves. This is called **'robustness'** of the ESD clamp and is translated into a peak current level, defined as 'ESD spec'.
- Maximum voltage. The maximum voltage 'Vmax' in the ESD design window is defined by the IO elements connected to the IO pad. Every device type or combination has its own failure voltage. For instance, the 'Vmax' level is different when a gate is connected to pad or a transistor drain junction. Moreover, the ESD sensitivity of these elements is dependent on the

voltage rating. 3.3V IO devices are less sensitive than core devices. When a clamp can shunt all of the ESD current at a voltage below the failure of the sensitive node, the clamp is called **'effective'**.

The ESD design window must be carefully constructed for each stress combination. The ESD design tool provides an interactive approach to define the ESD design window 'Vmax' based on the schematic representation of the circuit attached to the IO pad. In a few iterations the IC designer can enter the most complex IO circuits. The tool considers all the different current paths and summarizes into the Design window (Figure 7).
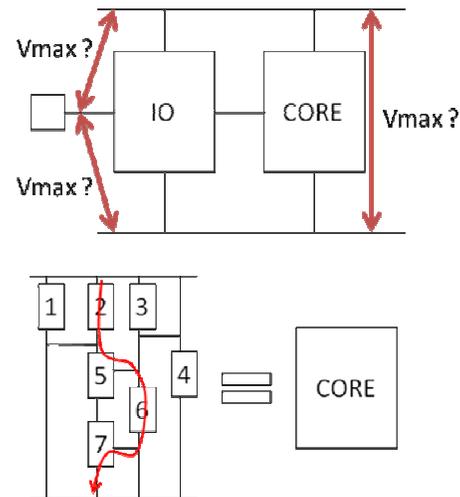

Figure 7: Determination of the maximum voltage is a crucial parameter in the ESD design flow. The design tool provides a 'design window definition' wizard that calculates the worst case situation based on the schematic representation of the IO circuit by dividing complex circuits into sub blocks.

The calculations are all based on comprehensive test chip analysis such as transient oxide breakdown and ESD behavior of many transistor variations such as size, silicidation and gate length. Once all the requirements for the ESD protection clamp are summarized in the ESD design window, the tool user can proceed to the protection definition.

3. Protection definition for IO's

Figure 8 depicts the IO protection definition wizard where the IC designer optimizes the ESD protection network for a specific IO. Different ESD elements are available (diodes, clamps 1-4, resistors) and through a user-friendly, intuitively 'point, click, change' method each element can be defined into the details of clamp type and size. For each foundry node, voltage domain, stress case and clamp number (1-4) different ESD devices are available to

the user. All of the ESD clamps are experimentally verified prior to inclusion into the tool.

Besides the optimization of the ESD network for ESD protection, the TakeCharge! ESD design tool provides additional features:

- Estimation of total parasitic capacitance connected to the IO pad. The capacitance values are based on Spice models supplied by the foundry. The influence of the pad voltage on the capacitance can be checked within the tool

- Determination of the IO leakage introduced by the ESD clamps at different ambient temperature. This is increasingly important for the low power Consumer Electronics gadgets running on batteries.

- Optimization of the clamp and total ESD silicon area depends on a number of factors. The current tool version includes a crude area calculation that will be fine tuned in the next release.

- Trade-off between the size of core, local clamps and bus resistance can be optimized.

Sarnoff Europe has invested in the past 5 years to port the silicon IP and ESD design tool to a very broad spectrum of foundry platforms evident from table 1.

Foundry	Tool available	ASIC production
TSMC	180nm, 130nm, 90nm, 65nm, 40nm	180nm, 130nm, 90nm, 65nm
UMC	130nm, 65nm	130nm
Toshiba	180nm, 130nm, 90nm, 65nm	180nm, 130nm, 90nm, 65nm
Tower	350nm, 130nm	350nm
Fujitsu	65nm	

Table 1: Availability of the ESD solutions and design tool for different foundries.

4. ESD design tool – examples

The ESD design tool is currently in use at leading semiconductor companies as well as small, fresh start-up fabless firms. In this section, measurement results are compared with the estimations from the ESD design tool. Two examples provide insight on how the ESD tool can significantly reduce the risk for expensive re-spins.

4.1 Example: 130nm TSMC technology

The first example highlights IC results in the TSMC 130nm CMOS technology. An ASIC for a medical application required a 2kV HBM protection level with an additional safety margin of 20%. Several samples are tested at 4 HBM levels. The results are summarized below. All the samples reached the target specification.

HBM Level	# samples	# Pass	# Fail
2kV	3	3	0
2.5kV	6	4	2
3kV	2	1	1
3.5kV	3	0	3

Table 2: Measurement results for the different stress combinations in the 130nm TSMC application. All samples reach the 2kV target specification.

4.2 Example: 5V 0.6um CMOS technology

A second example is based on a proprietary 5V 0.6um CMOS technology. The 10 pin power management IC required 200V Machine Model (MM) performance. A 20% safety margin was used for the calculations. The 8 IO's were stressed versus GND and VDD, 2 samples per case. From the table it is clear that all pins reach the required level. From a first view (table 3), one may argue that many pins are overdesigned for ESD protection.
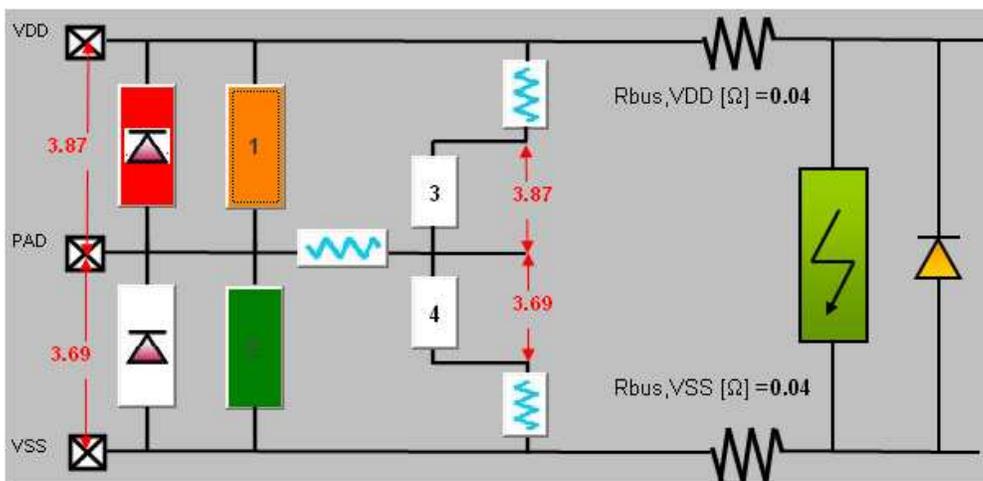

Figure 8: IO protection definition wizard where the IC designer can interactively calculate and optimize the ESD protection network for a specific IO. All of the elements in the GUI use the intuitive 'point, click, change' approach.

Chip pin		To GND	To VDD
Pin 1	+	400	400
	-	400	400
Pin 2	+	380-400	230-250
	-	400	230-250
Pin 3	+	400	320-380
	-	360	300-360
Pin4	+	400	260
	-	400	260
Pin 5	+	400	300-360
	-	400	300-360
Pin 6	+	400	280-360
	-	400	300-360
Pin 7	+	400	260-300
	-	400	260-300
Pin 8	+	400	400
	-	400	400

Table 3: Machine Model (MM) measurement results for the different stress combinations for the 0.6um CMOS power management ASIC. Two samples are used per stress combination.

There are various reasons why the actual results are higher than the calculated performance

- The design tool is used to optimize the worst case stress condition. For instance the circuitry between pin 1 to pin 8 is sensitive for ESD stress applied between those pins. Therefore, the local protection to VDD and GND is enhanced, leading to higher than required levels for other stress cases.
- The tool does not include parasitic current paths running through the functional circuitry of IC. The tool ensures that the sensitive circuitry never reaches a breakdown but in many cases the core circuitry can sustain a considerable amount of ESD current. Again, the design tool is build to provide protection for worst case situation where no ESD current through the core circuit is considered. The current through the circuit depends strongly on (transient) bias conditions which make it difficult to predict even for functional simulators.
- The clamp model includes safety margins to cover variations in the processing technology and variations in the HBM tester parasitic elements. That is one of the reasons why ESD performance varies between different samples as is eminent from the results table.
- IC designers simplify the ESD network creation through the definition of building blocks that protect certain IO types, independent of the distance to the nearest ESD power cell.

CONCLUSIONS

This publication provides an overview of the TakeCharge ESD design tool. It enables IC designers to calculate and optimize ESD performance. The tool uses a stepwise approach to cover all the stress combinations. IC designers can compare different protection strategies for each IO type and select the most appropriate ESD clamps for each application. The tool is customized per technology node and foundry. Behavior models for sensitive devices, ESD clamps and metallization are extracted from extensive measurements performed. The safety margins included in the calculations are based on experience in 8 CMOS generations.

Besides providing a robust and effective ESD network, the tool provides various degrees of freedom to minimize the influence of the ESD clamps on the functional performance. The IC designers can compare different ESD protection approaches and study the effect on consumed silicon area, induced leakage current, parasitic capacitance and target protection levels.

The toolset is used by both large, top-10 semiconductor companies and small fabless firms that have little or no ESD experience. A broad spectrum of applications such as ASIC's, FPGA's, LCD drivers, power, consumer and communications IC's are optimized with the tool. Two examples provide proof that the calculations before silicon production indeed provide a level of confidence required when developing ASIC's in advanced CMOS. To date, the ESD solutions included in the calculation tool provide protection in more than 450 IC's from various partners.

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About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include
- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

As is the case with many published ESD design solutions, the techniques and protection solutions described in this data sheet are protected by patents and patents pending and cannot be copied freely. PowerQubic, TakeCharge, and Sofics are trademarks of Sofics BVBA.

Version

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