



Conference paper Solving the problems with traditional Silicon Controlled Rectifier (SCR) approaches for ESD

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The Silicon Controlled Rectifier ('SCR') is widely used for ESD protection due to its superior performance and clamping capabilities. However, many believe that SCR based ESD protection is prone to latch-up, competitive triggering, long development cycles and slow trigger speed. This paper provides an overview of the problems and corresponding design solutions available.

Solving the problems with traditional Silicon Controlled Rectifier (SCR) approaches for ESD

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Abstract – The Silicon Controlled Rectifier (‘SCR’) is widely used for ESD protection due to its superior performance and clamping capabilities. However, many believe that SCR based ESD protection is prone to latch-up, competitive triggering, long development cycles and slow trigger speed. This paper provides an overview of the problems and corresponding design solutions available.

Introduction

Despite the efforts in prevention of charge build-up, Electro Static Discharge (‘ESD’) is still a very common cause for Integrated Circuit (‘IC’) failure. To protect the sensitive semiconductor chips against the harsh conditions during manufacturing, handling, transportation, assembly and use by the consumers, IC manufacturers include on-chip ESD protection circuits at the IO’s and power cells. Many different topologies, circuits and protection devices exist to achieve robust and effective ESD protection.

Early-on, the Thyristor or Silicon Controlled Rectifier (‘SCR’) was considered a perfect solution due to its superior ESD performance and clamping capabilities [1]. However, the use of the basic SCR brought with it a large number of issues such as latch-up, increased development and tuning cost, fab portability problems, ESD failures due to competitive triggering, CDM failures and a limited portability to advanced processes including SOI.

Although recent advances in SCR devices can solve most -if not all- of these problems, there is still a negative image associated with the SCR. This paper provides an overview of the problems and corresponding design solutions available.

After the introduction the typical problems related to SCR based ESD protection are summarized. For each of the topics, design solutions are demonstrated. Finally the benefits for the optimized SCR technology are highlighted in the conclusions.

I. SCR for ESD protection

The Basic SCR is constructed as a four layer (NPNP) element. The schematic, cross section in a P-substrate process and the typical IV curve are depicted in Figure 1. The N+/Nwell tie (G2) is connected to the anode while the P+/P-substrate tie (G1) is connected to the Cathode.

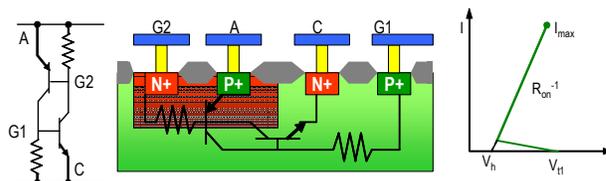


Figure 1: Basic SCR schematic, cross section and IV characteristic for Anode to Cathode stress.

This basic implementation has two inter coupled parasitic devices (lateral NPN and vertical PNP). The configuration creates a positive feedback once either one of the bipolar elements is turned on. The regenerative action is the key behind the snapback and low holding voltage (~1.2V) seen in the IV characteristic. At high currents, the structure behaves as an intrinsic PiN diode. To start the positive feedback, the Anode-Cathode voltage must exceed the Nwell/Pwell avalanche breakdown voltage. A measurement from a mature process technology (0.25um) is shown in Figure 2. Two problems are visible. Besides the low holding voltage, below the Vdd potential, a high Vt1 trigger voltage is visible. New SCR approaches have been introduced to cope

with this trigger problem such as the MLSCR and the LVTSCR (Figure 3) [2].

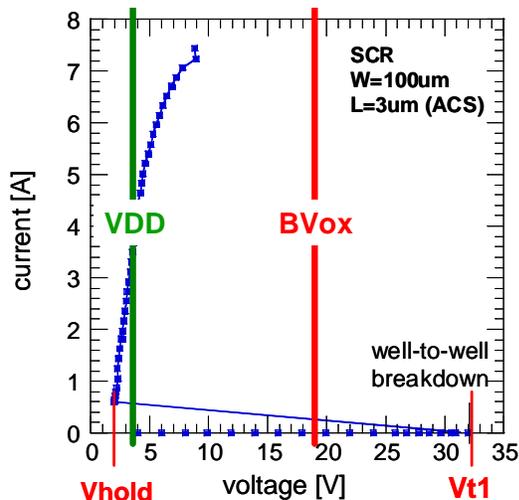


Figure 2: Characteristic IV curve for a basic SCR structure in a 3.3V – 0.25um technology. Due to the large Vt1 trigger voltage (Nwell/Pwell avalanche breakdown) the structure cannot protect the gate oxide (BVox). Moreover, the low holding voltage, below the VDD voltage can lead to latch-up problems.

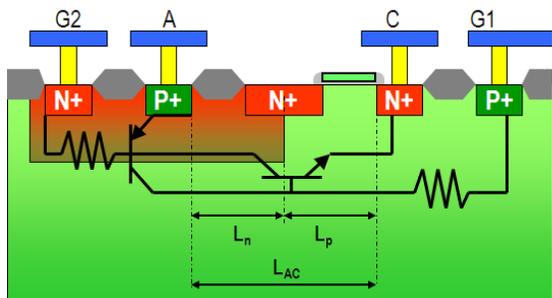


Figure 3: Characteristic cross section of the LVT-SCR (Low voltage triggered SCR). The additional N+ junction overlapping the Nwell/Pwell junction is inserted to drastically reduce the trigger voltage.

Certainly the LVTSCR has been widely used in industry in the mature process nodes. IC designers quickly realized the many benefits. The SCR is nearly an ideal switch device with low leakage in off-state combined with low impedance once triggered. Further, due to the very high ESD performance, area compact and low capacitance protection clamps can be created. However, the basic and LVTSCR did not solve all the problems. People reported latch-up problems due to the low clamping voltage. Moreover, it was difficult to correctly fit the SCR IV curve within the ESD design window. ESD engineers required a number of TEG runs to tune the trigger and holding voltage. Large semiconductor corporations noted serious IV curve fluctuations between their different fabrication plants. Further problems included difficulties to protect output buffers due to

competitive trigger issues, lower than expected CDM results due to slow trigger speed and integration problems into advanced technologies (STI isolation, SOI).

In the next sections, more information is provided for each of these reported issues. Examples from different technologies and mass produced products solutions are presented based on Sarnoff Europe's SCR solutions. When the optimized SCR devices are combined with the right process and product expertise the SCR device brings a great deal of benefits as detailed in section III.

II. Common SCR fears

When ESD designers discuss about Silicon Controlled Rectifiers it seems that all of them have suffered from some of the problems in the past. Most of these problems can be solved through improved SCR design as shown in the next 5 sections.

II.A Latch-up concerns

Latch-up problems are probably feared the most when Silicon Controlled Rectifiers are used. Because the holding voltage is only about 1.2V which is below the Vdd potential in most applications, a latch-up situation can easily occur. The main condition is that the ESD device is triggered during biased condition of the IC and that it opens a continuous current path that draws an over-current from the supply.

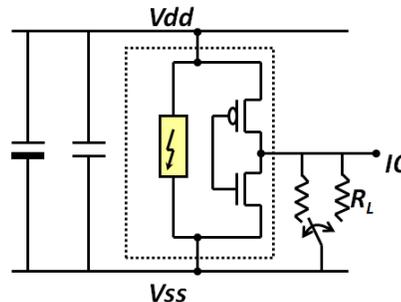


Figure 4: Simplified example of a latch-up situation. Through the sudden change of the external load impedance, noise can be induced on the Vdd or Vss lines. Similar problems can occur through the switching events internal of the IC

Such unexpected triggering can occur through different scenarios where noise is applied at the supply lines or IO pads:

- Over voltage applied at the IC terminals. If the applied voltage is higher than the trigger voltage the SCR is triggered. This can occur through wrong user interaction or through inductive effects.

- ESD stress applied during biased conditions. Such events mainly occur in automotive and industrial applications.
- Other noise events such as photo current are mainly important in space applications.

Based on these examples it is possible to define different constraints for the application of SCR based ESD protection:

Holding voltage engineering

For certain CMOS applications the holding voltage can easily be increased above V_{dd} by adding diodes in series with the SCR. This is demonstrated in Figure 5 below. Another possibility is to stack multiple SCR's in series.

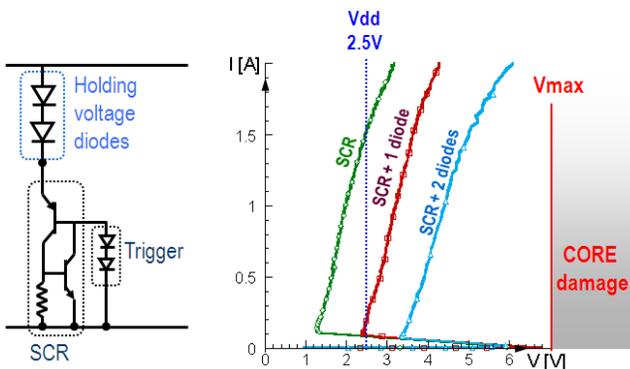


Figure 5: Increased holding voltage by adding series elements at the Anode of the SCR. This example shows that 2 additional diodes can make the SCR protection latch-up immune for 2.5V power lines. This technique can be applied up to 3.3V applications in most technologies.

Trigger point engineering

The trigger voltage and trigger current of the protection clamp must and can be increased above absolute maximum ratings. By applying a separate trigger element the latch-up conditions can be shifted to this trigger element [3,4]

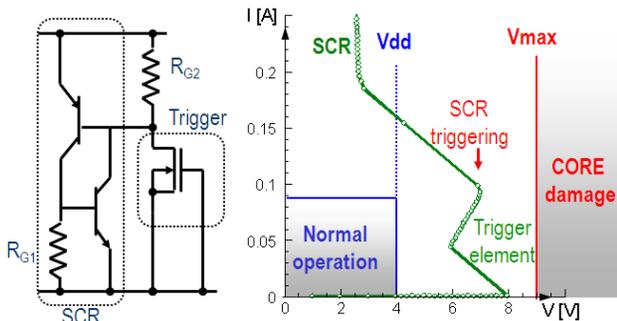


Figure 6: Increased trigger condition, above maximum noise at V_{dd} lines. The external trigger element is sized up to sustain larger trigger current. R_{G1} and R_{G2} shunt resistances are reduced to a low value like 5 ohm.

Holding current engineering

Besides a sustaining voltage (V_{hold}) every SCR has a certain holding current I_{hold}. If the current through the SCR is made smaller than I_{hold}, the positive feedback mechanism is interrupted. The holding current can be increased with special layout technique called Anode/Cathode segmentation to reduce the effective Nwell/Pwell resistance as shown on Figure 7. [3]

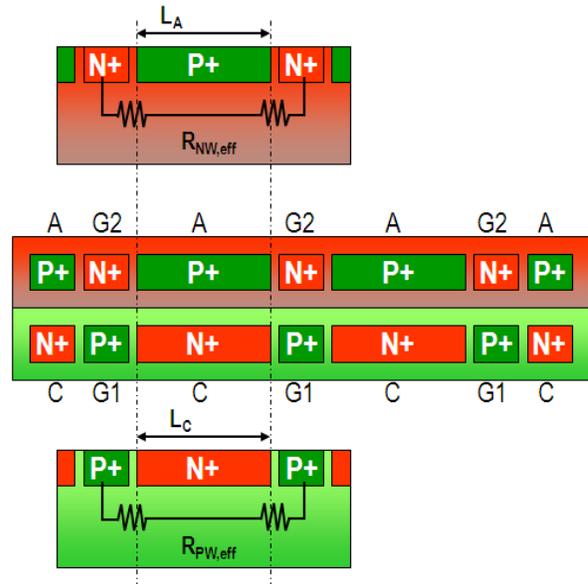


Figure 7: Segmented Anode and Cathode to reduce the effective well resistance increases the holding current and reduces latch-up issues.

These SCR improvements were applied at a number of IC products in mass production available today, including over 50 IC's in high voltage applications where the latch-up problem is even more threatening. The example below (Figure 8) is an OKI LCD driver IC where the SCR protection was included at the high voltage power cell. High latch-up immunity of >300mA was achieved.

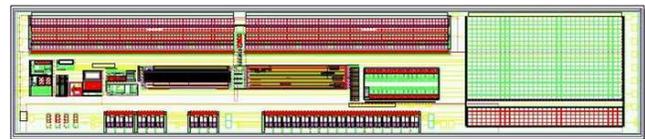


Figure 8: High voltage 0.5um – 42V LCD driver application including SCR based ESD protection. Due to the use of SCR protection, the robust ESD protection (6kV HBM, 250V MM) consumes only a small area. Due to the use of SCR improvement techniques (segmented layout, low shunt resistance, LU immune external trigger element) the latch-up immunity was very high: >300mA current injection and 1.5x overvoltage at V_{dd}, both according to JEDEC78. Further a CCL level of 200V was achieved in the same product family.

II.B Process tuning and fab portability

Due to the many benefits of SCR based ESD clamps several ESD designers have included SCR's in the protection approach of their ASIC's. All kinds of trigger and clamping options were conceived similar to the LVTSCR [2] in the late 1980-ties whereby the trigger circuit is integrated within the SCR body. Triggering mostly relied on avalanche breakdown. However, people quickly realized that these SCR types required extensive silicon experiments to tune the trigger and clamping behavior to match the ESD design window. Typically, layout improvements to control the trigger behavior also influenced the clamping behavior. Many companies reported issues when these SCR based protection schemes were ported to different fabs: even minimal process variations induced a strong influence on the ESD behavior because non standard elements were used. Many people lost faith in the Silicon Controlled Rectifier.

A solution to this problem was presented in 2001 [5]. In the new approach the trigger and clamping behavior are separated from each other such that both aspects can be controlled independently. The SCR clamping behavior (ESD robustness, resistivity, trigger speed) is optimized by minimal Anode-Cathode spacing (LAC) and close to the parasitic base triggering. The trigger behavior is controlled separately through the use of external trigger elements based on controlled devices such as resistors, diodes, MOS transistors. Several variations have since been used [6-7] (Figure 9).

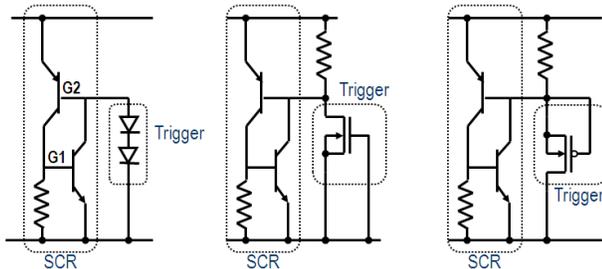


Figure 9: Overview of trigger options for SCR based ESD protection. The trigger behavior can be controlled independently from the clamping device. Because standard devices are used in the trigger scheme the portability between fabs and process nodes is guaranteed. Note that similar approaches are obvious with G1 instead of, or in addition to, G2 triggering.

This new approach is currently used in several hundred mass produced IC's in at least the eight most recent CMOS generations. Consistent ESD behavior is achieved. In Figure 10 Diode Triggered SCR (DT-SCR) devices on different process corners are

compared in a 65nm process technology. Almost no variation is visible.

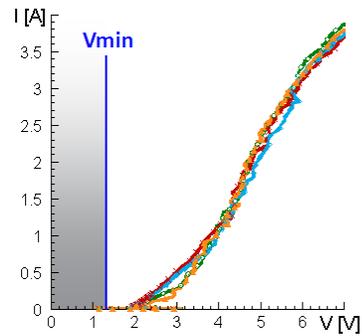


Figure 10: No variation visible on the different process corners in a 65nm CMOS technology. SCR devices processed under different process corners (TT, FS, FF, SS) are compared to verify that the clamping behavior does not degrade due to process variations.

II.C SCR trigger speed for CDM protection

Despite some of the problems with LVTSCR's as detailed above different corporations are still using the device as ESD protection clamp. In 2000, Wu and Rosenbaum discovered yet another problem when the LVTSCR device (Figure 3) is used in advanced CMOS technology [8]. They provided proof that the LVTSCR device did not respond fast enough to some ESD transients similar to CDM. The device was unable to protect a thin gate oxide monitor connected in parallel for pulses with a rise time of 1ns.

The new solution introduced in 2001 by Russ et al. [5] did overcome this trigger speed issue. An example is shown in Figure 11 where a thin oxide (1.4nm in 65nm CMOS) gate monitor device is protected using a Diode Triggered SCR (DT-SCR) clamp even for an ultra-fast applied rise time of 200ps. Recently, various independent sources have provided proof of CDM protection capabilities of the Sarnoff DT-SCR [9-12].

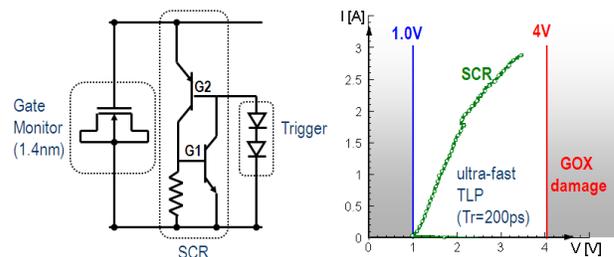


Figure 11: Silicon proof of effective protection of a thin oxide core monitor transistor in 65nm CMOS technology. The DTSCR protection clamp reacts fast enough to protect the sensitive element even under ultra-fast rise time (200ps) stress pulses.

Russ concluded that the main problem with the LVTSCR was the large Anode-Cathode distance

(LAC) due to the integrated trigger junction. When the SCR device is optimized (shortest LAC - Figure 12) and external trigger element is correctly defined the protection device is fast enough.

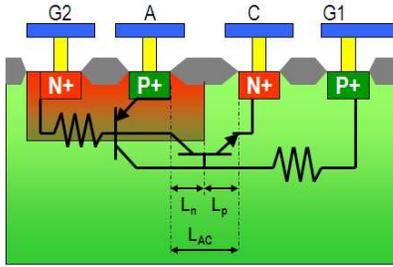


Figure 12: Schematic cross section of the optimal SCR ESD clamp. The anode-cathode distance is minimized to improve the device turn-on time. Because the trigger element is integrated in the LVTSCR device (Figure 3) its LAC is considerably larger leading to slow triggering.

II.D Competitive triggering

For the ESD protection of output buffers people have long relied on the intrinsic ESD properties of the parasitic bipolar device within the MOS transistors. Certainly in mature technologies this strategy is both simple and adequate. Through the application of silicide and LDD blocked drains the same approach was extended to more advanced CMOS technologies. Because of the severe silicon area consumption for this NPN based protection, many ESD designers have looked at smaller alternatives such as the LVTSCR.

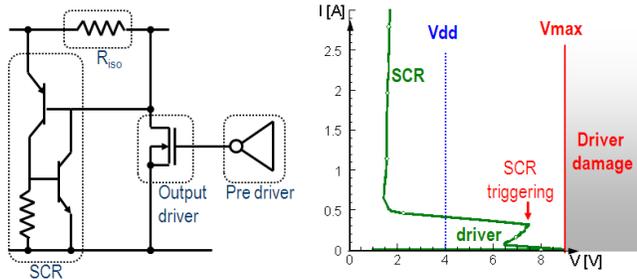


Figure 13: Schematic approach for the RT-SCR ESD clamp. The SCR triggering is controlled by the ESD current flow through the sensitive output driver. The trigger condition is tuned through the value of the Isolation resistance. Effective protection is achieved with only a minimal resistance added in the IO pad.

However, the application of the LVTSCR as a parallel protection element for the NMOS output transistor resulted in ESD failures due to competitive triggering. Both the sensitive buffer element and the clamp device have a very similar trigger mechanism: avalanche breakdown of an N+/Pwell junction. Furthermore, the trigger voltage of the sensitive output buffer NMOS device is reduced due to the undefined potential at its gate. This resulted in a broad statistical spread of the protection performance

when the NMOS driver is triggered into NPN conduction before the LVTSCR.

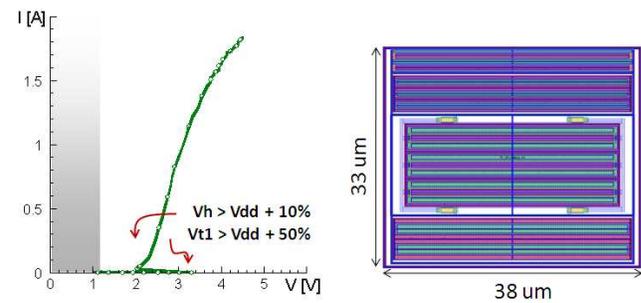
In 2005, Van Camp et al. introduced a straight forward solution to the problem of competitive triggering [13] (Figure 13). The sensitive device was promoted to become the trigger device for the SCR clamp. Instead of detecting ESD as an overvoltage stress, this RT-SCR approach relies on the detection of an excess current flowing through the sensitive elements in an output buffer. A small resistance of about 2 ohm is added in series with the output buffer.

II.E Advanced technologies

When Shallow Trench (STI) isolation replaced Field Oxide (FOX) schemes, many process engineers believed that the SCR benefits would disappear due to the much deeper isolation. Further it was believed that SCR based protection was not possible in SOI technology. Both statements proved to be wrong.

Marichal [14] provided information about the construction and application of SCR devices in SOI technologies. A special layout technique is needed to create the Nwell/Pwell junction and to connect the NPN/PNP bases.

Further, based on recent measurements on 40nm process technology, there is no reason to write-off the SCR approach for ESD protection in the most advanced CMOS nodes (Figure 14).



Core clamp	HBM	Holding voltage		Leakage	
		25°C	125°C	25°C	125°C
0.9V	>3.5kV	>2V	>1.6V	45pA	83nA
1.2V	>3.0kV			59pA	97nA
1.5V	>4.5kV	>3V	>2.5V	45pA	55nA
1.8V	>3.0kV			60pA	63nA

Figure 14: IV curve and layout view (top) of a DT-SCR based core protection in the 1.2V domain in the TSMC 40nm technology. The SCR based protection clamps are optimized for low leakage current, ideal for mobile consumer applications as is evident from the table (bottom). Clamp HBM performance and leakage results are calculated from measurements on an comprehensive ESD TEG.

Conclusions

Many ESD engineers do not like to use SCR based ESD protection related to bad experiences in the past such as latch-up, competitive or slow triggering and long development cycles with early LVTSCR-like device types. This paper reviewed and explained these issues and provided design solutions to cope with each problem.

Latch-up immunity problems can be solved, even for High Voltage process technologies, by careful SCR design. The paper provided demonstration of mass produced ICs where the SCR power clamp is made latch-up immune to high current injection, even at high temperatures.

The common experience of long development cycles and extensive process tuning required to fine-tune basic SCR triggering behavior can be solved easily through the use of external trigger circuits coupled to the G1/G2 well ties. The trigger circuits can be based on standard and well characterized elements (diode, MOS, resistor).

Many publications in the past have pointed to the slow trigger speed of the SCR as a main problem. The paper showed examples and references where recent innovations in SCR design can lead to effective ESD protection even for fast transients including CDM and IEC stress.

Finally, the optimized CMOS SCR structure has been ported to various technologies including SOI, BCD and HVCMOS where it is used as an effective ESD protection structure without influencing the normal operation conditions and bringing great benefits.

It is clear that when the optimized solutions are combined with strong expertise, the Silicon Controlled Rectifier device can be safely used for ESD protection bringing great benefits like reduced ESD area, low parasitic capacitance, low leakage current and excellent clamping behavior.

As is the case with many published ESD design solutions, most of the techniques and protection solutions described in this paper are covered under patents and cannot be copied freely.

Acknowledgements

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About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.



ESD SOLUTIONS AT YOUR FINGERTIPS

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
 - Enable unique requirements for Latch-up, ESD, EOS
 - Layout, metallization and aspect ratio customization
 - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

As is the case with many published ESD design solutions, the techniques and protection solutions described in this data sheet are protected by patents and patents pending and cannot be copied freely. PowerQubic, TakeCharge, and Sofics are trademarks of Sofics BVBA.

Version

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