



Conference paper **Analysis Methodology for Latch-up: Realistic Worst Case Stress Conditions for the Current Injection 'I-test'**

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When designing and characterizing process-, ESD- and I/O-TEG test chips for latch-up, there is a need to define the worst case stress conditions. Therefore, this paper provides guidelines for designing realistic worst case test structures for latch-up characterization. Furthermore, recommendations are provided regarding the use of a solid state voltage pulse generator in order to apply a realistic worst case stress approach to analyze for the standard current injection ('I-test') test defined by JEDEC/JEITA.

# Analysis Methodology for Latch-up: Realistic Worst Case Stress Conditions for the Current Injection ‘I-test’

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**50 Words Abstract** – When designing and characterizing process-, ESD- and I/O-TEG test chips for latch-up, there is a need to define the worst case stress conditions. Therefore, this paper provides guidelines for designing realistic worst case test structures for latch-up characterization. Furthermore, recommendations are provided regarding the use of a solid state voltage pulse generator in order to apply a realistic worst case stress approach to analyze for the standard current injection (‘I-test’) test defined by JEDEC/JEITA.

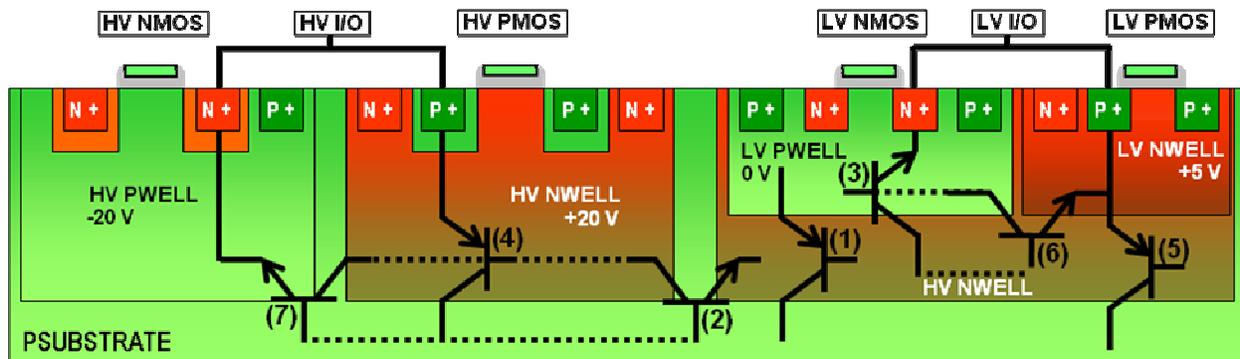


Figure 1: Cross-section and some identified parasitics for the process technology used in this study. Both high-voltage (HV) and low-voltage (LV) MOS devices are available. Parasitics (2), (3) and (7) are NPN bipolar parasitics. Parasitics (1), (4), (5) and (6) are PNP bipolar parasitics. At least three parasitic SCRs are formed by combination of the NPN and PNP parasitics: SCR (2&4) is formed by NPN (2) and PNP (4), SCR (3&6) is formed by NPN (3) and PNP (6), SCR (4&7) is formed by NPN (7) and PNP (4). Because the combination of NPN (2) and PNP (4) is one of the most ‘sensitive’ parasitic SCRs for latch-up, SCR (2&4) is the subject of this study.

## I. Introduction

Besides ESD qualification and functional verification, latch-up testing on ICs is an important aspect of product reliability. New application types (motor drivers) and harsh environments (automotive, industrial) add more stringent latch-up requirements to the process technology. Due to the strong competition in the commodity market for H-bridge ICs, DC-DC converters and other power management ICs, it is extremely important to evaluate the latch-up properties of the basic elements and device concepts before they are included into a final IC product. As Figure 1 shows, for a LV and HV IO, several parasitic NPNs and PNPs are inherently present in the IO or between the IOs. These parasitic NPNs and PNPs can latch on their own, or they

can form parasitic SCRs, which are even more latch-up prone. A detailed latch-up characterization program is needed to evaluate the latch-up sensitiveness of the basic IO elements and their parasitics.

Figure 2 presents an overview of such a generic 6-step program conducted to define latch-up rules for a selected process technology. After a detailed study of the process technology and the design rules (step 1), the different parasitic devices are identified (step 2). The parasitic identification relies on a careful investigation of the device cross-sections. Important in this step is to prioritize the most dangerous parasitics and to eliminate the ‘safe’ parasitics (by also considering the bias conditions). Defining appropriate test structures (step 3), and executing a general and detailed silicon analysis (step 4 and 5) are very typical steps for any latch-up process characterization.

Finally, based on detailed measurements and analysis, latch-up rules are derived (step 6).

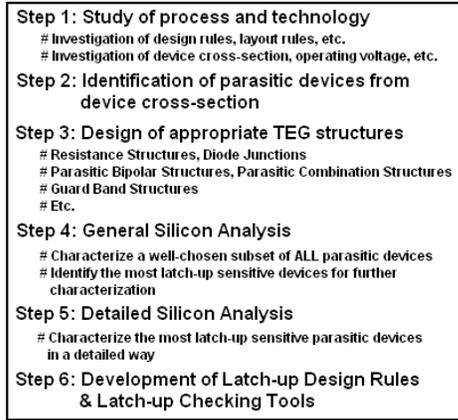


Figure 2: Generic 6-step latch-up design rule program flow.

The paper has 5 sections: First, in Section II, the process technology and the parasitic devices are introduced. The next section summarizes the two most commonly used latch-up qualification tests (current injection ‘I-test’ for I/O pins, and over voltage ‘V-test’ for supply pins). Further, in section IV, two approaches for the ‘I-test’ are compared. In section V, the worst case conditions are defined, such that latch-up properties for complex ICs can be guaranteed. The paper concludes with basic guidelines for ‘I-test’ analysis interpretation, based on solid-state voltage pulse generator equipment.

## II. Technology and Devices

Figure 1 provides an overview of the HV and LV MOS devices available in the investigated  $\pm 20V$  HV-CMOS technology. Many different parasitic devices can be identified in the technology. This study focuses on the SCR combination of parasitic (2) (lateral NPN between LV and HV NWell) and parasitic (4) (vertical PNP between HV P+ diffusion and P-substrate), as it is one of the most ‘sensitive’ parasitics, considering latch-up.

The parasitic SCR detection, mentioned in step 2 of the generic latch-up characterization program of the previous section, consists of identifying ALL possible PNPN structures, whereby the base of the NPN is also the collector of the PNP, and the base of the PNP is also the collector of the NPN, i.e. the biasing ultimately determines whether the PNPN structure is a latch-up sensitive parasitic SCR or not. Careful investigation of the cross-section of Figure 1 results in at least 6 possible parasitic SCR structures. Further careful analysis of the biasing schemes for these 6 parasitic SCR ‘candidates’, eventually results in 3 ‘real’ parasitic SCRs.

E.g. PNP (1) and NPN (3) are interconnected as a PNPN structure, but the biasing prohibits latching SCR action. The same is true for the combination of PNP (1) and NPN (2), and the combination of NPN (2) and PNP (5). In a few other cases, the parasitic NPN and PNP are connected as a PNPN structure, and the biasing scheme is such that the PNPN structure is latch-up sensitive. The combination of

NPN (2) and PNP (4) forms an SCR with the anode biased 25 V positive with respect to the cathode, during worst case latch-up test conditions. The SCR combination of NPN (2) and PNP (4) connects the HV with the LV domain. This SCR can be weakened by increasing the spacing between N Wells of the LV and HV domain. The combination of NPN (3) and PNP (6) forms an SCR with the anode biased 7.5 V positive with respect to the cathode, during worst case latch-up test conditions. The combination of NPN (3) and PNP (6) SCR is entirely located in the LV domain, and is inherently present in a LV output or I/O. Finally, the combination of PNP (4) and NPN (7) forms an SCR with the anode biased 50 V positive with respect to the cathode, during worst case latch-up test conditions. The SCR combination of PNP (4) and NPN (7) is entirely located in the HV domain, and is inherent to a HV output or I/O.

## III. Latch-up Test Overview

Two tests are widely used in the industry to qualify finalized product ICs for latch-up: the I/O current injection ‘I-test’ and the supply over voltage ‘V-test’ (Figure 3).

The ‘V-test’ is applied at the V<sub>dd</sub> pins of the circuit and is mainly relevant to detect latch-up caused by avalanche multiplication in parasitic elements.

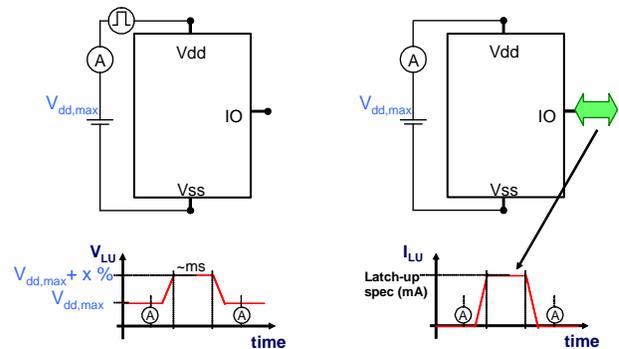


Figure 3: Overview of the two most commonly used latch-up tests for ICs: supply over voltage test (‘V-test’, left side) and I/O current injection test (‘I-test’, right side).

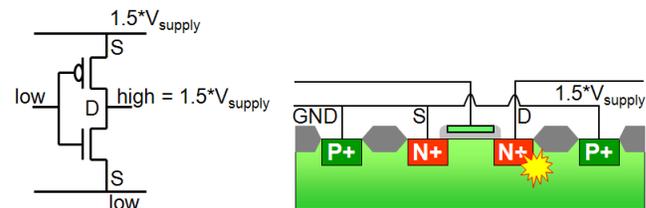


Figure 4: Example of ‘V-test’ applied at an inverter structure. The PMOS source is biased at  $1.5 * V_{supply}$ . When the inverter gate is pulled low, the PMOS drain is pulled high, increasing the NMOS drain potential leading to an increased avalanche current generation at the NMOS drain-bulk junction, which can lead to triggering of the intrinsic parasitic NPN device.

An example of the ‘V-test’ is shown in Figure 4 where the supply voltage is increased by 50% (typical specification). Depending on technology, such an increased potential could generate avalanche multiplication current at the drain-well junction, possibly triggering the parasitic bipolar devices (NPN in NMOS, PNP in PMOS).

During the ‘I-test’, a fixed current pulse (typical 100 mA) is forced into the I/O terminal. Such injection is shown in Figure 5.

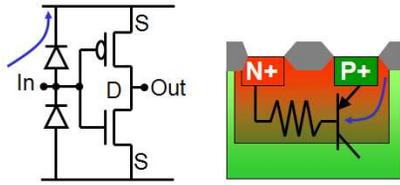


Figure 5: Applied ‘I-test’ at an input pad, protected with a dual diode approach. The stress forward biases the P+/Nwell junction in the ‘diode up’ which leads to injection of holes into the substrate through the vertical PNP.

Positive current injection at an I/O pad typically injects holes into the substrate that subsequently flow through the P+/substrate connection(s) to the ground bus. However, before reaching the guard band the holes can forward bias P-substrate/N+ or P-substrate/Nwell junctions leading to a latch-up situation [1] [2].

Both ‘I-test’ and ‘V-test’ are standardized by several organizations such as JEDEC [3] and JEITA [4], and provide only a ‘pass/fail’ result for IC qualification. However, during CMOS process technology development, a more detailed analysis is required. In this study, the ‘I-test’ and ‘V-test’ are mimicked through the use of solid state pulse generators [5] and current measurement through digital oscilloscopes. Figure 6 shows such an accurate current measurement where the sudden increase in collector current of a NPN device signals when the device is triggered into latch-up.

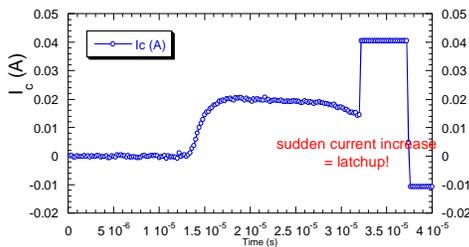


Figure 6: NPN collector current versus time during nearby substrate current injection. At a certain time (32 us) the NPN device is latched (current measurement is clipped at 40 mA by the scope input). Before latch-up occurs, the bipolar conduction can be measured (~20 mA).

## IV. Voltage versus Current Source

The ‘I-test’ can be performed through two test approaches as shown by Figure 7: on the right side, the current injection is realized through a current source, while on the left side a voltage pulse generator is used to inject current into the NPN base terminal. Both approaches generate identical collector current versus emitter current ( $I_c$  vs.  $I_e$ ) behavior.

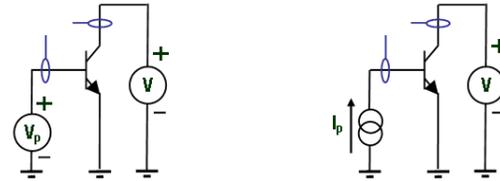


Figure 7: The current injection test (‘I-test’) can be performed with two approaches. On the left, the ‘I-test’ is simulated through the use of a voltage pulse generator used as voltage source with amplitude ‘ $V_p$ ’. Measurement probes at base and collector are used to analyze the current versus time. On the right, a real current pulse is injected at the base of the NPN parasitic.

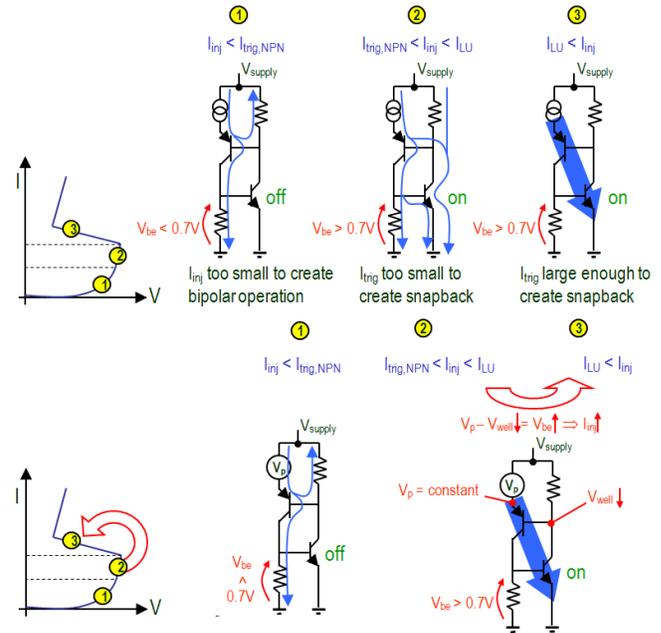


Figure 8: Stepwise increase (1-2-3) of injected current, and corresponding current flow visualized in the SCR schematic. When the ‘I-test’ is performed with a current source (top figures) the injected current is limited and the positive SCR feedback is prohibited. When a voltage pulse generator is used (bottom figures) the current is not limited, and the SCR is triggered into a low ohmic state as soon as the NPN device is turned on, as this initiates the positive feedback mechanism.

The main difference between the two approaches is related to the current limitation for the injected current in the base terminal. A current source provides a constant –and thus limited– current level to the base-emitter junction. A voltage source on the other hand, has a low output impedance, to ensure a constant voltage, independent of the load current. This leads to an uncontrolled behavior, as evident from Figure 8. It is obvious that the use of a voltage pulse generator for the analysis of the current injection latch-up properties of a SCR parasitic represents a worst case condition.

The difference between the two approaches is confirmed by measurements on ‘simple’ SCR test structures, containing parasitic NPN (2) and PNP (4).

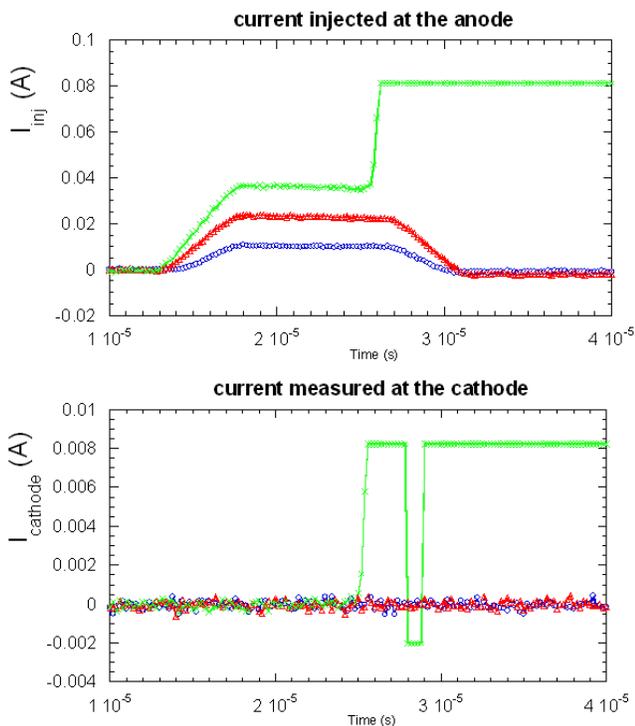


Figure 9: Current injection by using a voltage source on PNP of SCR (2&4). Because the current is not limited, latch-up occurs as soon as NPN (2) goes into bipolar operation. 38 mA is injected into the emitter of the PNP (4).

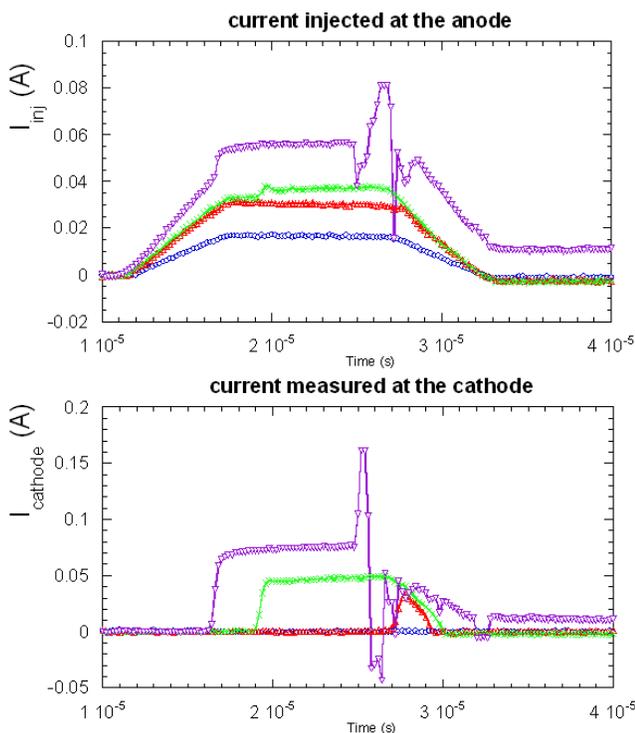


Figure 10: Current injection by using a current source on PNP of SCR (2&4). Because the current is limited, latch-up does not occur as soon as NPN (2) goes into bipolar operation. 56 mA needs to be injected into the emitter of the PNP (4), before latch-up occurs.

Figure 9 shows that in case current injection is performed by using a voltage source on the PNP of SCR (2&4), latch-up occurs as soon as NPN (2) goes into bipolar operation.

This happens when 38 mA is injected into the emitter of the PNP (4). For lower injection currents, the NPN is not turned on (Figure 9, red triangles and blue circles). Figure 10 shows that in case current injection is performed by using a current source on the PNP of SCR (2&4), latch-up does not occur as soon as NPN (2) goes into bipolar operation. In this case, 56 mA needs to be injected into the emitter of the PNP (4), before latch-up occurs. For lower injection currents, the NPN is already conducting current, while no latch-up occurs (Figure 10, green crosses).

## V. Realistic Worst Case I/O Latch-up Test Structures

In many cases, for investigating the latching characteristics of a parasitic SCR device, 'simple' test structures are used which contain (parameter variations of) the parasitic SCR, but which do mostly not contain the other parasitic devices found in a real I/O.

In this section, we will show that there is a complex interaction between the different parasitics usually found in a real I/O. This interaction influences the latch-up behavior in two ways, at the same time: (1) the existence of extra parasitics might lead to lower levels of latch-up triggering (i.e. detrimental effect), (2) at the same time, the existence of extra parasitic devices might also shunt some current away from the substrate, leading to higher levels of latch-up triggering (i.e. beneficial effect). Both effects are present in a real I/O, and cannot be captured by the 'simple' (single-SCR) test structures. Therefore, there is a need for using more 'complex' (multi-SCR) test structures, mimicking a real I/O with its different parasitics.

Figure 11 depicts such a special test structure, where 2 P+ diffusions are incorporated in the HV NWell. This corresponds to the realistic case of a PMOS device in a HV output or I/O driver. In this case, two vertical bipolar PNPs (parasitic (4) and parasitic (4')) are present.

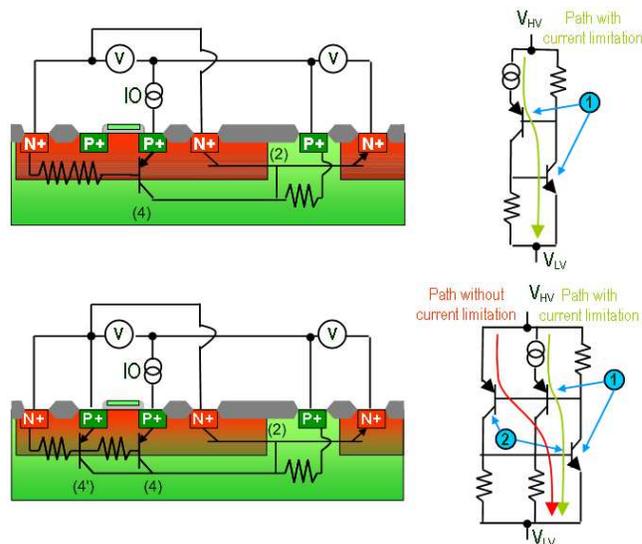


Figure 11: 'I-test' measurement setup for 'complex' test structure. In the top figure only one PNP is connected. In the bottom figure both PNPs are connected, mimicking a real I/O

When performing a (positive) constant current injection latch-up test ('1-test') on the HV output, current is forced into the drain of the PMOS (see also Figure 12). As such, parasitic SCR (2&4) (combination of NPN (2) and PNP (4)) is driven by a current-limiting current source (as the JEITA/JEDEC standard describes). However, in the real case of a HV I/O, an additional SCR (2&4') is also present (see Figure 14). Because SCR (2&4') is biased by a voltage supply – and thus not current-limited – this SCR will be the SCR that latches more easily, even when injecting on the anode of SCR (2&4) (the output node). In order to determine realistic worst case conditions for latch-up testing, both in terms of test structure design and current injection method, 3 different setups (Figure 12 to Figure 14) are compared.

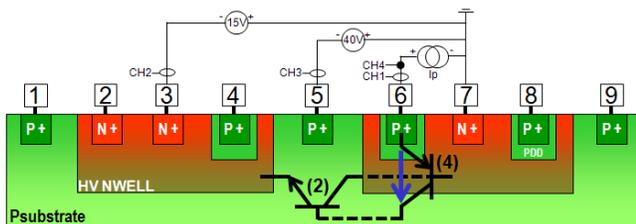


Figure 12: Setup 1: Injection on vertical PNP of SCR (2&4) by using a current source. Only SCR (2&4) is stressed.

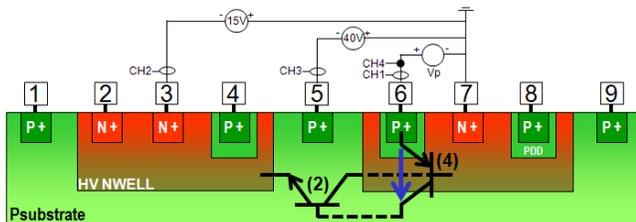


Figure 13: Setup 2: Injection on vertical PNP of SCR (2&4) by using a voltage source. Only SCR (2&4) is stressed.

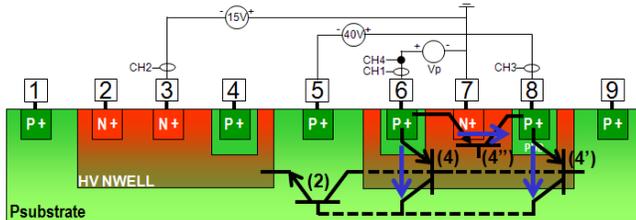


Figure 14: Setup 3: Injection on vertical PNP of SCR (2&4) by using a current source. Because the drain of the HV PMOS is connected to  $V_{supply}$ , an extra vertical PNP (4') and a lateral PNP (4'') are present. Vertical PNP (4') forms an additional SCR (2&4') with NPN (2).

Figure 12 shows the case where only parasitic SCR (2&4) is connected and injection occurs through a (current-limiting) current source  $I_p$  (setup 1). In this case, latch-up is triggered for an injection current of 84 mA. This result is derived from the waveforms for the injection current  $I_{inj,LU}$  (Figure 15) and the cathode current  $I_{cathode,LU}$  (Figure 16).

Figure 13 shows the case where only SCR (2&4) is connected and injection occurs through a (non-current-limiting) voltage source  $V_p$  (setup 2). From the measurements, it can be seen that in this case the injection current needed for triggering latch-up ( $I_{inj,LU}$ ) is only 36 mA. As has been explained in Figure 8, the SCR latches as

soon as the NPN starts bipolar action, because the increased demand for current, due to positive feedback, will easily be fulfilled by the non-current-limiting voltage source.

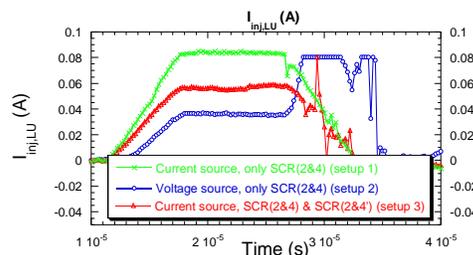


Figure 15: The injection current waveforms triggering latch-up ( $I_{inj,LU}$ ) (for the 3 different setups).

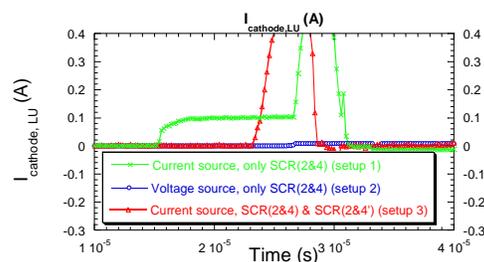


Figure 16: The cathode current waveforms for the injection steps triggering latch-up ( $I_{cathode,LU}$ ) (for the 3 different setups).

Figure 14 shows the case where both SCR (2&4) and SCR (2&4') are connected, as in a real I/O, and injection occurs through a (current-limiting) current source  $I_p$  (setup 3). From the measurements, it can be seen that the injection current needed for triggering latch-up ( $I_{inj,LU}$ ) is 56 mA. Setup 3 corresponds to the realistic case where the drain of the PMOS is connected to  $V_{supply}$ , and latch-up testing occurs by means of constant current injection on the I/O.

The latch-up trigger current results ( $I_{inj,LU}$ ) for the three setups are also listed in Table 1.

	Setup 1	Setup 2	Setup 3
	Current source; only SCR (2&4)	Voltage source; only SCR (2&4)	Current source; SCR (2&4) & SCR (2&4')
$I_{inj,LU}$	84 mA	36 mA	56 mA

Table 1: Comparison between the injection current needed for triggering latch up ( $I_{inj,LU}$ ) for three different setups.

The question now arises: which are the most recommended latch-up testing conditions? From our setup experiments, it is clear that a primary requirement, for accurate latch-up characterization, is to design 'complex' test structures, which do not only incorporate the parasitic SCR present between output pin and ground, but which do also contain the other parasitic SCRs and bipolars present in the I/O.

The measurement results of setup 1 show that, if one uses 'simple' test structures, incorporating only the SCR present between I/O pin and ground pin, by using constant current injection, one obtains a too optimistic latch-up trigger current. In this case, the measurement suggests that latch-up is only triggered by injecting 84 mA of injection current at the I/O pad. As setup 3 demonstrates, in a more realistic case, latch-up will be triggered for a lower injection current (of 56 mA), because the parasitic SCR (2&4') between  $V_{supply}$  pin and ground pin, is not limited in current, and

latches more easily. However, in the case one is limited to using ‘simple’ parasitic SCR test structures, it is recommended to use a non-current-limiting voltage source instead of a current-limiting current source.

How can the differences in latch-up trigger current be explained? The anode current of SCR (2&4’) is measured through a CT-2 Tektronix current probe, connected to channel 3 (CH3) of the oscilloscope (Figure 14 and Figure 18). The measurement of the current at the anode of SCR (2&4’), shows that just before latch-up a lateral current of 5.5 mA flows through the lateral PNP (4’), formed between the two anodes of the two parasitic SCRs (Figure 18).

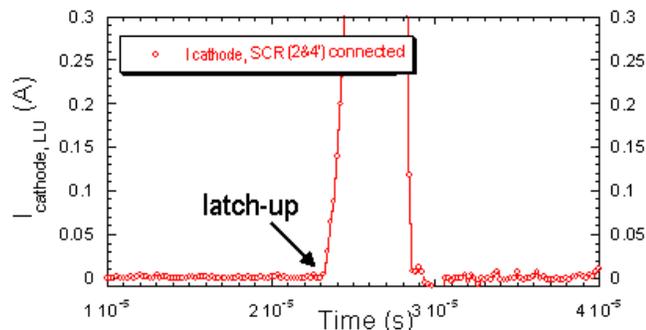


Figure 17: Cathode current for the parasitic SCRs for setup 3.

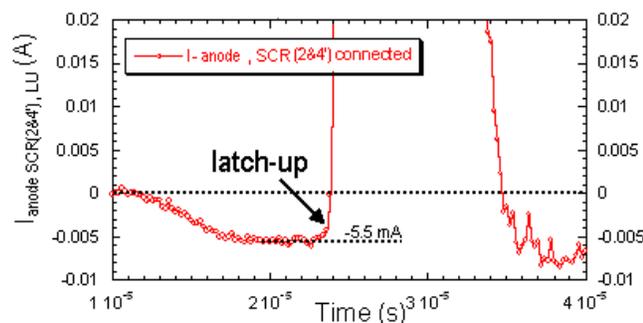


Figure 18: Anode current for parasitic SCR (2&4’) for setup 3.

Figure 18 also shows that the anode current reverses polarity at the moment SCR (2&4’) latches. From this study and previous research it appears that a critical level of current has to be injected by the vertical PNP into the substrate and the base of the NPN (2), corresponding to the base current for bipolar NPN action, before the SCR latches [1]. Because the lateral PNP (4’’) drains away a part of the injected current, in order to trigger latch-up for setup 3, more current will need to be injected into the emitter of the PNP injector than for the case where only parasitic SCR (2&4) is connected (setup 1). Because the collector versus emitter current ( $I_c$  vs.  $I_e$ ) curve has a typical sub-linear shape, due to saturation, the increase of injection current needed will be substantially higher than 5.5 mA (the collector current of the lateral PNP (4’’)). Due to this beneficial effect the latch-up trigger current is increased significantly. The second SCR (2&4’), which is also present, is not limited in current. Therefore, SCR (2&4’) latches as soon as NPN (2) starts bipolar operation. This is

a detrimental effect for latch-up, because SCR (2&4’) needs less substrate current to latch than SCR (2&4).

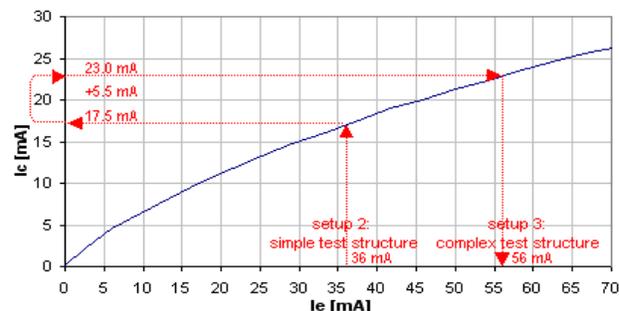


Figure 19: Current balance visualized on the  $I_c$ - $I_e$  curve of the vertical PNP for injection on the emitter of PNP (4), for the case SCR (2&4’) is connected (setup 3). When only SCR (2&4) is connected (setup 2), 36 mA of injection current triggers latch-up. When also SCR (2&4’) is connected (setup 3), the lateral PNP (4’’) between the two anodes of the two SCRs draws 5.5 mA of collector current, and the injection current needs to be increased to 56 mA in order to trigger latch-up, i.e. a ‘gain’ of 20 mA of injection current with regard to the case only parasitic SCR (2&4) is connected and stressed with a voltage source (setup 2).

## Conclusion

This paper presents a generic analysis methodology for characterizing parasitic bipolar and SCR elements in a HV CMOS technology for latch-up. Data of a  $\pm 20V$  HV-CMOS technology is used to demonstrate different measurement approaches for defining design rules for the standard current injection (‘I-test’) latch-up test. It is evident from the measurement results and discussion that the current source as described in the standard (JEITA/JEDEC) does not always represent the worst case stress condition. An improved analysis methodology based on solid state voltage pulse generators is provided. The paper also presents latch-up relevant test structures, containing the different parasitics, as found in a real I/O. Only results obtained from these ‘complex’ test structures will be relevant with regard to latch-up occurrence in a real product.

## Acknowledgements

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