Conference paper

Novel tool for accurate prediction of the ESD failure voltage of analog circuits

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Unlike HBM and MM, CDM robustness is highly dependent on IC layout and packaging. Therefore, IC companies mimic IC IO rings on IO-TEG test chips to select the most appropriate CDM protection concepts (correlation from IO-TEG to final IC's). This publication highlights pitfalls for this approach. Ensuring consistent substrate and Vss connections drastically improve the correlation.

Novel tool for accurate prediction of the ESD failure voltage of analog circuits

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Abstract – The application of state-of-the-art analog circuits in advanced technologies has led to an increase of unexpected ESD failures despite the use of robust ESD protection. It seems analog circuit designers need support to define the maximum tolerated voltage during ESD stress. This paper presents a novel tool to accurately calculate the ESD design window and to subsequently define an effective ESD protection approach.

Introduction

Thanks to a strong focus by the major foundries, analog design is now moving much faster to the most advanced technology nodes as compared to 5 years ago. The mixed analog-digital SoC's (system on chip) of today combine complex logic features with state-of-the art analog and high speed interfaces. While this trend has led to many innovative Consumer Electronics products it also did create a rise of unexpected ESD failures. This paper provides case studies where the standard ESD protection is not effective due to a much reduced maximum tolerated voltage (Figure 1) [1-4]. The second part describes a methodology to accurately calculate the ESD design window. The final section describes a tool – in progress – that supports analog designers to correctly define the ESD design window 'V_{max}' value and effective ESD protection.

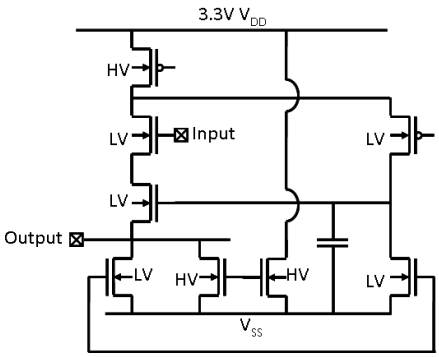

Figure 1: Schematic of a analog subcircuit in a high speed communication IC. Analog design engineers use different tricks to enhance the speed of the circuits such as applying core devices (1.2V) into the 3.3 V domain. This practice drastically reduces the maximum voltage between V_{DD} and V_{SS} during ESD stress events and leads to early degradation when a standard 3.3V power protection cell is used. Despite the use of robust ESD (4kV HBM) clamps the IC in this example failed at 1kV HBM for V_{DD} to V_{SS} stress.

I. Failure cause

Some analog/RF designers rely on core devices (1.2V) coupled between high voltage (3.3V) transistors inside a 3.3V domain (example in Figure 1). Standard reliability aspects during normal operation (maximum V_{gs},V_{ds}) may be covered by further circuit and process tricks such as the use of isolated Pwell to reduce the drain-bulk voltage. The core ESD failure voltage is however strongly reduced and the 3.3V protection concept (V_{t1}, V_{t2} based on 3.3V design window) is no longer effective for the reduced V_{max}.

Domain	Device	V_{max}	
1.2 V	FS NMOS	V_h	3.3 V
	FS PMOS	V_h	5.2 V
	GOX NMOS	$V_{ox,bd}$	5.2 V
	GOX PMOS	$V_{ox,bd}$	6.2 V
3.3 V	FS NMOS	V_h	4.6 V
	FS PMOS	V_h	7.0 V
	GOX NMOS	$V_{ox,bd}$	15.5 V
	GOX PMOS	$V_{ox,bd}$	17.3 V

Table 1: Vmax values for the different basic elements in the 130nm technology. For all the gate oxides, the maximum current 'I_{max}' is set to '0'. The behavior of IO transistors are also summarized. Depending on the circuit configuration the tool uses either the holding voltage or the failure voltage in the design window calculations.

II. ESD design methodology

To define the ESD design window 'V_{max}' (i.e. the maximum tolerated voltage during ESD), the voltage over the core circuit basic elements (MOS, diode, resistor,…) are measured (Table 1). From each of the measurements, summary parameters are determined: Maximum current level 'I_{max}' and the maximum voltage as a function of the stress current 'V_{max} = f(I)'. These values are inserted into the Design Window Calculation (DWC) tool.

III. Design tool

The algorithm described in Figure 3 is integrated into an ESD design tool [6] that circuit designers can use to define the correct ESD design window and subsequently select the most appropriate protection approach and clamping devices. The table in Figure 4 provides measurement results for an analog application IC in TSMC 130nm. All samples reach the 2kV HBM target performance.

Conclusions

Due to technology scaling and the recent increased use of complex sensitive analog interfaces, the accurately determination of the maximum voltage 'V_{max}' on the most sensitive nodes becomes ever more difficult. This work presents an interactive ESD design environment to cope with this complexity. The toolset provides immediate feedback on the weakest path and calculates the maximum allowed voltage on these nodes.

References

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[6] Keppens, B. et al, "Comprehensive tool for on-chip ESD protection design to achieve first-time-right success", accepted for presentation at D&R IPSOC 2008 conference

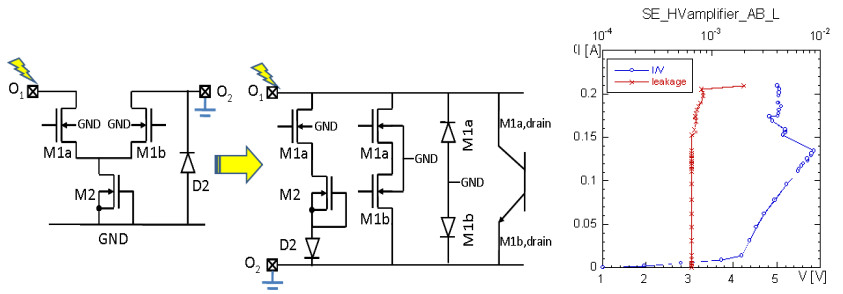


Figure 2: Case study of differential output circuit: Stress from output 1 to output 2 is translated into a parallel connection of different branches that are possible candidates for the ESD current. The branch with the least resistance needs to be identified by the calculation tool. The actual measurement shows a very low Vt2 maximum voltage of about 6V.

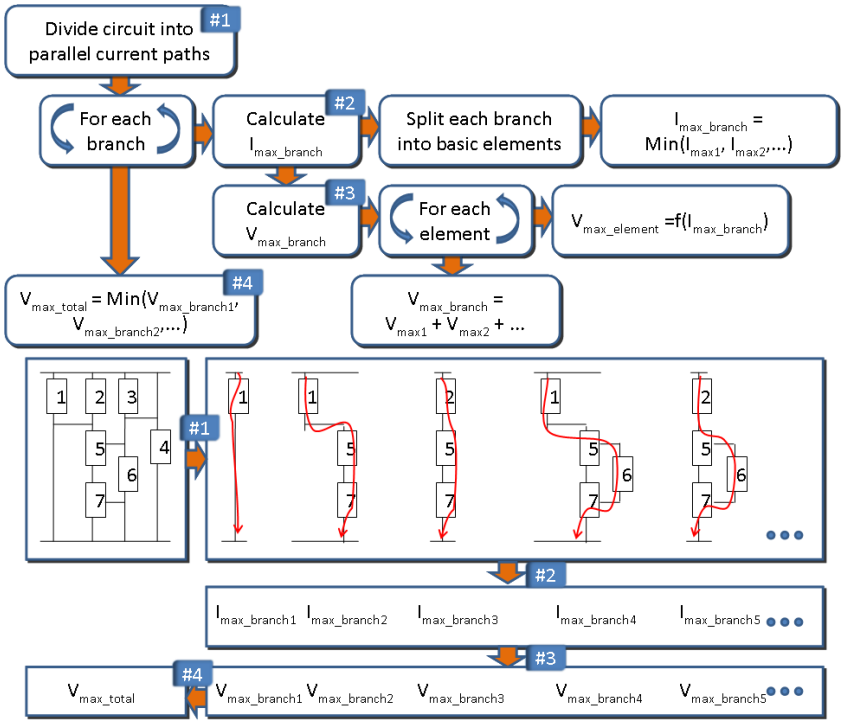
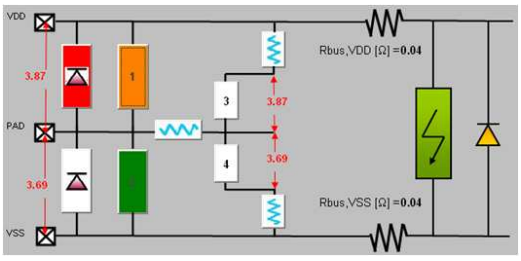


Figure 3: Graphical representation of the algorithm used to determine the maximum tolerated voltage for complex IO/Core circuits consisting of the combination of multiple branches, each with multiple basic elements (MOS, resistor, diode, oxide). To determine the maximum tolerated voltage per branch some heuristics are included in the software algorithm that depend on e.g. cascade configurations with shared bulk.



HBM Level	# samples	# Pass	# Fail
2kV	3	3	0
2.5kV	6	4	2
3kV	2	1	1
3.5kV	3	0	3

Figure 4: IO protection definition wizard where the IC designer can interactively calculate and optimize the ESD protection network for a specific IO. All of the elements in the GUI use the intuitive 'point, click, change' approach. The Green-Red colors depict robustness of the clamp devices. Table at the right side contain measurement results for the different stress combinations in the 130nm TSMC application. All samples reach the 2kV target specification.

About Sofics

ESD SOLUTIONS AT YOUR FINGERTIPS

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
    - Enable unique requirements for Latch-up, ESD, EOS
    - Layout, metallization and aspect ratio customization
    - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

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