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International Electrostatic Discharge Workshop 2010

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On-Chip ESD Protection with Improved High Holding Current SCR (HHISCR) Achieving IEC 8kV Contact System Level

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Abstract – For the design of on-chip ESD clamps against system level ESD stress three main challenges exist: reach a high failure current, ensure latch up immunity and limit transient overshoots. Bearing these in mind, high system level ESD requirements should be within reach. A novel improved high holding current SCR is introduced fulfilling all three requirements within drastically reduced silicon area.

I. Introduction

System level ESD robustness is important to ensure the reliability for any product. External (off-chip) ESD protection devices are widely used in the industry, but for some innovative consumer applications there is a trend induced by cost, form factor and operational performance to remove these board level devices and replace them by on-chip protection and thus connect I/O pins directly to the harsh outside world. The on-chip ESD clamp is scaled up to increase its failure currents which leads to many issues with traditional ESD solutions: increased pad leakage, increased load capacitance and especially larger die area. Therefore, IC designers request custom ESD protection structures with a high ESD performance but within a small silicon area while maintaining the desired IC specifications.

This paper presents a case study of a communication application where dedicated on-chip system level ESD protection is placed at the Rx and Tx pins. The transmitter operates in an open drain configuration.

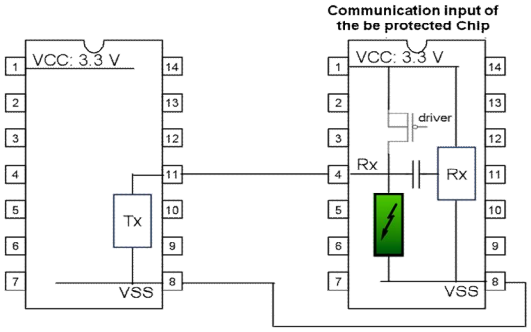

Figure 1: Schematic representation of the communication chip with local protection between the Rx-input and VSS.

II. High Holding Current SCR

Silicon Controlled Rectifiers (SCR's) are one of the many ESD protection strategies used in the industry. They combine a lot of advantages such as low leakage/capacitance, low clamping voltage and especially high current capability per area. This turns the SCR into an excellent device for high ESD current levels such as during system level ESD.

Besides high current levels, latch up immunity is the second requirement for system level protection. To improve the latch-up safety of SCRs, several techniques exist. One approach is the holding voltage engineering (adding holding diodes) to attain a holding voltage larger than the supply voltage [1],[4],[5]. Another approach is the high holding current (HHISCR), presented by Mergens [1],[2]. The basic idea is to increase the trigger/holding current above the JEDEC LU (e.g. 200mA) / normal specification (Figure 2) through external shunt resistors and a special SCR layout.

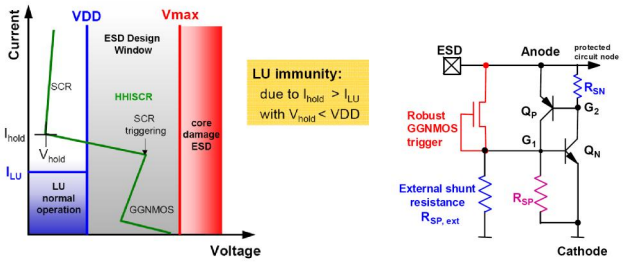

Figure 2: HHISCR as presented in [2].

The JEDEC latch-up test is only one aspect of the latch-up story: the ESD protection device *should not trigger* during this test. However, in the absence of off-chip ESD protection, the on-chip protection must trigger during the system-level test to protect the functional circuits. To prevent LU in that case, the condition changes so the device *must turn off* after the system level pulse has passed. While the first condition generally relates to the trigger current of the HHISCR, the second is mainly governed by its holding current.

To determine the relevant holding current and voltage of a stand-alone ESD clamp, an ESD stress pulse is super imposed on a DC bias level. When the DC bias level is step wise decreased in subsequent measurements the exact holding voltage and current can easily be determined in the relevant time domain.

In the application example of Figure 1, the PMOS line driver (maximum drive current 15mA) cannot source the current for maintaining the latch situation. For the system level ESD protection under test (HHISCR), the measurements show an effective holding current above 22mA at a holding voltage of 2.45V. The SCR will turn off after the ESD pulse has disappeared because the PMOS cannot deliver the required holding current of 22mA at a low drain-source voltage. This holding current can be tuned to the desired value by the resistors R_{SN} and R_{SP} and by the layout of the SCR body.

Combining the **high failure current** and the demonstrated **latch-up immunity**, the HHISCR is a viable option for IO protection in this application. The two remaining constraints

are related to area consumption and transient overshoot. The next section presents an improved HHISCR device with an area reduction of 22% and faster SCR turn-on.

III. Integrated Trigger Approach

The standard HHISCR uses FS poly resistors or metal resistors (1-10 Ohm) and an NMOS based trigger device. Instead of FS poly resistors, active resistors (N+/PWell) can be used. By applying a proper layout implementation, an NPN bipolar transistor is formed between the R_{SN} (Resistor between anode and G2) and R_{SP} (Resistor between G1 and cathode). This NPN bipolar acts as a trigger element replacing the NPN bipolar of the NMOS trigger device. The bipolar is evenly distributed across the resistors as shown in Figure 3 (b,c) for simplicity drawn as 3 separate devices. The upper NPN bipolar is formed between anode and G1, the lower NPN bipolar between G2 and GND and another NPN bipolar is formed somewhere in between. Note that each part of the NPN always sees the same resistance (R_{SN}, R_{SP} or a combination of these) given both resistors are of the same value.

The advantage of this distributed technique is that the SCR is not triggered in only one of the two trigger taps (G1, G2), but simultaneously in both trigger taps improving the turn-on speed and reducing the overshoot of the HHISCR. The basic device operation is as follows:

1. Avalanching starts at the anode of the resistor R_{SN} and turns on the NPN between G2 and GND
2. The conduction spreads upwards to the middle bipolar
3. Finally the current is distributed through the total NPN.

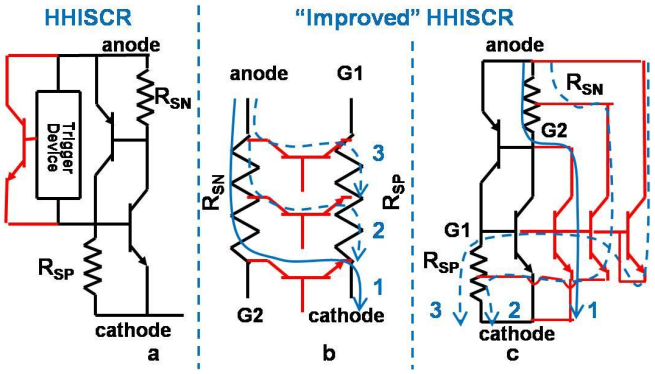

Figure 3: a) the standard HHISCR with only injection in G1 trigger tap (NMOS trigger device) b) the NPN is formed distributed over the 2 resistors (R_{SN}, R_{SP}) c) the NPN shown in b injects trigger current in G1 and G2 trigger tap.

IV. Measurement results

Figure 4 compares TLP measurements of the standard and the improved HHISCR devices (100ns pulse width, 10ns rise time) showing a similar clamping behaviour with a small difference in the trigger voltage (Vt1) which is related to the different type of trigger bipolar that is formed. Both devices remain within the design window of the I/O pins. Techniques to lower the trigger voltage (NPN engineering) are under investigation. A slightly higher failure current for the proposed device is observed due to an increased failure voltage of the trigger bipolar compared to the NMOS based trigger device.

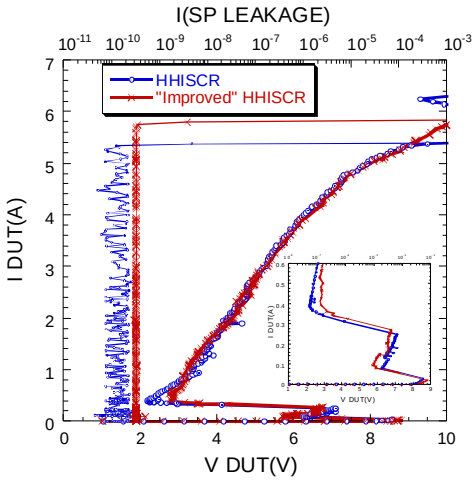

Figure 4: TLP extracted IV curves.

The improved HHISCR has a similar performance compared to the standard version but the required area has decreased 22%. This saving is due to the integration of the trigger device in the optimized layout of the resistors. (Figure 5)

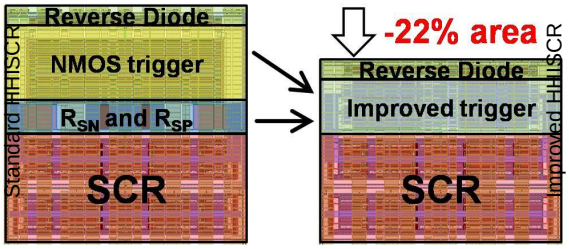

Figure 5: Top view of the ESD layout.

The proposed clamp was successfully implemented in a 0.13um technology (3.3 V domain) and in a 0.35 um CMOS technology (3.3 V domain). The HBM level of the clamp exceeds the 8kV limit of the tester in line with the expectations based on SCR size. System level tests (IEC 61000-4-2) on product level, under powered conditions and without any additional protection components at the connector pin passed 8kV contact and 15 kV air discharge. On-chip protection against 8kV HBM was enough for this application since not all the current flows through the IO. A proper shield/ground implementation already discharges a part of the ESD current.[6]

Conclusion

High current levels and latch up safety are the key aspects for a successful system level implementation. This paper showed that optimized layout of the HHISCR can reduce the needed area to reach system level ESD requirements by integrating the trigger device into the resistor layout.

References

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[6] M. Rosseeuw, “On-Chip ESD Protection Achieving 8kV HBM Without Compromising the 3.4Gbps HDMI Interface”, RCJ 2009

About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

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Version

May 2011

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