Conference paper

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Taiwan ESD and Reliability Conference 2010

Nowadays, mobile consumer electronics devices integrate various wireless interfaces like WIFI, Bluetooth, GPRS and GPS. Various approaches exist to protect the wireless interfaces against ESD stress. In recent years, researchers have focused on so-called 'co-design' techniques to solve both functional and protection constraints together which requires both RF and ESD design skills. However many IC designers still prefer to work with 'plug-n-play' protection concepts where the ESD clamps exhibit low parasitic capacitance, low series resistance and low leakage. This paper presents measurement results of 3 different SCR based protection approaches that exhibit high Q-factor and low and stable parasitic capacitance over a broad voltage and frequency range. The clamps are used for protection of LNA circuits in 90nm and 40nm Low Power (LP) CMOS technologies.

# SCR based on-chip ESD protection for LNA's in 90nm and 40nm CMOS

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***Abstract* – Nowadays, mobile consumer electronics devices integrate various wireless interfaces like WIFI, Bluetooth, GPRS and GPS. Various approaches exist to protect the wireless interfaces against ESD stress. In recent years, researchers have focused on so-called 'co-design' techniques to solve both functional and protection constraints together which requires both RF and ESD design skills. However many IC designers still prefer to work with 'plug-n-play' protection concepts where the ESD clamps exhibit low parasitic capacitance, low series resistance and low leakage. This paper presents measurement results of 3 different SCR based protection approaches that exhibit high Q-factor and low and stable parasitic capacitance over a broad voltage and frequency range. The clamps are used for protection of LNA circuits in 90nm and 40nm Low Power (LP) CMOS technologies.**

## INTRODUCTION

The number of wireless enabled systems is very diverse and steadily growing. System makers include wireless functions into mature applications like fixed-line telephones and TV's, increase the wireless features in mobile phones with support of multiple standards and come up with new device types that thrive on being always wirelessly connected for the newest content [1]. Further, also the transport, security, medical and payment sectors are quickly switching to wireless interfaces for improved user experience. Intelligent wireless bus, subway and train tickets replace the paper versions. Expensive equipment or resources in general are traced back thanks to RFID tags. Sensor networks reduce the cost of medical care while they increase the reaction speed when needed. Near Field Communication 'NFC' bank cards replace the smartcard and magnetic strips now commonly used.

Wireless communication comes in many forms, each designed or optimized for a specific task and application and sometimes constrained by local legislations differences [2]. Moreover existing standards are typically upgraded a few years down the road to enable higher data throughput or to extend the range [3]. Wireless standards can be grouped or compared based on different parameters like center frequency, primary use, encoding protocol, degree of mobility or range for instance. A rather complete overview of industry standards and proprietary formats can be found online [4].

Despite the improved ESD awareness and control in assembly factories and the related push for a reduction of component level ESD performance [5, 6] IC's still need adequate ESD protection. In many cases, traditional ESD protection devices used for low speed digital interfaces offered by foundries, IO library providers are not suited for the RF interfaces for a number of reasons:

- Capacitive loading shunts large part of the RF signal to Vdd/Vss lines due to high parasitic junction and metal capacitance of ESD clamps.
- Increased noise injected at the receiver due to series resistance used between primary and secondary ESD clamps
- DC leakage current degrades Q-factor and influences the size of the bias circuits

To reduce the cost of consumer electronics devices designers also try to combine different standards into a single silicon die [3] adding more constraints for the ESD protection approaches: the clamp parasitic influence should be as stable as possible across a large frequency band and voltage range.

This publication first (section I) briefly summarizes existing approaches for ESD protection of RF interfaces like plug-n-play, co-design and cancellation techniques. Section II describes a plug-n-play SCR clamp validated for an 8.5 GHz LNA designed in TSMC 90nm LP. Section III describes 2 different SCR based protection devices validated in TSMC 40nm LP CMOS to be used in a plug-n-play configuration. The most appropriate clamp is selected based on TLP, HBM, RF / S-parameter and DC leakage measurements at 3 temperatures.

In this publication we focus on Bluetooth, GPS and the IEEE 802.15.4a standard used for Real Time Location Systems (RTLS) [7] but the ESD devices can be used more broadly thanks to the low parasitic capacitance, high Q factor and low leakage.

## I. ESD APPROACHES FOR WIRELESS INTERFACES

IC designers use a variety of ESD protection approaches to protect the integrated circuits against ESD stress. The well known 'dual diode' based ESD protection has been used by many designers for the protection of analog circuits thanks to the small area, straightforward implementation, low leakage and low capacitive loading. Recently however various researches have predicted the end of 'dual diode based ESD design' for RF circuits in advanced CMOS (65nm and beyond) due to the shrinking ESD design window of the sensitive circuits [8-13]. They reason that to ensure effective protection the diodes connected to the IO's must be designed with larger perimeter to reduce the voltage drop ($R_{on}$ x $I_{ESD}$) which in turn leads to higher leakage and higher capacitive loading worsening the RF performance of the connected circuits.

Fortunately there are alternatives to protect RF circuits against ESD stress. This section very briefly outlines different protection approaches [11, 14] and provides relevant references:

(1) Plug-n-play, minimal parasitic capacitive loading
The parasitic capacitance of the ESD devices is minimized such that the degradation of the RF performance is limited. Researchers have compared different device types for this purpose [15-17]. Besides the active ESD devices people have used low frequency filters for high frequency applications (>5GHz) [18-21]

(2) 'LC' Cancellation techniques
In various publications designers compensated the parasitic effects of ESD devices by adding tuned LC elements [10, 13, 22]

(3) Co-design
Through the use of 'co-design' traditional ESD solutions with high capacitive loading can still be used because the negative effects are compensated for in the matching circuits [23, 24].

The following sections provide case studies based on one specific protection approach: plug-n-play protection with low capacitive SCR based protection.

## II. ESD FOR 8.5GHZ LNA IN 90NM LP

An SCR based protection clamp is validated for an 8.5 GHz LNA designed in TSMC 90nm LP. The ESD protection is designed to protect the ultra-wideband RF circuits based on the IEEE 802.15.4a standard [7]. 802.15.4a is an alternate PHY and adds location awareness, low power and higher data rates to the PHY and MAC specification for Zigbee devices. The circuit can be used for accurate real-time indoor location of resources/assets and in wireless sensors for health, retail, manufacturing and security sectors. One of the key requirements is the low leakage core and IO circuits: The chip operates off a single watch battery for up to 10 years.

The proprietary circuit to be protected consists of 3.3V transistors leading to a failure voltage (ESD design window) of 11.4V enabling various ESD protection concepts. To leave room for a large analog circuit including coils on the top metal, the IO ring is designed such that there is only a low resistive Vss bus available at the RF interfaces which means that a 'dual diode' protection approach is not feasible. To enable the high frequency signals the parasitic junction capacitance of ESD clamps has to be below 100fF. Furthermore the clamp leakage at room temperature must be below 1nA.

The selected protection design consists of an SCR clamp triggered by a NMOS device [25, 27] with dynamic gate bias as shown in figure 1 (top). The layout (figure 1 bottom) includes the SCR clamp, NMOS trigger, RC ESD detection filter, reverse diode and all required guard bands within an area of 55.91um by 52.08um. Thanks to this small area the ESD cell could be located under the bond pad (Circuit under Pad - CUP) leaving room for the large area inductors of the RF circuit. Besides the IO pad and a low resistive metal connection to Vss, a narrow connection to Vdd is required to keep the capacitance of the RC detection circuit charged up during functional operation of the circuit and to keep the diode from pad to anode reverse biased.

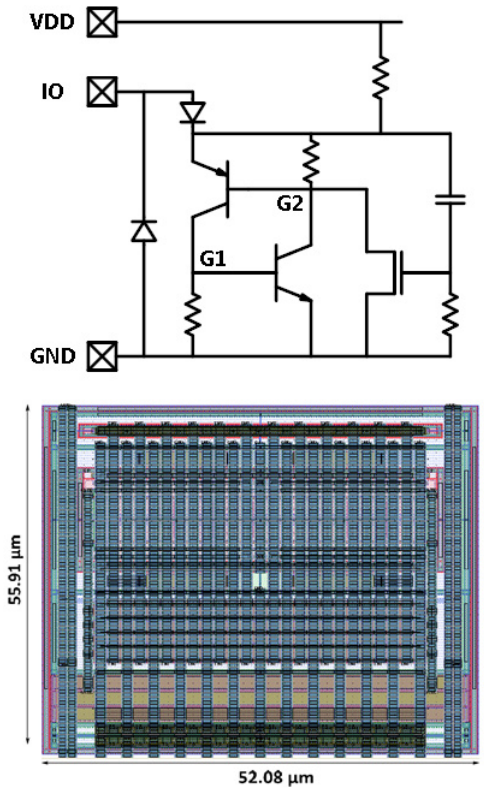



*Figure 1: Schematic and layout view of the MOS triggered SCR protection clamp. The total silicon footprint is less than 3000um² and could easily fit under the bond pad.*

The parasitic capacitance loading of the ESD clamp is calculated based on available models from the foundry following the equivalent circuit consisting of 9 junction capacitances and 7 metal capacitance values (figure 2). Total IO capacitance is less than 100fF.

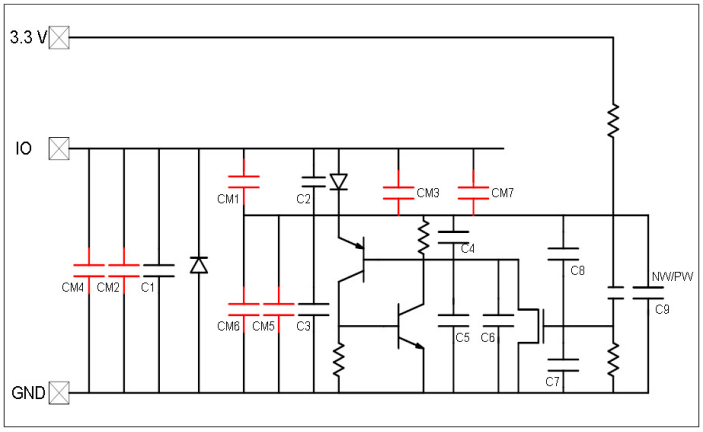



*Figure 2: Equivalent circuit for the calculation of parasitic junction and metal capacitance. Total capacitance at the IO's is 98.62fF.*

The ESD design guarantees effective ESD protection up to 2kV HBM, well above the standard requirement used for RF interfaces in advanced CMOS technology. This means that the chip can be handled in low cost assembly houses to push down the cost of the system.

Thanks to the low capacitive loading of 98.62fF and low leakage below 0.1 nA (@ 25°C), 55nA (@ 125°C) the clamp does not influence the RF behavior thereby greatly simplifying the design of the RF circuits. RF data will be available at the presentation of the publication.

## III. SCR BASED RF PROTECTION IN 40NM LP

This section outlines various SCR based approaches for ESD protection of wireless interfaces in a 40nm Low Power CMOS technology. First the different device types and measurement setups are described followed by the measurement results. Finally the most appropriate ESD protection device is selected based on the TLP, HBM, RF / S-parameter and DC leakage measurements.

### III.A. DEVICE TYPES

Two different SCR based protection clamps are compared for 1.1 (1.2V overdrive) RF interfaces. The variation between the clamps is mainly related to the trigger concept. Figure 3 provides an overview of the two clamp devices including a top view of the layout.

- The ESD-on-SCR is triggered as soon as the IO level raises 1 diode drop (Anode-G2) above the Vdd voltage [26].
- The DTSCR is turned on once the Anode-G2 and 3 trigger diodes are forward biased [27, 28].

Besides these two main types some other variations were combined on an RF TEG test chip to validate SCR based protection for LNA circuits.

All SCR clamps are designed for 2kV HBM and 200V MM which corresponds to more than 2A of TLP current in the TSMC 40nm process technology. The SCR perimeter of 2x47um is the same for all devices. All use 4 layers of metal leaving all other layers for bus routing. To limit noise coupling all devices described here use the deep Nwell layer.

Each clamp type is connected to Ground-Signal-Ground pads to obtain accurate capacitance and Q-factor values. De-embedding structures (short, open) are available too (Figure 4).

ESD devices are available as stand-alone clamps (for accurate leakage tests) and with 2 different monitor structures to characterize the effectiveness of the ESD protection: (1) The 'GOX' monitor [25] is a minimum size, fully silicided thin oxide transistor with gate connected to the IO pad. (2) The 'RC-MOS' monitor is a minimum size, fully silicided thin oxide transistor where drain is connected to pad, source to ground and gate is biased at 1/3 of the drain voltage through an RC-filter scheme.

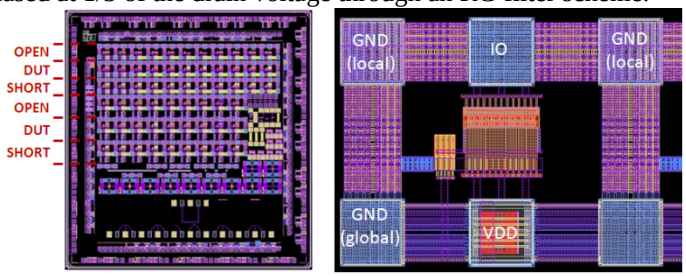
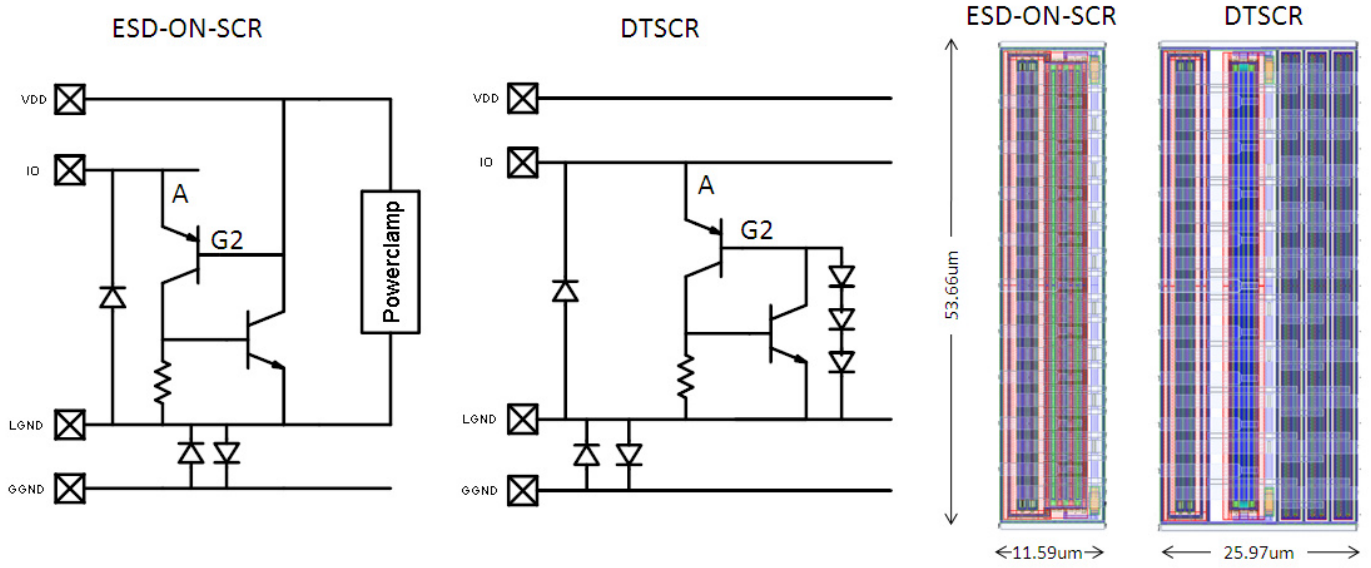



*Figure 4: 40nm RF test chip overview (left) and GSG layout example for a single clamp cell (right). The S-parameters are de-embedded to the edge of the ESD-clamps. An individual OPEN and SHORT structure is provided for each clamp.*




| Device | Leakage @ 1.32V | | | Parasitic capacitance | | | Q-factor | Area [um²] | ESD performance | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 25°C [A] | 85°C [A] | 125°C [A] | Total [fF] | To VSS [fF] | To VDD [fF] | | | HBM [kV] | MM [V] | TLP [A] |
| ESD-on-SCR | 7.46p | 12.7p | 18.5p | 177 | 116 | 61 | 71 | 622 | 5.2 | 300 | 2.51 |
| DTSCR | 85.3p | 13.2n | 174n | 178 | 170 | 8 | 43 | 1286 | 4.5 | 240 | 2.59 |

*Figure 3: Overview of the 2 SCR based ESD clamps used in this work. The schematics are depicted on the top, left. The ESD-on-SCR is triggered as soon as the IO level raises 1 diode drop (Anode-G2) above the Vdd voltage. The DTSCR is turned on once the Anode-G2 and trigger diodes are forward biased. Layout comparison of the clamps is shown top, right: Due to the trigger diodes, the DTSCR clamp (1286um²) is twice the size as the ESD-on-SCR clamp (622um²). While the trigger condition of the ESD-on-SCR is partly determined by power clamp device the silicon area of the power clamp is not included in this area comparison because the power clamp device is required anyway. Measurement results are summarized in the table.*

### III.B. Measurement setups and results

The different SCR clamps and monitor structures are measured with Transmission Line Pulse (TLP), HBM, MM, DC leakage and S-parameter systems.

The TLP data is performed with a Barth Electronics (10ns rise time, 100ns pulse width). For all devices positive stress is applied to the IO pad while the local ground (LGND) is grounded. During TLP stress relay S1 is open (Figure 5) but in order to obtain accurate leakage current results the substrate needs to be grounded through the global ground pad (GGND) by closing relay S1 during the leakage test. For some devices, a diode is present from IO to VDD. This results in an additional leakage path through the diode from IO to VDD and through the power clamp to LGND/GGND. The leakage current for these configurations is still low enough to detect failure if the VDD pad is left floating. Therefore the VDD pad is not powered during the leakage test. The maximum current level '$I_{max}$' is defined as $I_{t2}$ failure current minus a 20% safety margin.

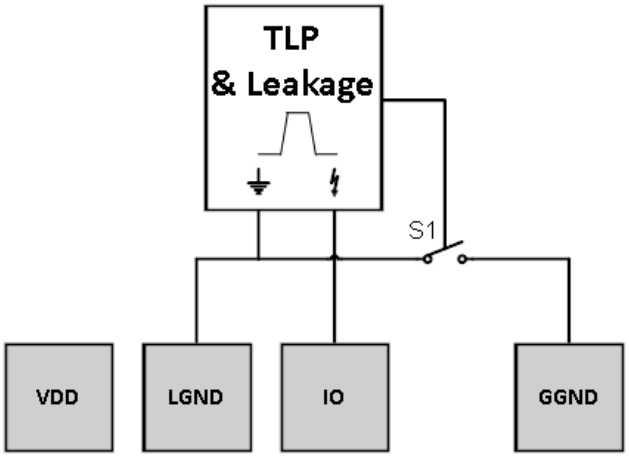



*Figure 5: TLP measurement setup: During TLP pulsing between IO and ground the global ground 'GGND' is not connected. For leakage measurements in between 'zaps' the global ground (and complete substrate) is connected together with the local ground 'LGND'. Vdd remains floating during the TLP/leakage tests.*

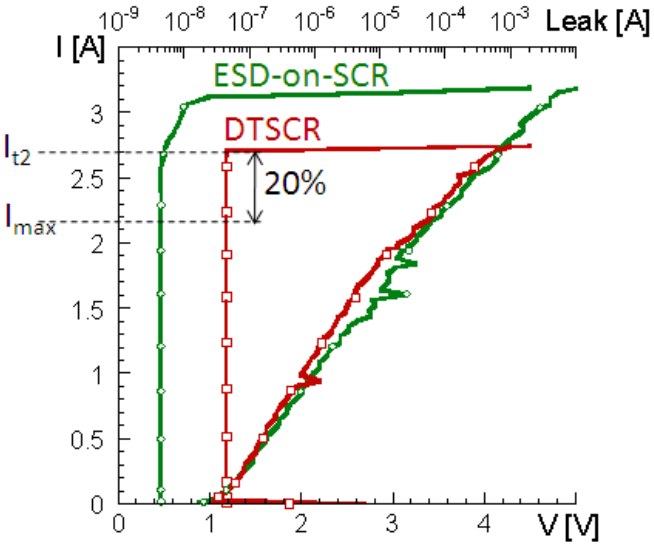



*Figure 6: TLP IV curves for the 2 device types: The clamping behavior is identical. For the ESD-on-SCR the Vdd pad is biased at 1.1V during the leakage measurement.*

Figure 6 and 7 plot the TLP IV curves of the 2 devices. The clamping device (SCR) is the same in the 2 device types also evident from the figures: the clamping behavior is exactly the same. The failure current $I_{t2}$ is more than 2.5A. After subtracting a safety margin of about 20% to cover process variations the maximum current level ('$I_{max}$') is more than 2A for all devices. As expected, the triggering of the ESD-on-SCR is strongly different compared to the DTSCR and makes it more effective for protection of sensitive circuits.

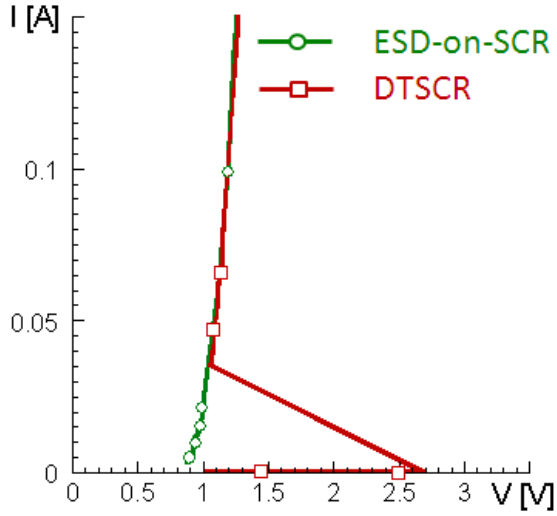



*Figure 7: Zoom-in on the TLP IV curves for the 2 device types: The trigger voltage of the ESD-on-SCR is much lower than the DTSCR.*

Besides standard TLP tests each clamp is also stressed with multiple pulses according to the same test setup. At least 1000 TLP pulses are applied with current amplitude fixed to the maximum current level '$I_{max}$' [25, 29]. The leakage current is measured after each set of 100 pulses. Failure is defined as any significant or systematic deviation from the pre-stress leakage current. All devices passed this test condition without leakage increase.

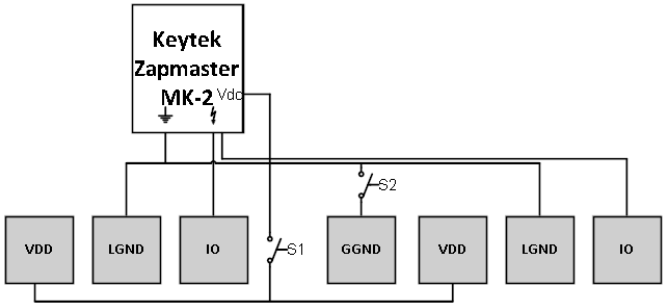



*Figure 8: Measurement setup for HBM/MM measurements. VDD and GGND are only connected during the curve trace phase by closing switch S1 and S2*

HBM, MM measurements are applied to the IO pin with all LGND pins grounded and with VDD and GGND floating. The DC sweep between zaps is performed while both GND and LGND pads are grounded and 1.32V bias is applied to the VDD pad. Figure 8 illustrates the measurement setup used for the HBM and MM tests. Minimum pass level for HBM and MM measurements is given in the table in figure 3, based on data of 6 samples (3 with 'GOX' monitor and 3 with 'RC-MOS' monitor).

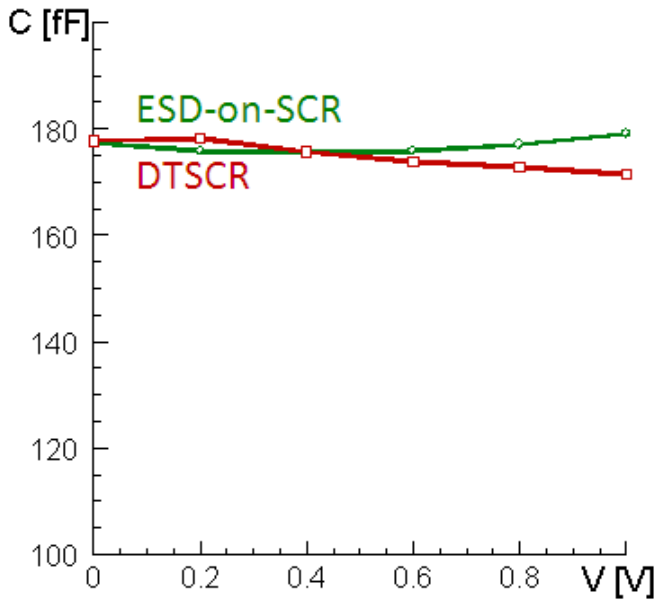



*Figure 10: S-parameter analysis at 5GHz- average of 4 dies. Influence of the total IO capacitance versus IO voltage: Both devices show a rather small variation in parasitic capacitance.*

During DC leakage measurements both global and local ground pads are connected and grounded. The supply pad (VDD) is biased at 1.32V DC. The voltage at the IO pad is swept linearly from 0V to 1.32V. The measurements are performed on devices without a monitor device to accurately measure the clamp leakage. The measurements are performed on die, in the dark and at three temperatures: room temperature (25°C), 85°C and 120°C. Figure 9 summarizes the data for the two device types. The measurements on the ESD-on-SCR show that the intrinsic leakage of the SCR device is very low even in 40nm CMOS (~10pA). The leakage of the DTSCR is determined by the trigger element: the leakage stays below 100pA when a diode chain is used to trigger the SCR. The leakage current has a strong relation to the Q-factor of the ESD clamps: The table in figure 3 shows that the Q-factor of the ESD-on-SCR (lowest leakage) is 1.5 times higher than that of the DTSCR where the leakage is 10 times higher.

Finally, the different clamps were measured with RF S-parameter equipment. After de-embedding based on 'open' and 'short' structures, the device parasitic capacitance (junction and metal combined) is determined as a function of IO bias voltage (between 0 and 1V) and frequency (between 1 and 20 GHz). Both plots (Figures 10 and 11) show that the capacitance level variation is less than 6%.

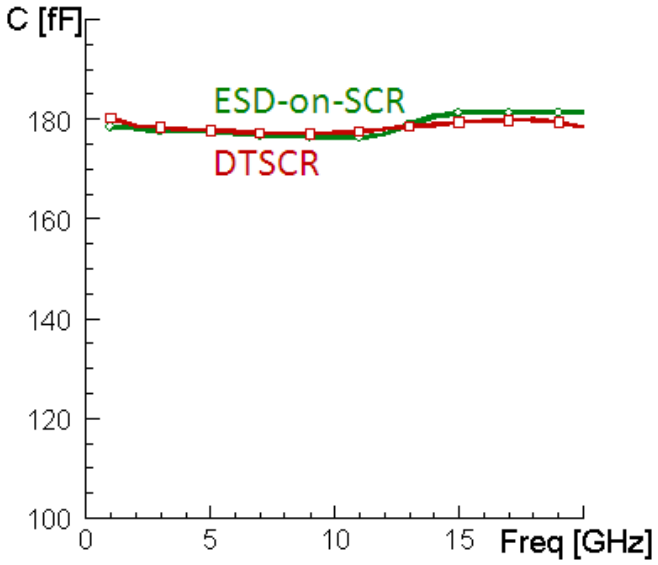



*Figure 11: S-parameter analysis at 0V IO bias, average of 4 dies: Influence of the total IO capacitance versus signal frequency: Both device types have a small variation in capacitance value.*

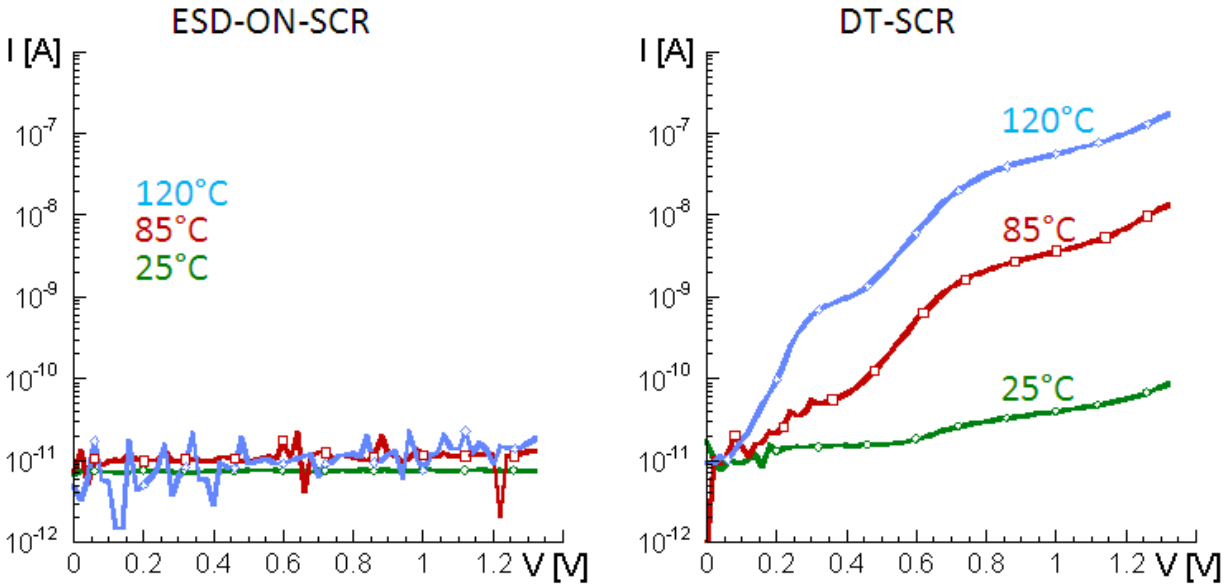



*Figure 9: Comparison of the DC leakage measurements at three temperatures (25℃, 85℃ and 120℃) betwe en the two SCR types in this study. To measure the clamp related leakage individually all test structures were measured without monitor devices. The basic SCR in 40nm has an extremely low leakage (~10pA) that is very stable across temperature. This is visible in the leakage measurements on the ESD-on-SCR device (Vdd is biased at 1.2V). The leakage current for DTSCR is determined by the trigger element. The leakage difference can be used to select the clamp with the highest Q-factor: The ESD-on-SCR has the lowest leakage and the highest Q-factor.*

Besides the standard devices described above additional variations are included on the test chip including capacitance reduction circuits, SCR anode/cathode layout variations and versions without deep Nwell. A summary of the ESD, Q-factor and capacitance values is given in figure 12.

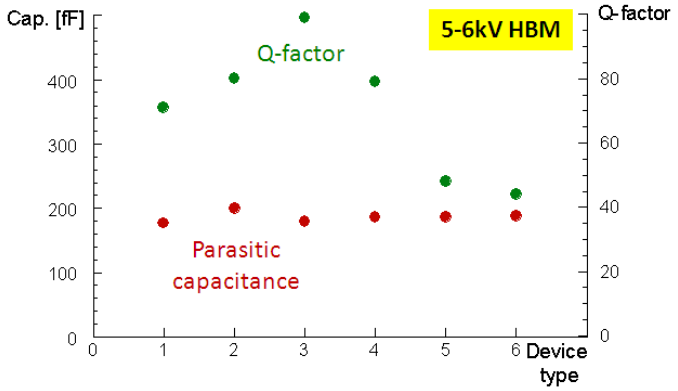



*Figure 12: Various layout variations were available on the RF test chip. High ESD performance combined with low leakage, high Q-factor and low parasitic capacitance loading can be easily achieved in 40nm.*

### III.C. Selection of the most appropriate ESD clamp

Based on the different measurements the recommended protection solution for LNA circuits in 40nm is the ESD-on-SCR. While the parasitic capacitance is similar between DTSCR and ESD-on-SCR devices, the latter has much lower leakage current, higher Q-factor and a much smaller silicon footprint. The ESD data shows that the ESD-on-SCR provides an effective protection of more than 300V MM and 5.2kV HBM. However, in many cases the required protection level is only 2kV HBM. Thanks to the simple layout style and straightforward metallization concept the ESD-on-SCR can be easily scaled down to lower the ESD performance leading to further reduced leakage (below 10pA), capacitance (~100fF) and silicon area (~500um$^2$).

Important to note is that the ESD-on-SCR is triggered into low voltage clamping mode as soon as the IO voltage raises 0.7V above the Vdd potential (1.2V). For the LNA circuits described here this is not a concern: The applied signal has no DC component. Also, the bias circuit has a high output resistance and the bias level is somewhere between 0.3V and 0.5V much lower than the SCR holding voltage. Moreover, the input signal from the antenna has a low amplitude which means that the trigger condition for the ESD-on-SCR is never fulfilled. For the protection of other applications in advanced CMOS the SCR can easily be tweaked to solve most latch-up constraints including transient latch-up situations during system level stress [30, 31].

If the Vdd line is rather noisy it could couple to the RF IO pad. Therefore, some designers may prefer the DTSCR device type because it has much less parasitic capacitance between IO and Vdd.

## IV. Discussion

CDM is a major concern but because it can only be measured in final products we have confirmed the voltage response of the clamps with TLP pulses with fast rise time of 200ps.

## Conclusion

This publication provided information about SCR based ESD protection clamps for RF circuits validated in TSMC 90nm and TSMC 40nm LP CMOS technologies. In both technologies the ESD protection clamps described have excellent figures of merit: Due to the low parasitic capacitance, low leakage and high Q-factor the influence on the RF performance is limited. RF designers can rely on these SCR device types without the need for extensive co-design optimizations between RF (matching) circuitry and ESD protection devices.

The paper provided measurement results on TSMC 40nm RF LNA's where the sensitive thin oxide circuit is effectively protected up to 5.2kV HBM while the leakage stays below 10pA and the parasitic capacitance is around 180fF over a broad range of frequency and voltage.

While this paper focused on Bluetooth, GPS and the IEEE 802.15.4a standard the ESD device concepts can be used more broadly for both high frequency RF IO's as well as high speed differential, digital interfaces like HDMI and USB 3.0.

## Note

As is the case with many published ESD design solutions, the techniques and protection solutions described in this paper are covered under patents and cannot be copied freely.

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# About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

# Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

# Notes



# Version

May 2011

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