Conference paper

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The Hebistor Device: Novel latch-up immune ESD Protection Clamp for High Voltage Interfaces

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***Abstract* – High voltage interfaces are broadly used in many IC applications like motor control, power management and conversion, LCD panel drivers and automotive systems. Because the high voltage IC's are typically used in severe applications IC designers need to protect their circuits to a steady growing list of requirements. In this paper we present an overview of the ESD, EOS and latch-up requirements and compare the performance of different on-chip ESD protection approaches. The paper introduces a newly developed protection device with a high holding voltage for absolute latch-up immunity.**

INTRODUCTION

A growing set of IC applications require a high voltage interface. Examples include power management, power conversion and automotive chips with interfaces typically between 12V and 100V. Also mobile devices like cell phones and personal navigation devices today include interfaces above 10V to e.g. control and sense MEMS gyroscopic or compass sensors. And, most LCD/OLED display technologies require driving voltages between 10 and 40V. Besides the power, MEMS and display interfaces many devices include some sort of motor like the optical zoom lens and shutter control of digital cameras or the 'silent mode' vibrator in cell phones.

Though these applications represent fast growth markets, the underlying silicon process technologies lack standardized high performance ESD solutions. Today, different protection clamp types are used in the industry, each with significant performance and cost burdens that prevent generic use. The main problems with traditional solutions are high leakage current, large silicon area consumption and extensive custom (trial and error) development cycles for each process/fab change.

Despite the efforts from the 'ESD council' [1,2] to reduce the component level ESD performance levels there is a opposite trend to push system related ESD/latch-up requirements down to the IC design level in order to reduce system failures and improve user safety [3-5]. This is mostly prevalent in automotive, industrial and consumer electronics markets. OEM makers request very robust and latch-up immune on-chip ESD protection devices. This paper introduces hebistor clamps that address these stated needs and requirements.

The paper first provides an overview of the currently used ESD protection solutions (Section I). In Section II the requirements for a generic high voltage ESD device are summarized. Section III introduces the innovative solution that meets all these requirements within a small silicon area and without the need for semiconductor process tuning. The main benefits are summarized in the Conclusion.

I. COMPARISON OF TRADITIONAL ESD APPROACHES

Today IC designers use a variety of ESD protection device types in HV-CMOS or BCD process nodes to protect the integrated circuits against ESD stress. Below a non-exhaustive overview highlights the main devices.

Clamp	Curve	Flexibility	Effective protection	ESD/Area	JEDEC Latch-up immunity	System level ESD	ESD/Leakage
Zener diode	A	I_{max}	☆	☆	☆☆☆☆☆	☆☆	☆
RC-MOS	B	I_{max}, V_{t1}	☆☆☆☆☆	☆	☆☆☆☆☆	☆☆	☆
PNP, PMOS	A	I_{max}	☆☆	☆☆	☆☆☆☆☆	☆☆	☆☆☆
NPN, NMOS	C		☆☆☆	☆☆☆	☆	☆	☆☆☆
BASIC SCR	D	I_{max}	☆☆☆	☆☆☆☆☆	☆	☆	☆☆☆☆☆
Sofics HHI-SCR	E	I_{max}, V_{t1}, I_{t1}	☆☆☆☆☆	☆☆☆☆☆	☆☆☆☆☆	☆☆	☆☆☆☆☆
Sofics Hebistor	F	I_{max}, V_{t1}, V_h	☆☆☆☆☆	☆☆☆☆	☆☆☆☆☆	☆☆☆☆☆	☆☆☆☆☆

Table1: The table summarizes the most relevant performance parameters for each device type: The higher the number of stars the better. The 'flexibility' parameter summarizes the behavior parameters that can be easily changed ('tuned') by changes in the device layout. The 'Effective protection' column depicts the ability to protect sensitive circuits. The 'ESD/area' and 'ESD/leakage' columns compare the ESD performance per area and per leakage. The 'System level ESD' represents immunity to high ESD stress as well as transient latch-up constraints, which is strongly different from latch-up tests according to JEDEC 78A.

I.A. Zener diodes

Zener based protection devices have been around for a long time. The characteristic behavior is depicted in Figure 1 (type 'a'). The breakdown and holding voltage are above the supply voltage level ensuring latch-up immune ESD protection. Zeners can be applied in many technology nodes though there are many drawbacks for ESD protection:

- The intrinsic ESD robustness level is rather low which leads to a large device size.
- The large device size means that the capacitance and leakage values are higher than any other device type when scaled to the same protection level.
- For many circuits the Zener device cannot provide effective protection due to a too high holding voltage. A change in the holding voltage is possible by dedicated process modifications (doping levels/profiles) with the risk of degrading core functional performance or by adding expensive processing steps and masks. Furthermore IC designers can create applications with different supply voltage levels within one process technology which requires different tuned Zener diodes.

I.B. RC-MOS (a.k.a. BIGFET)

The dynamically triggered MOS transistor is extensively used in low voltage technology nodes for many general purpose IO libraries [6, 7]. The characteristic behavior is depicted in Figure 1 (type 'b'). The MOS is biased such that all the ESD current is shunted in the active MOS conduction mode. The MOS device is turned off during normal operation. Many different configurations exist to tune the device behavior (timing, boosted bias, false trigger prevention) [8, 9]. However, in high voltage technologies the application of RC-MOS devices is less straight forward, typically leading to very large area consumption, even for a low ESD HBM protection level. However the main problem is the inability to protect the sensitive circuits against ESD stress occurring under biased conditions.

I.C. PMOS, PNP

The HV-PMOS device has a characteristic similar to the Zener device (Figure 1, type 'a'). Its ESD performance is very process dependent. In 'good' technology nodes the robustness level per micron device width is higher than the Zener device due to the bipolar PNP action. This results in a somewhat better performance for the leakage and silicon area consumption. Moreover, due to a lower breakdown and holding voltage the device is typically better suited to protect sensitive circuits.

I.D. NMOS, NPN

Designers use NMOS and NPN based approaches because the It2 robustness level is typically higher than the 3 previous device types leading to smaller silicon area and reduced leakage. However, degradation issues due to non-uniform triggering are a major problem and road block, as reported and documented by various sources [5, 10, 11]. In addition, the key issue is the latch-up weakness due to a low holding voltage, typically much below the supply voltage. This characteristic behavior is depicted in Figure 1 (type 'c').

I.E. SCR

Finally for some high voltage signal pins it is possible to rely on Silicon Controlled Rectifier (SCR) based protection devices [5, 12]. SCRs have superb ESD characteristics with low leakage and low capacitance but require careful high holding and trigger current control to avoid latch-up problems [13]. The characteristic behavior of the basic SCR device is depicted in Figure 1 (type 'd') while the latch-up improved high holding current (HHI) SCR approach is shown as type 'e' [10, 13-15].

Table 1 summarizes the different devices with advantages and disadvantages. The star rating is based on extensive benchmarking of high voltage technologies from various foundries and IDMs but it is not an absolute overview. Exceptions exist where e.g. processes are modified to enhance the ESD properties of certain devices [5]. Clearly within the existing device pool (A-E) there is no generic and no optimal solution. It basically comes down to a selection between a cost-effective design (NPN, SCR) with major latch-up immunity weakness or a guaranteed latch-up immune design that occupies a huge chip area (Zener diode, PMOS). A single, generic device that solves all the different aspects would greatly simplify IC design in HVCMOS and BCD process technology.

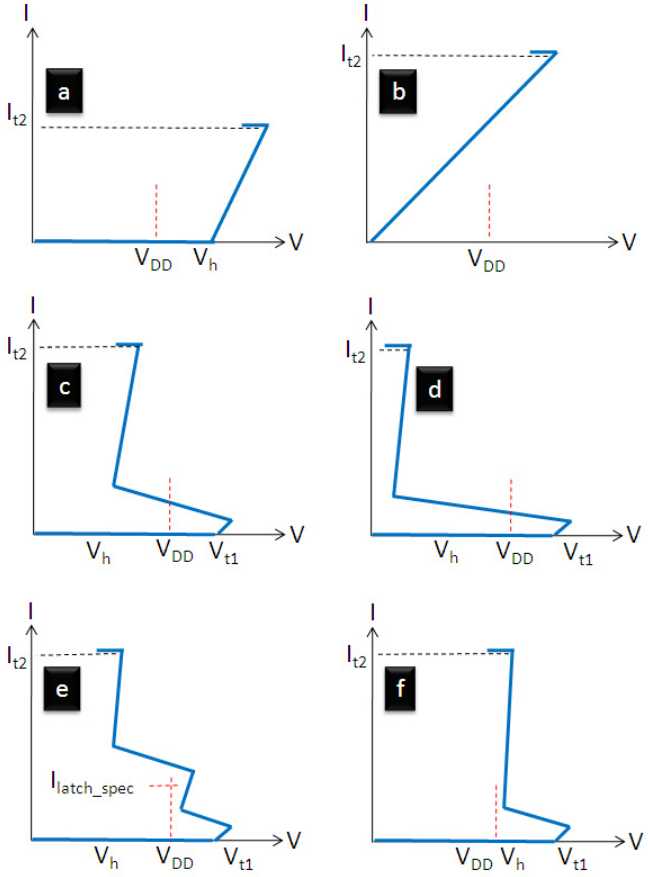

Figure 1: Simplified behavior of the main ESD solution types used for protection of high voltage interfaces: (a) Zener diode, (b) RC MOS, (c) NMOS or NPN device, (d) Basic SCR, (e) HHI-SCR, (f) Novel hebistor clamp.

II. Requirements for high voltage ESD clamps

This section outlines the broad set of requirements for on-chip ESD protection clamps. Foremost, the ESD clamp needs to protect the chip circuitry. This can be an entire power domain (supply pin protection) or a single input, output or IO circuit (IO pin protection). While different test like HBM, MM and CDM are used to quantify protection levels, Transmission Line Pulse ('TLP') testers are standard systems to characterize the ESD relevant performance parameters of the protection clamps.

Example TLP curves are depicted on Figure 2 (top) for a Zener diode, HV-PMOS, SCR device and a hebistor clamp device, all produced in a 0.35um 15V technology.

The Zener, HV-PMOS and hebistor clamps have a high enough holding voltage above VDD to ensure latch-up immune operation. The SCR holding voltage is well below Vdd which may result in latch-up problems.

The operation regime of the Zener is above the maximum allowed voltage ('Vmax') leading to destruction of the sensitive to-be-protected circuits, hence rendering the clamp ineffective. The PMOS device has an ineffective operation region above 0.8 Ampere which means that the clamp size has to be increased if more than 1kV HBM (with a minimum safety margin) is required. SCR and hebistor clamps provide effective protection.

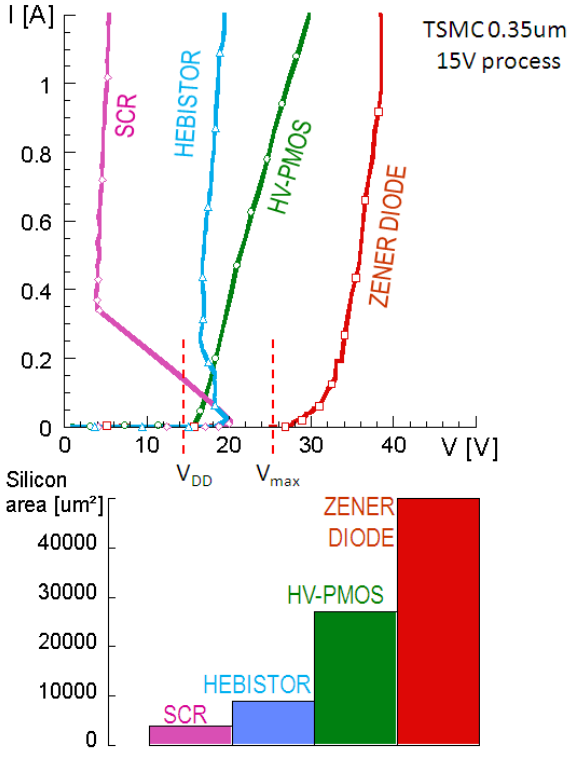

Figure 2: Transmission Line Pulse ('TLP') IV curves for 4 device types measured on 0.35um 15V CMOS technology: Zener diode, HV-PMOS, avalanche triggered SCR and the novel Hebistor. The bottom figure provides an overview of silicon footprint for the 4 device types designed to achieve 8kV HBM protection.

Figure 2 (bottom) also provides an overview of the silicon footprint for the 4 devices types scaled to an ESD protection level of 8kV HBM. Clearly, the SCR and hebistor clamp types are much smaller than the HV-PMOS and Zener based ESD protection approaches.

While ESD devices are routinely characterized with TLP to determine the optimal design, there are 3 main problems with TLP measurements that are relevant for this discussion:
(1) The TLP characteristic is based on averaged values of voltage and current versus time waveforms, hence the TLP curve hides relevant information about the time dependent behavior [16-18].
(2) The TLP pulse width is typically limited to 100ns; that is enough for ESD relevant analysis but it is not relevant for EOS (electrical overstress) which has a much longer timeframe.
(3) TLP measurements are performed on 2 pins, leaving other pins floating. No bias is applied at Vdd so latch-up issues cannot be investigated [19].
(4) Most TLP systems use 50 ohm characteristic impedance, not suited for analysis of HV snapback clamps [18, 20].

Therefore, in addition to standard TLP analysis, it is important for high voltage applications to look carefully into the full waveform information and to include longer pulse durations in the evaluation. This is evident from Figure 3: the voltage versus time waveform of the Basic HV SCR shows that the device has an operating regime well above Vdd for the first 100ns (TLP time domain – highlighted by the rectangle). However the operating voltage drastically decreases below the Vdd voltage for longer pulses. This means that latch-up issues may occur when this device is used as ESD protection clamp under transient latch-up situations like some EOS and IEC 61000-4-2 stress situations. To compare, the novel hebistor device (Figure 3, right side) exhibits the desired behavior under long stress pulses. The clamping voltage stays above the supply level.

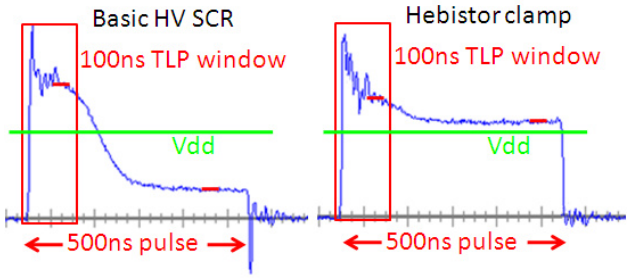

Figure 3: Voltage versus time waveform characterization of a basic high voltage SCR device (left side) and the novel hebistor clamp (right side) in 0.35um 15V CMOS. The voltage waveforms are measured with a TLP like setup with solid state pulse generators with a much longer pulse width (500ns instead of the TLP standard 100ns duration). Within the 100ns TLP window the measured holding voltage is high enough for both devices. However for the Basic SCR device, the voltage drops drastically below the supply level after 250ns… which can lead to latch-up. The hebistor device on the other hand shows a voltage level above the supply voltage for the entire pulse width which ensures latch-up immunity.

Other measurement approaches exist to verify the transient latch-up susceptibility. Professor Ker from Taiwan for instance tends to use a system depicted in figure 4 [21-23]. First a DC bias of Vdd (40V in the example) is applied to the device under test. Secondly a sharp pulse is superimposed on the DC level by connecting a charged capacitor to the biased device. Such test has many different names depending on actual conditions: Vlatch, Charged Capacitance Latch-up (CCL) [13], transient latch-up [24] or Machine Model under powered conditions. It can also be simulated with a multi-level TLP approach [25]. Due to this pulse, the ESD protection clamp will turn on to shunt the ESD current. If the clamp is latch-up immune the voltage returns to the initial DC bias level once the superimposed MM pulse is over. When performing such transient latch-up tests it is important to use a fast and low resistive power supply for the DC bias.

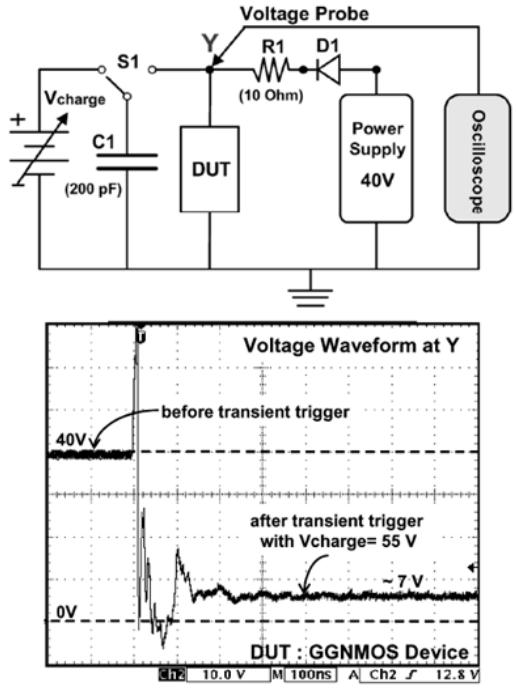

Figure 4: Transient latch-up setup (top) described by professor Ker [21-23]. A charged 200pF capacitor is discharged to a biased device under test. When such a pulse is imposed on a HV-NMOS device in a 40V technology (bottom) the latch-up problem is clearly visible.

When such a test is applied on a HV ggNMOS device the latch-up problem is clearly demonstrated (Figure 4 bottom). After the ESD pulse, the voltage quickly drops to a low value of about 7V and remains latched at that low value.

Finally, in real world applications end-user systems can receive multiple ESD stress pulses over the product lifetime. Certainly HV-NMOS based protection devices are prone to degradation issues. The example given below shows two TLP measurements of identical grounded gate HV NMOS snapback clamps in a 0.5um (43V) technology.

After snapback, at roughly 73V, a clear and steady degradation is visible in the leakage current [10]. Different TLP stress step levels are used to define the real failure current level. The data shows that the final failure current (device leakage in uA order of magnitude) is dependent on the pulse density. When a small stress step is applied, the failure current is much lower.

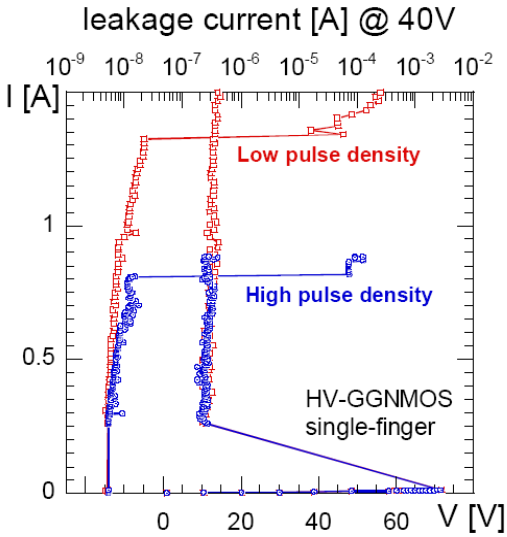

Figure 5: TLP curves on HV-NMOS devices in a 0.5um 43V process technology. The TLP stress is applied at 2 devices, once with large steps (low pulse density) and once with small steps (high pulse density). Due to the degradation effect the number of stress pulses strongly influences the failure current It2.

On-chip ESD protection for high voltage interfaces must fulfill many requirements. Current solutions cannot provide a low leakage, cost-effective and latch-up immune ESD protection clamp without degradation effects that is needed for the growing set of high voltage applications. The hebistor devices discussed in the next Section provide a possible solution.

III. Hebistor Clamps for ESD Protection

This section provides measurement results from the validation of the hebistor technology on TSMC 0.35um 15V and TSMC 0.25um BCD 40V technology platforms.

III.A. TSMC 0.35um 15V process

The TLP curve for the hebistor device in 0.35um 15V CMOS is compared to the Zener diode, SCR and HVPMOS clamps on Figure 2. The measurement with long pulse duration depicted on Figure 3 (right side) shows that the holding voltage remains above the supply voltage.

Further beyond-the-standard transient latch-up stress tests clearly show that the hebistor device is guaranteed latch-up free as shown on figure 6. Similar to the experiment outlined in figure 4 a Agilent 8110 pulse generator [26] is used to combine a DC bias level of 15V (pulse source 1) and a fast transient pulse of 5V (pulse source 2) to turn on the hebistor protection clamp. After the transient pulse is over the voltage is restored to 15V: no latch-up situation occurred.

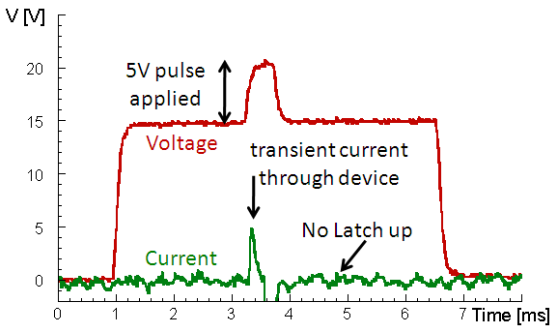

Figure 6: Voltage and current versus time for a 15V hebistor device in the 0.35um TSMC process. The device is biased at 15V prior to the transient stress pulse which turns on the hebistor. After the stress pulse the voltage returns to 15V showing no latch-up occurred.

III.B. TSMC 0.25UM 40V BCD

The TSMC 0.25um 40V BCD technology allows different voltage domains to be used on the single die like 12V, 24V, 40V. While the validation effort described further focused on 40V device concepts are proven for all these voltage domains as is evident from Figure 7.

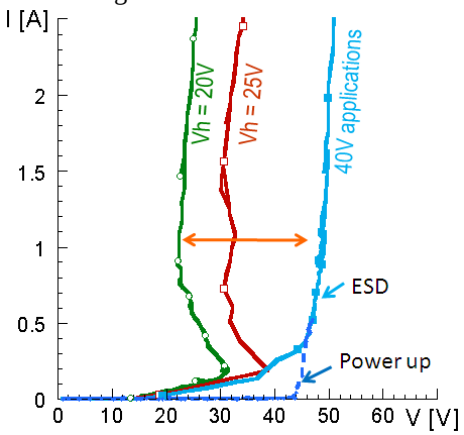

Figure 7: TLP IV curves of the hebistor clamp with different holding voltages in the 0.25um BCD technology. Holding voltage and transient trigger voltage for the 40V clamp are 44.5V. The Vt1 trigger voltage is well below the failure voltage defined by 1.3x Vdd. A transient trigger effect to reduce the trigger voltage under ESD conditions is visible. Under DC conditions the breakdown voltage is increased above 50V as is evident from figure 8.

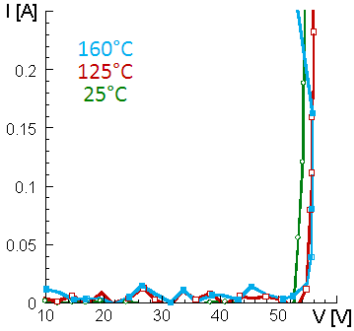

Figure 8: Under DC conditions the breakdown voltage is increased above 50V to ensure there is no problem with unwanted triggering of the device under normal operation.

The TLP IV measurements (Figure 7) of the hebistor clamp show a high holding voltage, high failure current of more than 2.5A and a very low on-resistance. Not shown on the figure is the low leakage of 50nA for the 40V clamp scaled for 4kV HBM/200V MM. The IV curve shows a transient trigger effect to reduce the trigger voltage under fast transient conditions such as ESD stress. Under DC conditions however the breakdown voltage is increased above 50V (Figure 8).

Besides TLP IV measurements extensive waveform analysis was performed (Figure 9) to investigate the holding voltage. Clearly the holding voltage does not drop below the supply voltage even under longer pulse durations.

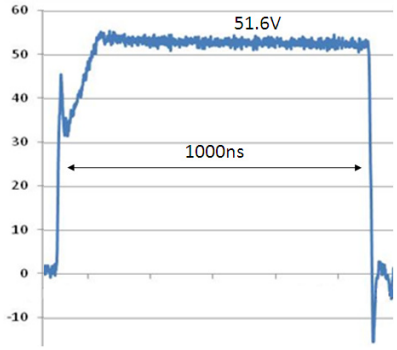

Figure 9: A voltage waveform for the 40V clamp shows that the holding voltage remains above 50V even for long pulses.

The hebistor device behavior was also checked with various transient latch-up approaches. One such test consisted of a 100ns TLP pulse of 1 ampere that is superimposed on a 50V DC bias level. Figure 10 shows the voltage and current waveforms captured during the test. At about 100ns from the start of the measurement, the biased (50V) device is stressed with a high amplitude (1A) TLP pulse. The current waveform shows the current flowing through the device. After the TLP pulse is over, the bias voltage restores at 50V while the current through the device is reduced to the level before the ESD stress (hebistor leakage current). The overshoot and undershoot are related to a combination of device response and test system parasitic inductance.

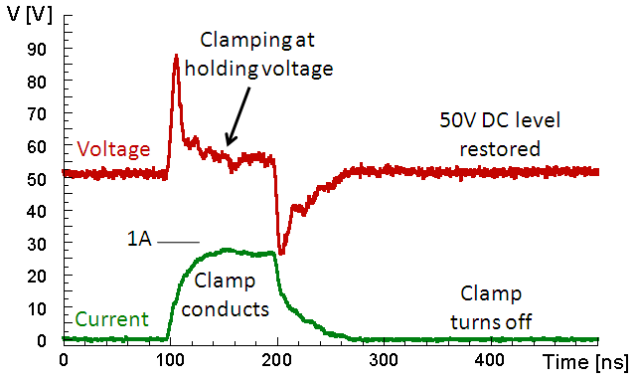

Figure 10: Transient latch-up test where a 1 ampere TLP pulse is superimposed on a 50V bias level. After the TLP pulse the voltage restores to 50V while the current through the clamp returns to the (leakage) level before the TLP pulse. The hebistor clamp does not remain latched.

Another important test investigates the turn-off behavior of the hebistor clamp. Figure 11 shows the measurement setup and resulting voltage and current waveforms.

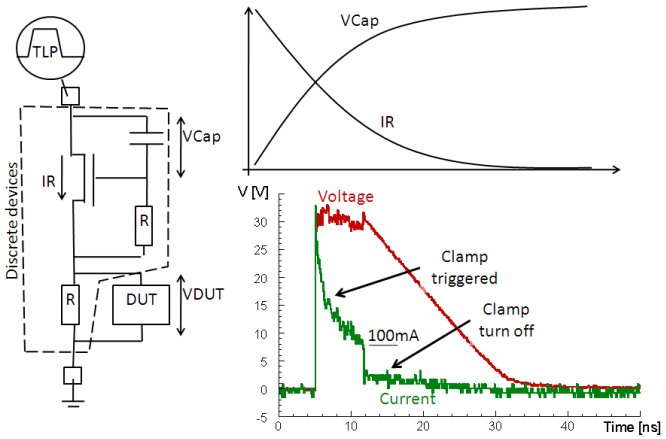

Figure 11: Measurement setup (left) to validate the turn-off behavior of the hebistor clamp. The setup stresses a discrete HV MOS device with TLP pulse to create a pulse with a fast rising edge and slow falling edge. The measurement (bottom right) shows that the hebistor (30V clamp) is first triggered (fast rising edge), clamps the voltage at its holding voltage and is then turned off clearly showing the holding voltage of 30V.

The robustness level scaling to any HBM level was verified by extensive silicon testing.

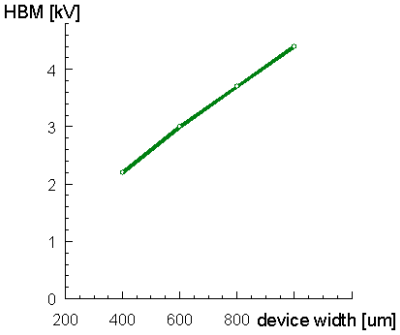

Figure 12: HBM performance for different hebistor device widths: a linear scaling is achieved.

To check for hidden degradation effects, the final hebistor clamps have been stressed multiple times at a level of 80% of the It2 failure current. No degradation effects were found even after 2,000 stress pulses.

Different variations are possible of the hebistor device such that the trigger voltage and holding voltage can be tuned. This ensures that various application types and IO circuits can be protected with the same generic approach. Figure 9 (left side) demonstrates that the holding voltage can be tuned to a broad set of values through the use of different clamp body types combined with tuning control circuits. Because the trigger voltage (Vt1) and holding voltage (Vh) can be tuned independently the hebistor device can be used for many different applications and interfaces including IO and supply protection.

IV. Conclusion

While high voltage interfaces are broadly used in many IC applications like motor control, power management and conversion, LCD panel drivers and automotive systems, IC designers still lack a low leakage, cost effective and latch-up immune ESD protection clamp.

While IC designers worldwide continue to produce very creative systems and applications based on HVCMOS or BCD technology nodes the ESD protection clamps have almost not evolved: the industry is still using large area, highly leaky clamps that typically require extensive process tuning and time consuming trial and error experiments and analysis.

This paper introduced a newly developed protection device, called hebistor clamp, and compared it with the traditional approaches, based on measurements on TSMC 0.35um 15V and TSMC 0.25um 40V technology. In the 0.25um BCD technology the novel hebistor device with holding voltage above 40V achieves more than 4kV HBM, 200V MM while the leakage and capacitance stay well below typical requirements (<10nA and <250fF).

Thanks to the high holding voltage, the hebistor devices are latch-up immune for the various industry standard requirements including transient latch-up, long pulse durations and high temperature conditions.

Note

As is the case with many published ESD design solutions, the techniques and protection solutions described in this paper are covered under patents and cannot be copied without the appropriate license agreement.

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[26] Agilent 8114A, 8110A User Guides and Application Notes

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Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

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