Conference paper

Protection of a 3.3V Domain and Switchable 1.8V/3.3V I/O in 40nm and 28nm 1.8V processes

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Today's advanced technologies' overdrive transistors cannot always meet the signal speeds of existing standards. This paper describes the issues, solutions and results to build the necessary protection for HBM, MM, CDM and latch-up for a 3.3V domain and 1.8V/3.3V I/O, based only on 1.8V transistors, in a 40nm process. Results of the design ported to 28nm are also presented.

Protection of a 3.3V Domain and Switchable 1.8V/3.3V I/O in 40nm and 28nm 1.8V processes

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Abstract - Today's advanced technologies' overdrive transistors cannot always meet the signal speeds of existing standards. This paper describes the issues, solutions and results to build the necessary protection for HBM, MM, CDM and latch-up for a 3.3V domain and 1.8V/3.3V I/O, based only on 1.8V transistors, in a 40nm process. Results of the design ported to 28nm are also presented.

I. Introduction

With shrinking technology parameters, the I/O and power supply voltages have been reduced from a gentle 5V in 0.25µm processes over 3.3V in 0.13µm to 1.8V or 2.5V in 40nm. For compatibility with legacy devices and standards, sometimes I/O devices are required whose voltage swing exceeds the nominal I/O voltage. For this purpose, overdrive transistors are provided, which are capable of handling a drain voltage, larger than nominal. For extreme tight timing constraints, however, these transistors are inadequate and the intelligent use of stacked standard transistors is required. This may look straightforward for an input but is obviously not for an output structure, since driving the output to 3.3V requires a separate power domain. To protect such structures under all possible working conditions against HBM, MM, CDM and latch-up, is the scope of this paper. First, the circuit to be protected will be shortly explained based on analysis of 40nm CMOS, followed by the protection concept, the different clamps used and finally the results on both 40nm and 28nm.

II. 1.8V/3.3V I/O circuit

The circuitry is developed using standard I/O transistors to get superior specs compared when using overdrive transistors. It converts 1.8V internal signaling to 3.3V or 1.8V level input/output while using only 1.8V devices. As an additional benefit, the extra 3.3V overdrive mask is no longer required.

Typical applications are legacy card interfaces like SIM and SDXC interfaces.

A. I/O design

The circuitry has 4 different supply voltages: VDD3V3 and VDD1V8 as power lines and VSS_IO and VSS_core as ground lines, where the latter is used as substrate voltage. Basically the I/O circuitry (Figure 1) has to be able to both receive and transmit 1.8V as well as 3.3V signals. The transmitter is composed out of 2 different signal paths, for 1.8V and 3.3V, each with different specs. A logic block selects what signal level should be sent to the output pad. The receiver is set up so that both signal levels can be handled. Controlled pull-up structures finally define the high impedance state.

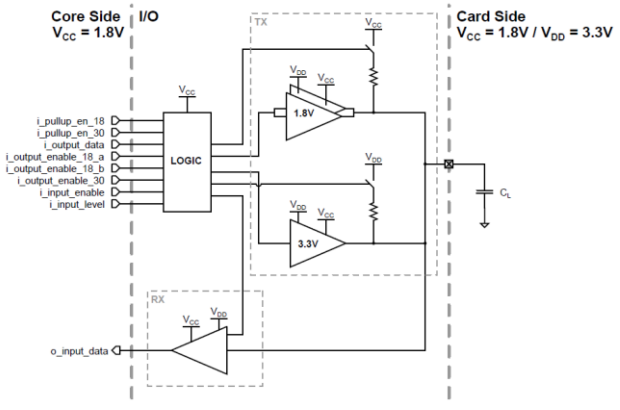

Figure 1: Block diagram of I/O circuit, with dual drivers, single receiver and logic control block

B. Design window

Since in worst case, a cascoded NMOS transistor pair can have a V_{t1} as low as a single transistor [1 – 5], the design window was set to V_{max} of 6.5V for the I/O port. Figure 2 shows the different TLP-IV curves measured on a 40nm CMOS process: 280µm wide devices with a merged bulk have a V_{t1} of approximately 7 volts, while devices with the bulk separated may show a larger V_{t1}, pending the gate bias condition. The design window is larger for the PMOS transistor pairs with separated bulk and also for the power domain due to the combination of both NMOS and PMOS cascoded stacks. This in turn has implications on the protection strategy: when optimizing for the power clamp design window, a dual diode solution for the smaller I/O design window proved not to be feasible.

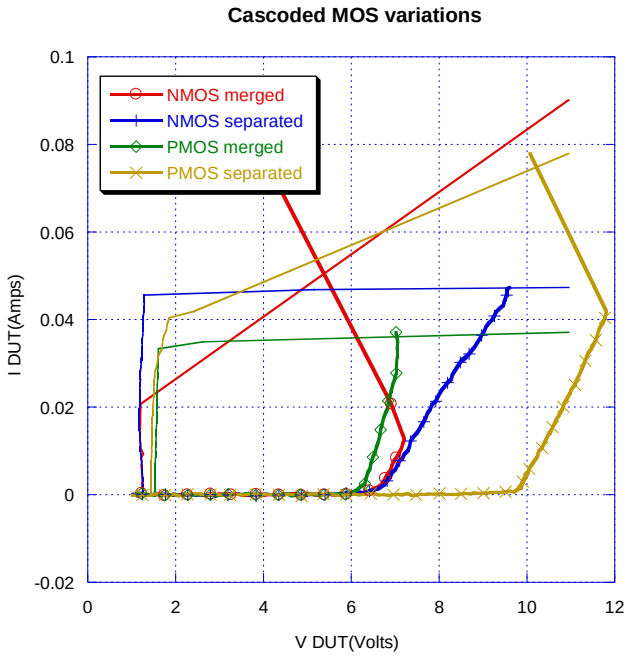

Figure 2: TLP-IV curves of different cascoded MOS structures, with merged and separated bulk, measured on TSMC 40nm

III. Protection

Protection for 2kV HBM and 200V MM was requested, while reaching a CDM level of 250V without additional CDM-specific structures was preferred. At the same time, the solution had to be latch-up immune (JESD78A, 100mA). The resulting clamps are supposed to be plug-and-place devices, fitting into the foundry's existing power bus routing. A bus extension for the new 3.3V domain is added. Protection of the regular 1.8V domain is handled by the foundry's standard solution.

A. Protection concept

1. Power clamp

Basically, single MOS based techniques cannot be applied on overvoltage structures: since all voltages applied to these MOS, even in cascodes, need to be limited to the nominal voltage of 1.8V, the challenge would shift from protection against transients to protection against DC voltages. An ESD structure, independent of the fragile MOS oxide, is required. Hence as a first candidate, it is opted to use a Sofics proprietary, level triggered DTSCR [6, 7] for PC1.

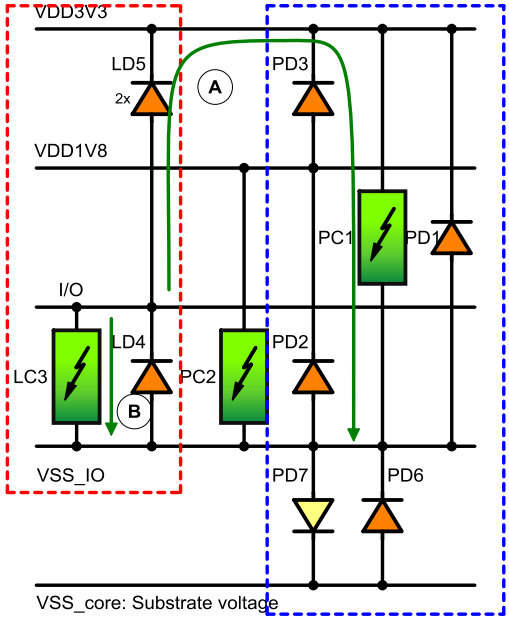

Figure 3: Conceptual diagram with local protection (red) and power protection (blue)

2. I/O clamp

No diode is allowed between the I/O pin and the VDD1V8 supply, since this would not allow for 3.3V signals. Furthermore the sum of the voltage drops over the diode to VDD3V3, the 3V3 power clamp and possible bus resistance (see path A in Figure 3) may exceed the given design window, hence a local approach (path B) is chosen, instead of a dual diode approach. This results in a protection scheme as shown in Figure 3. All PD symbols are diodes which are located inside the 3.3V ESD Power clamp module, together with the 3.3V Power clamp (PC1). The local diodes (LDx) are placed together with local clamp (LC3) in each I/O block. Finally, for protection of the default 1.8V domain, the foundry's solution (PC2) has been used.

B. Clamp construction

1. Power clamp

Creating a DTSCR for a 3.3V domain, requires a large number of trigger diodes to keep leakage low and a large number of holding diodes to keep the holding voltage above VDD3V3 avoiding latch-up. The large number of holding diodes may form a large resistive load for the SCR, so they need to be sized up to keep the overall on-resistance low. Leakage, another concern, through the PNP behavior of P+/N-Well diodes is kept low by the use of isolated diodes and SCR.

Based on silicon selection, a DTSCR with 4 trigger diodes and 3 holding diodes (Figure 4) comes out as primary candidate. The complete clamp uses less than 2000µm² of area. The power clamp module (Figure 5), containing all necessary diodes as mentioned above, consumes less than 4000µm² of area, and fits directly into the foundry's existing bus-structure.

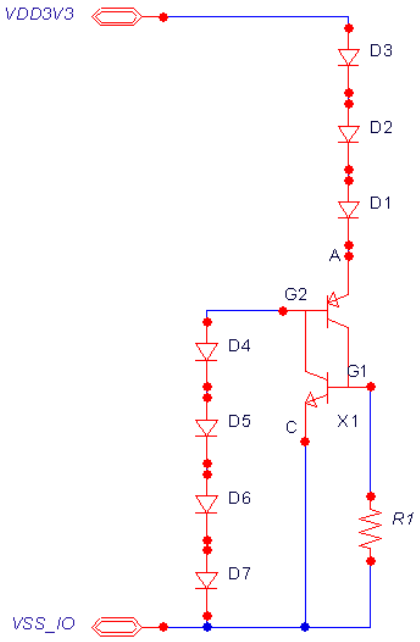

Figure 4: Schematic representation of the power clamp PC1, a DTSCR with 4 trigger diodes and 3 holding diodes.

TLP-IV analysis of the standalone clamp PC1 is shown in Figure 6. This standalone clamp can handle 3.5A of TLP current and can accordingly handle >4kV HBM and > 400V MM. The high values are caused by the size of this clamp, which was mainly scaled for resistance reasons. It can thus easily handle the 2kV HBM of the original specifications.

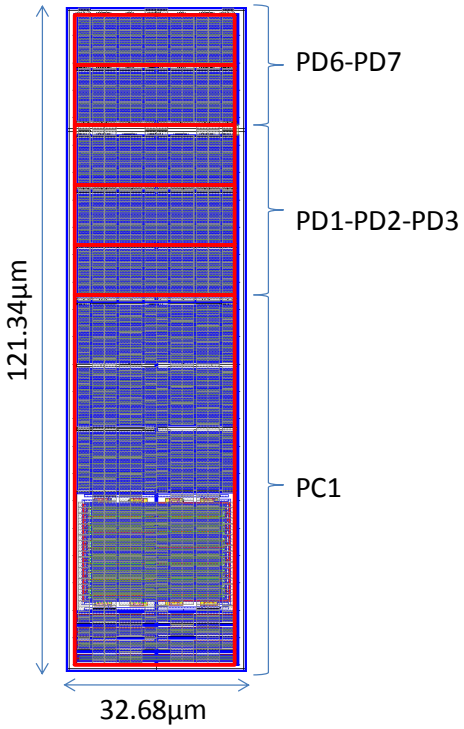

Figure 5: Layout of the complete structure at VDD3V3 in 40nm, its overall size less than 4000µm²

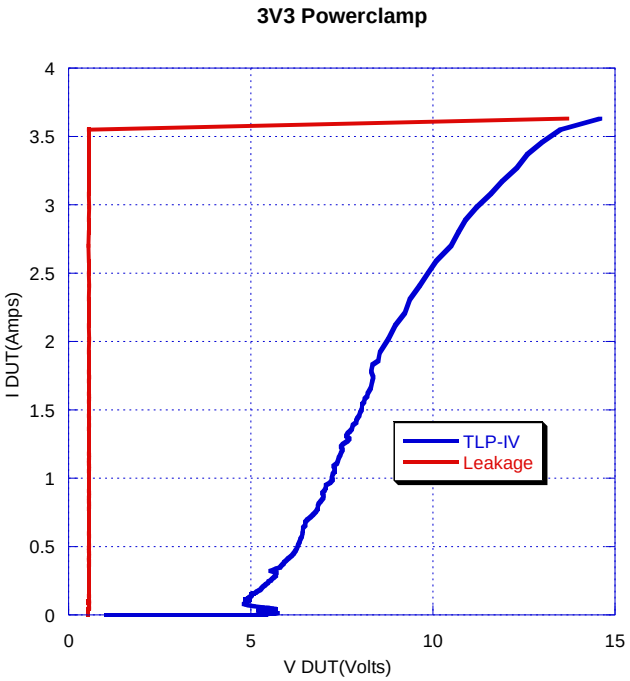

Figure 6: TLP-IV curve for standalone power clamp PC1 measured on the 40nm test chip.

Alternative power clamp candidates are made, by means of other triggering techniques including RC-MOS. Again, all MOS devices may not exceed the nominal voltage during normal operation, thus requiring a stacked solution.

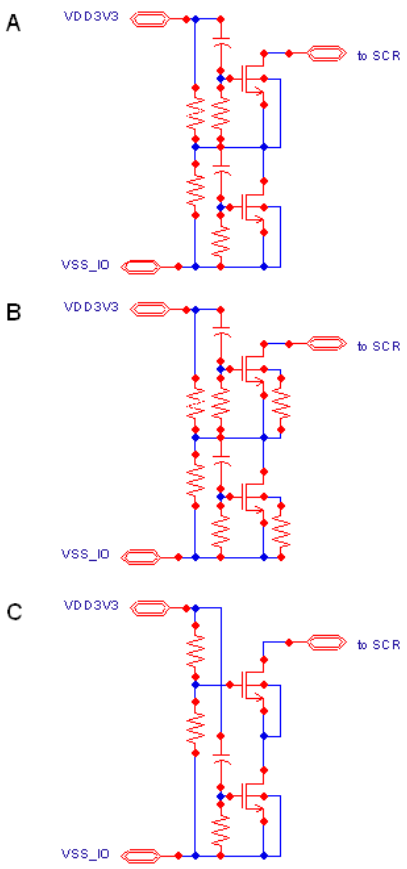

Figure 7: Different RC triggering topologies:
A) Double RC triggering,
B) Double RC triggering with bulk bias
C) RC triggering with MOS bias

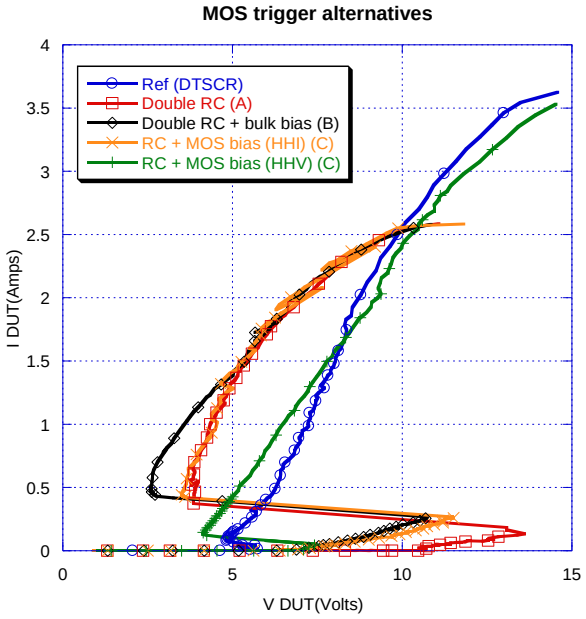

Figure 8: TLP-IV curves for clamps with alternative MOS trigger circuits on 40nm.

Figure 7 shows the different topologies. Topology A uses two basic RC-triggered MOS which have been stacked. A voltage dividing network, here represented by 2 resistors, biases the midpoint. Adding some bulk bias returns topology B. Finally, biasing the upper MOS to an acceptable level for DC and triggering the lower MOS is shown in C.

This stacked solution has been combined with 2 different latch-up risk limiting techniques: the high-holding voltage technique (HHV), using holding diodes, and the high-holding/high-trigger current technique (HHI) [9].

Figure 8 shows topology A, B and C which have been combined with the HHI and topology C combined with the HHV.

All devices have a higher V_{t1} than the DTSCR. Engineering these to get a similar or smaller trigger voltage may increase the area consumption. MOS-based capacitors must be stacked in order not to compromise gate-oxide integrity.

Another advantage of the DTSCR is that its V_{t1} will not shift when the chip is powered up, unlike RC-triggered devices.

2. I/O clamp

To meet the severe constraints in design window, the local clamp (LC3) is set up as an ESD-ON-SCR [8].

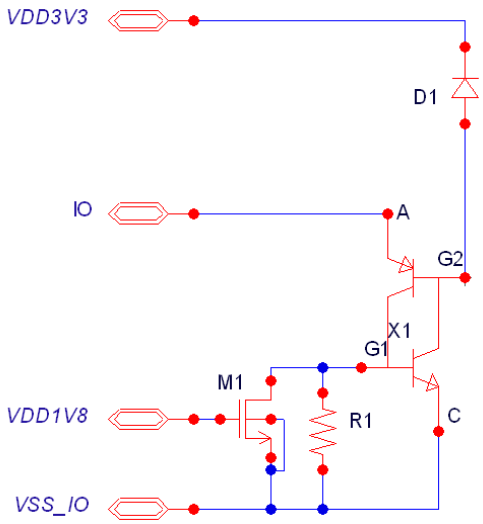

Figure 9: Schematic representation of the local clamp LC3+LD5, an ESD-ON-SCR extended with the HHI-SCR principle.

A local DTSCR pair could be possible but would require a larger area. To avoid latch-up of the clamp when sourcing current, the ESD-ON-SCR (Figure 9) has been implemented as a high-holding/high-trigger current SCR (HHI-SCR) [9]. This is obtained by use of an additional controlling MOS M1, connecting the SCR's first gate to VSS_IO when powered up.

In case of an event which could cause latch-up, the I/O pin will see only the 2 diodes to VDD3V3, while the SCR will stay turned off.

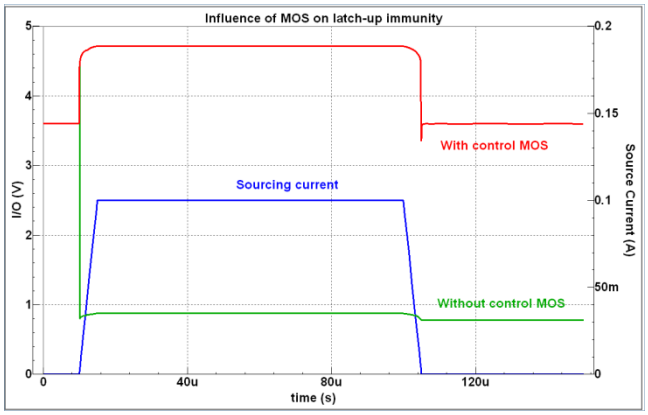

Figure 10: Latch-up test simulation results for local clamp

Simulation of this technique (Figure 10) reveals indeed that the SCR will not trigger when a 100mA sourcing current is applied in case a HHI MOS is present, and does trigger when not present.

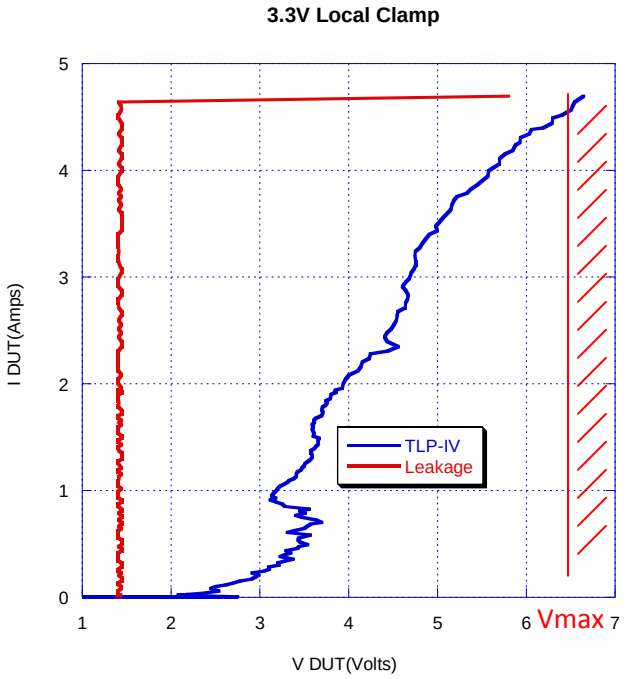

Figure 11: TLP-IV curve for local clamp LC3+LD5 from engineering test chip (full I/O ring) on 40nm

From Figure 11, the TLP-IV curve shows that the clamp efficiently protects the I/O. The structure was measured on a fully functional I/O ring, hence the capricious curve. The assumed design window indeed matches the real-life breakdown value.

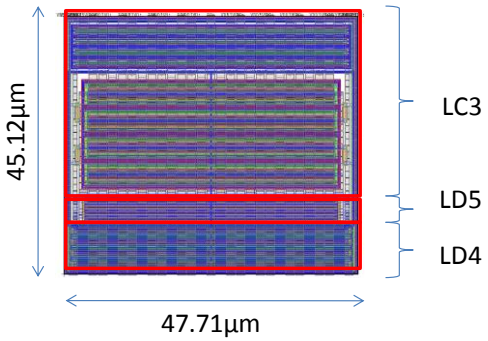

Figure 12: Layout of the complete structure at I/O in 40nm, its overall size approximately 2150µm²

Figure 12 shows the complete structure at any I/O. The area consumption is only 1700µm² for the local clamp LC3+LD5, 2150µm² including the diode down (LD4 in Figure 3).

IV. Product integration and results

The solutions have been integrated in both an engineering test chip and in a full production multichip stacked BGA.

The engineering test chip was a fully functional I/O ring, wire bonded in DIL and QFP packages. The Power domain segment had 3 power clamp modules connected. As seen from the results from Table 1, the HBM and MM values, measured with a KeyTek Mk2, strongly exceeded the default specs of 2kV and 200V.

Table 1: Results from engineering test chip on 40nm

Device	HBM	MM	LU
3.3V domain (3x clamp)	>8kV	>600V	V-test pass VDD + 50%
3.3V IO	>7kV	>300V	I-test pass 100mA

Table 2: Qualification results on 40nm samples, measurements are only performed till spec requirements

Production Device	HBM qualified	CDM qualified
3.3V domain (3x clamp)	> 2kV	> 400V
3.3V I/O	> 2kV	> 400V

Since CDM values are very package dependant, these have been evaluated (Table 2) on production parts, which are flip-chip BGA's, by measurements on a KeyTek RCDM3. This resulted in a qualified (on 3 parts fully tested) CDM protection level > 400V.

Also HBM was fully qualified above 2kV. Further testing till 3kV, outside the qualification, did not reveal any failure either, so one can expect that the ratings are in line with the test chip.

V. 28nm results

Based on the achieved results the partners decided to cooperate on a 28nm version of the IO and ESD protection. The same on-chip ESD protection approach was used as described above for the 40nm case. The IO circuits were placed in an IO section (

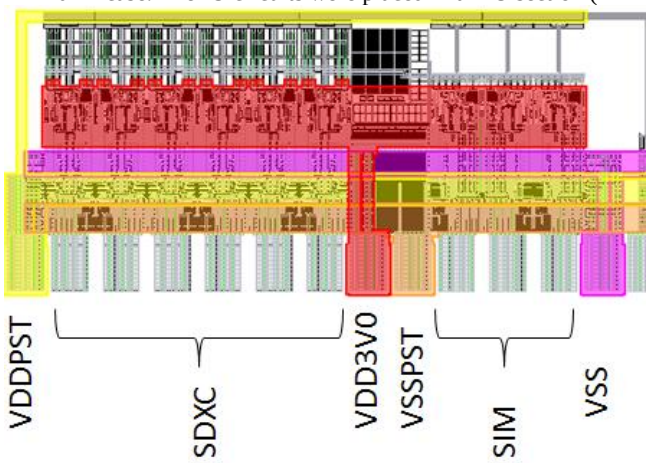

Figure 13) on a 28nm MPW run.

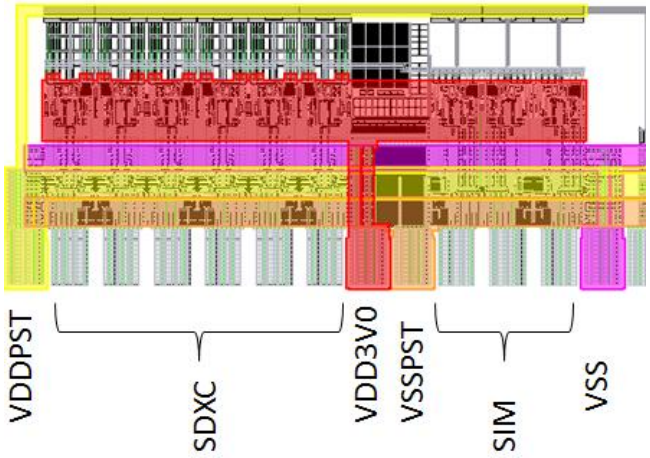

Figure 13: layout of the I/O ring on the 28nm MPW test chip. The protection approach is similar to the design on 40nm

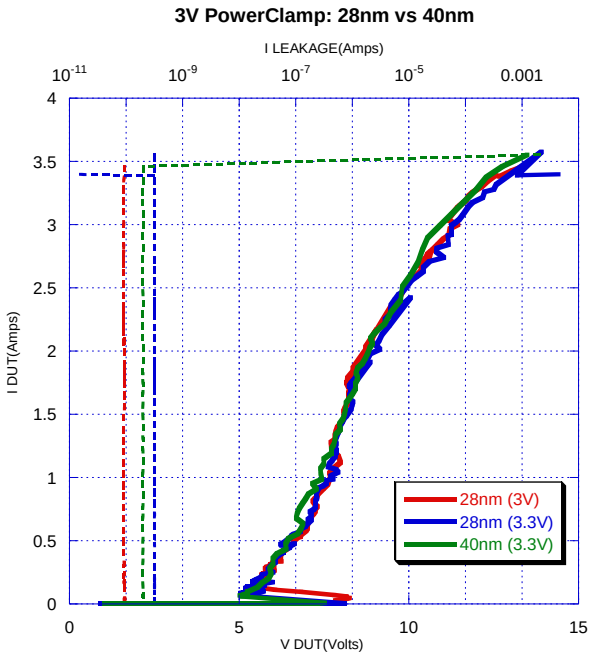

Figure 14: TLP-IV curves comparing the 3.3V power clamp behavior on 40nm and 28nm. Clearly the difference is very small

Figure 14 shows the TLP IV curves for the 3.3V clamp measured on both 40nm and 28nm. It is obvious from the results that the behavior is identical on both processes.

VI. Conclusions

The protection of a 3.3V domain and mixed 1.8V/3.3V I/O cell in a 1.8V technology by using a DTSCR as power clamp and a dedicated ESD-ON SCR as local clamp returned very good results. Further on, latch-up was eliminated by holding diodes for the power clamp and a novel implementation of the HHI-SCR principle in the ESD-ON SCR.

A 28 nm version has been developed showing very similar results proving the portability of the ESD technology.

Acknowledgements

Many thanks go to the different design groups at Sofics, ICsense and Icera, for co-operation to meet the tough specs and deadline dates and for open communication to get the maximum out of this new product.

Notes

As is the case with many published ESD design solutions, this publication describes techniques and

protection solutions that are protected by patents and patents pending and cannot be copied freely.

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ESD SOLUTIONS AT YOUR FINGERTIPS

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
    - Enable unique requirements for Latch-up, ESD, EOS
    - Layout, metallization and aspect ratio customization
    - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

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