Conference paper Protection strategy for EOS (IEC 61000-4-5)

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Protection strategy for EOS (IEC 61000-4-5)

Bart Sorgeloos, Ilse Backers, Olivier Marichal, Bart Keppens

Sofics, Brugse Baan 188A, B-8470 Gistel, Belgium,
phone: ++32-9-21-68-333; fax: ++32-9-3-746-846; e-mail: bsorgeloos@sofics.com

Abstract The standard IEC 61000-4-5 is used to characterize IC designs for EOS robustness. Each chip should achieve a minimum level of protection to withstand against EOS. Based on Long TLP and simulation, a strategy is developed to handle this requirement. The methodology has been applied for a T-con product in 130nm CMOS.

I. Introduction

The last few years, there is a large interest to provide beside on-chip ESD protection also on chip EOS protection. More than 40% of the field failures are related to EOS. The big challenge with EOS is defining it. In the industry, the IEC 61000-4-5 standard [1] has been used to simulate EOS stress. A strategy to define EOS protection by correlating Long TLP results with the IEC61000-4-5 standard is presented in this paper and a calculation/simulation flow is suggested. This protection methodology has been developed for a T-con or timing controller inside a LCD TV.

A T-con or timing controller is the link between the external signals received by the LCD TV and the internal display drivers. Misalignment of the connector on the PCB and the FFC (Flat Flexible Cable) is very often observed. A first correlation between these field failures and a specific surge test was found by Jae-Hyung Kim [2]. It was shown that a simulator based on the IEC61000-4-5 standard gives the same failures as in the field. This paper continues by providing a strategy for protecting the T-con IC to a certain level of IEC61000-4-5

II. IEC 61000-4-5

IEC 61000-4-5 is one of the standards published by the international electro technical committees (IEC) relating to the electromagnetic compatibility (EMC) of systems. This specific standard relates to the immunity requirements caused by over voltages from switching and lightning transients.

A simplified representation of the EOS simulator is shown in Figure 1. It is defined by a high voltage source, an energy storage capacitor C_c and a charging resistor R_c as the source for the surge stress. The resistors R_{s1} and R_{s2} define the pulse duration, the inductor L_r is included to define the rise time and the resistor R_m functions as an impedance matching circuit.

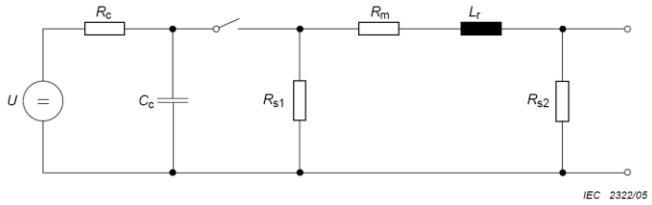

Figure 1: Simplified circuit diagram of the simulator: C_c= 5uF, R_{s1}=32 Ohm, R_{s2}=21 Ohm, R_m=2 Ohm and L_r=11uH

The characteristics of the voltage/current waveforms at the output of the simulator are defined by 2 loads: an open (Figure 2) and short (Figure 3).

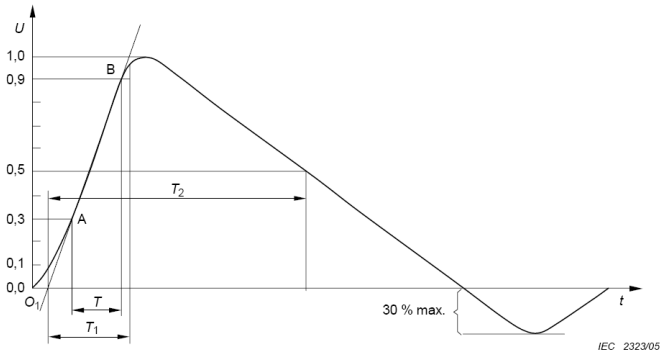

Figure 2: Open-circuit voltage waveform (1.2/50 µs) at the output of the simulator

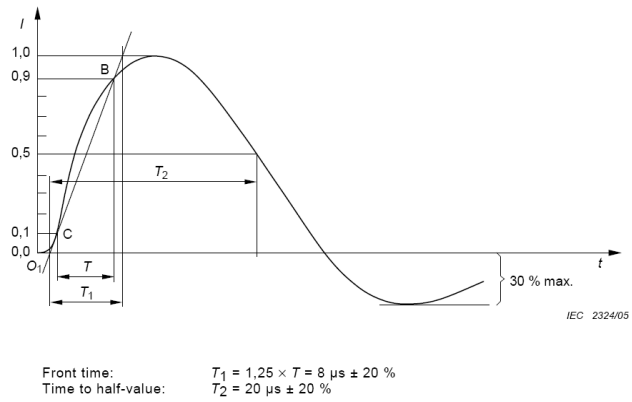

Figure 3: Short-circuit current waveform (8/20 µs) at the output of the simulator

The simulator has an internal 2 Ohm resistor. This means that 100V at an open circuit correlates to 50A for a short circuit. Systems, stressed at the power supply, can achieve a level between 0.5 kV to 4kV. At this level the current (250A to 2000A) is too high to sink safely through on-chip protection circuits.

While this test is not meant as IC device level test many system manufacturers require that a certain (lower) level must be achieved on chip according to this test since it correlates well with field failures. For example, for the T-con IC, besides the HBM ESD requirements, also 12V up to 19V EOS requirements had to be fulfilled for the 3.3V IO. For a commonly used 'dual diode' ESD protection, the diode will shunt 5.5A for instance from GND to IO. The amount of current is determined by the stress level (example 12V) minus the voltage over the DUT, divided by the internal 2 Ohm resistance of the simulator. Hereby it is assumed 1V built-in voltage and the resistance of the diode is neglected. When the diode is replaced by a clamp with a higher clamping voltage (for example 10V) then the current during EOS surge stress is much lower at 1A. But a 10V clamping voltage causes problems during ESD stress.

In defining an optimal solution for ESD as well for EOS, an iterative strategy is found to primarily limit the EOS current, and secondly to handle the ESD current. This strategy will be explained in the next section.

III. Strategy for EOS protection

For achieving an efficient protection, for both ESD and EOS an adequate strategy is needed. The flow can be divided in the following steps:

1. Characterize the protection structures with and without monitor structures for ESD (HBM, MM, CDM) and for EOS (IEC 61000-4-5)
2. Define a correlation between TLP and ESD performance and between Long TLP and EOS.
3. Define a calculation/simulation rule for an efficient ESD/EOS protection strategy

1. Characterization of protection devices for IEC 61000-4-5

The first step is to characterize the failure voltage and the failure current of different ESD protection devices used in a certain technology. The measurements are done with an IEC 61000-4-5 simulator (KT 200SG surge tester [3]), an oscilloscope and a parametric analyzer. The DUT is stepwise increased from 1V up to the failure voltage. For each stress pulse, the peak current is monitored and the failure is defined by a 10% shift in the IV curve of the device. The results are shown in Table 1. Note that the process has already a natural level of protection. For example, the minimum level that a device can handle on its own is at least its DC trigger voltage. But levels just above this value could already cause too much current.

Device (2 different 0.13um technologies)	**Failure level**	**I_{peak} (before failure)**
GGNMOS triggered SCR(technology 1)	5 V	1.28 A
N+/PW diode (technology 1)	6.2 V	1.27 A
N+/PW diode (technology 2)	5.2 V	1.30 A
P+/NW diode (technology 1)	5.6 V	1.15 A
GGNMOS triggered SCR with 3 Holding diodes (technology 2)	16 V	2.26 A
GGNMOS triggered SCR with 1 Holding diode (technology 2)	12 V	2.56 A
GGNMOS triggered SCR with 2 Holding diodes (technology 1)	12 V	2.08 A
GGNMOS triggered SCR (technology 2)	>15 V	> 6.8 A
Back-end-ballasting NMOS	>15 V	> 6.3 A

Table 1: IEC 61000-4-5 measurements

2. Correlation between IEC 61000-4-5 and long TLP

A second step in the flow is to find a correlation between IEC 61000-4-5 and Long TLP (TLP with different pulse durations). Therefore the same structures were measured with a TLP system with different pulse durations.

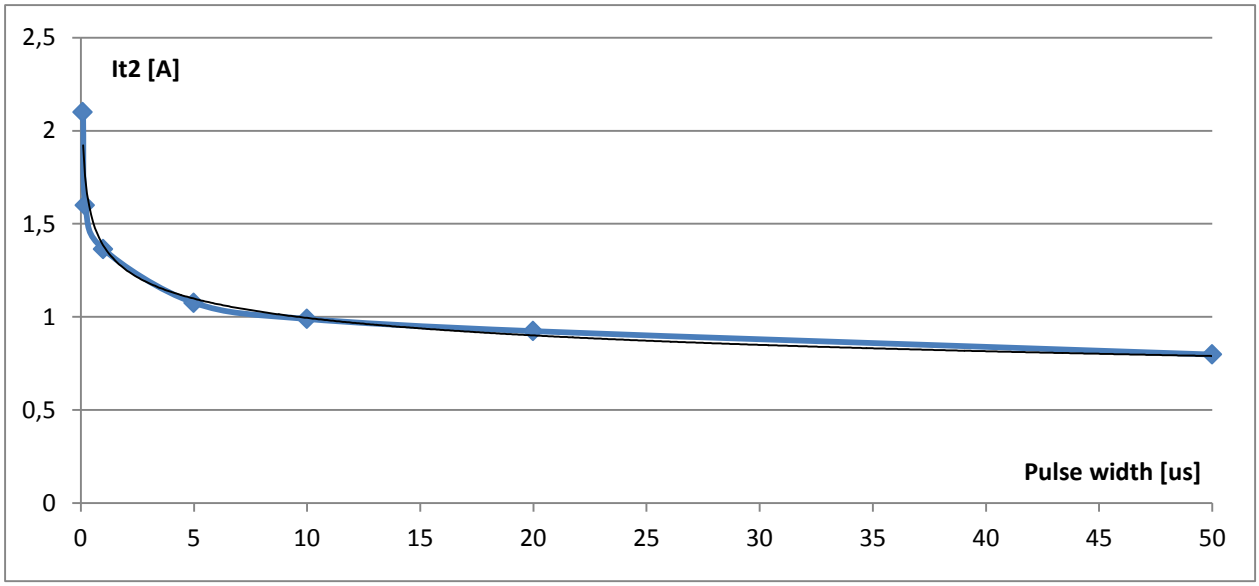

Figure 4: It2 versus pulse duration of an N+/Pwell diode measured with long TLP.

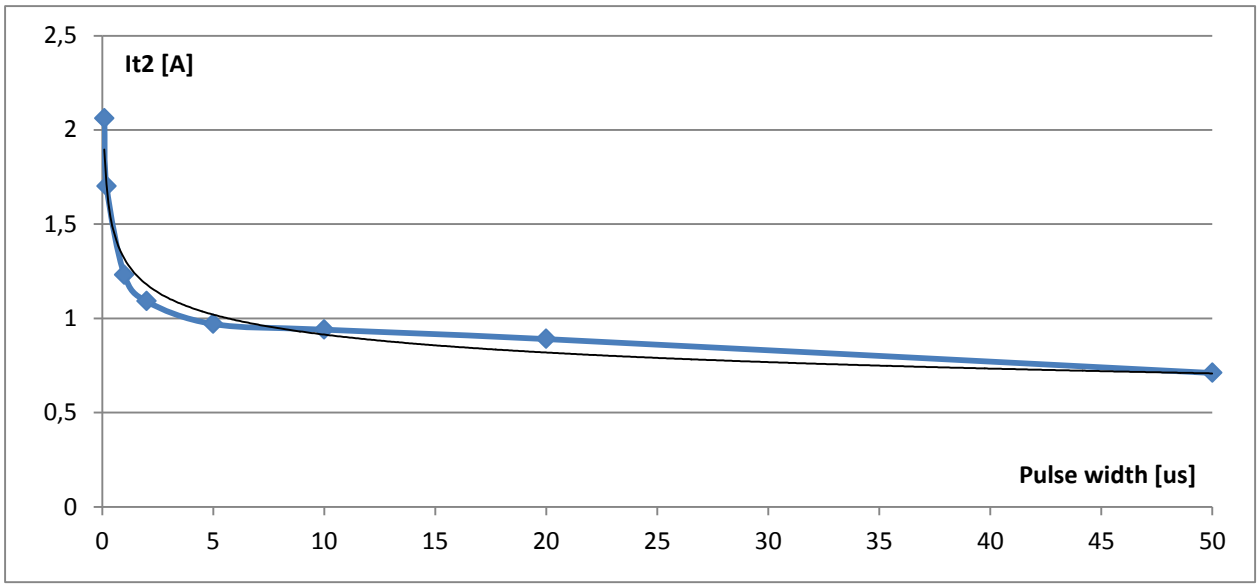

Figure 5: It2 versus pulse duration for GGSCR devices measured with long TLP.

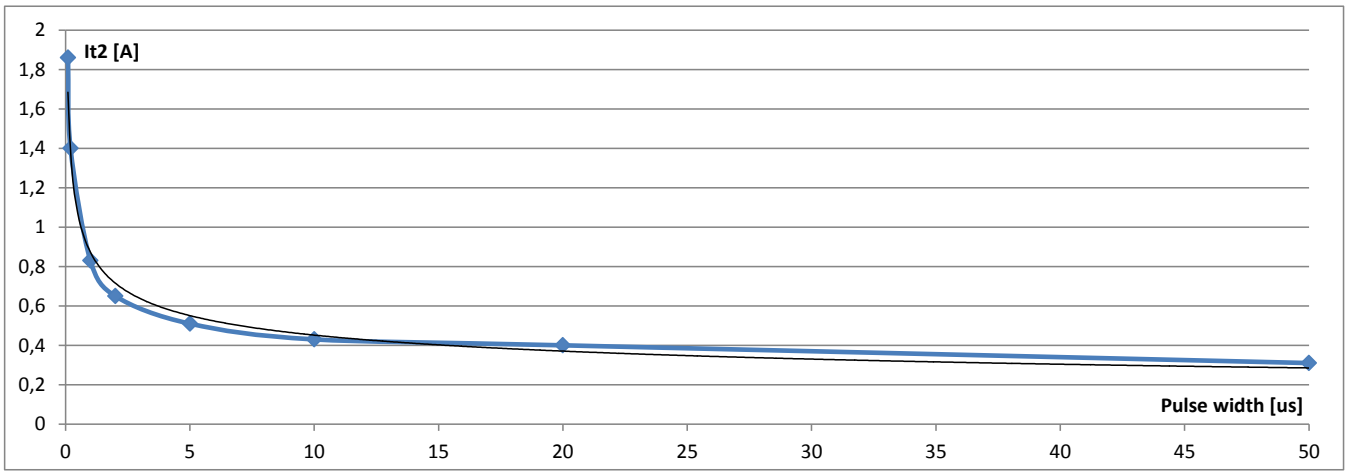

Figure 6: It2 versus pulse duration for metal lines measured with long TLP.

Figure 4, Figure 5 and Figure 6 shows the resulting failure current of an N+/Pwell diode, GGSCR [5] device and metal lines for different TLP pulse durations: the expected "Wunsch-Bell" [4] curves. The TLP curves are show in Figure 7 and Figure 8.

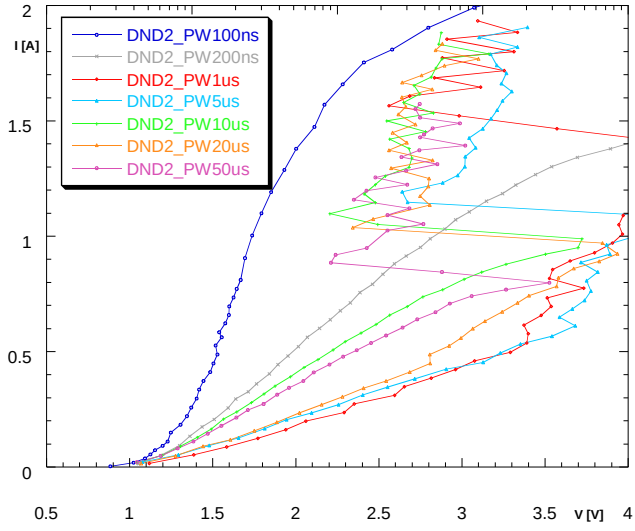

Figure 7: (long) TLP curves with different pulse durations for an N+/Pwell diode.

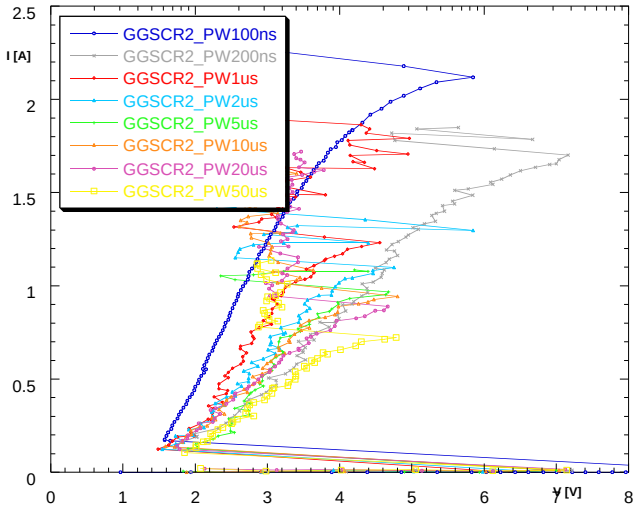

Figure 8: (long) TLP curves with different pulse durations for the GGSCR device.

When comparing the failure current (Table1) during the IEC 61000-4-5 stress and the failure current (4, 5, 6) during long TLP it can be concluded across different devices, samples and technologies that the 2us TLP pulse duration failure current matches best with the peak current of the EOS pulse.

A following step consists of characterizing all the possible sensitive elements for the EOS stress. For example Table 2 shows the failure voltage for the sensitive gate oxides, while Table 3 shows the results of ESD protection devices suitable for this technology.

Core/GOX design window	$V_{t2,d}$ (V)	$V_{max,d}$ (V)
LV – GOX NMOS	5.00	4.50
LV – GOX PMOS	5.63	5.63
HV – GOX NMOS	11.16	11.16
HV – GOX PMOS	13.25	13.25

Table 2: Long TLP results based on 2µs TLP results

ESD/EOS clamp	V_h (V)	I_{max} (mA/um)	R_{on} (Ohm.um)
Power clamps			
1.2 V DTSCR	1.82	17.00	110
3.3 V GGSCR with holding diodes	4	15.26	129
Local clamps			
1.2 V DTSCR	1.1	17.25	106
ESD-on-SCR	1.1	16.73	106
RTSCR (version 1)	1.1	15.45	106
GGSCR (version 1)	1.1	16.73	106
GGSCR (version 2)	1.1	16.73	106

Table 3: Long TLP results based on 2µs TLP results

3. Calculation/simulation rule for IEC 61000-4-5

The approach for a successful EOS protection consists of 4 steps. The strategy is summarized in Figure 9.

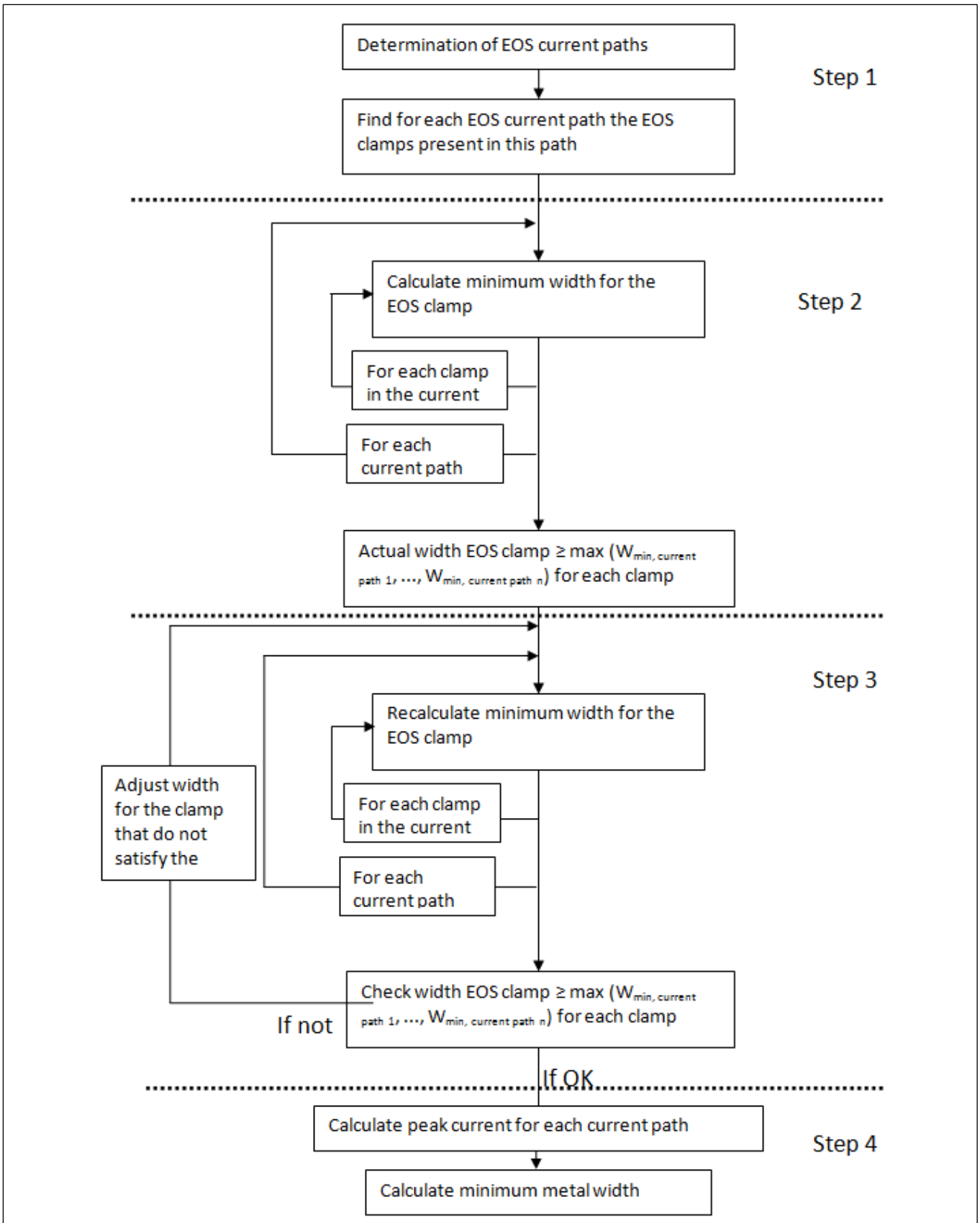

Figure 9: Flow chart for the EOS procedure

Step 1: Determination of the EOS current path

First the EOS path must be determined for each stress case that is applied:

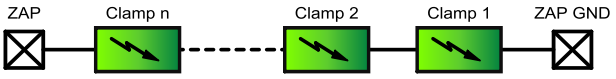

Figure 10: EOS current path

The EOS path can consist of n different clamps. For example, when there is a stress between VDD (ZAP) and IO (ZAP GND), the ESD path consists of a power clamp (clamp2) in series with a diode down (clamp1) if a 'dual diode' protection approach is applied.

Step 2: Calculate width of the EOS/ESD clamp

From the simplified circuit diagram of the tester a formula can be derived to calculate the minimum width for each ith clamp in the EOS path:

$$W_{min,i} = \frac{1}{2}\cdot\left(\frac{\left(V_{EOS} - \sum_{j=1}^{n}(V_{h,j})\right).1000}{I_{max,i}'} - \sum_{j=1}^{n}\left(R_{on,j}'\cdot\frac{I_{max,j}'}{I_{max,i}'}\right)\right) \quad (i = 1 \dots n)$$

With:

$W_{min,i}$: *minimum width for the* i^{th} *EOS/ESD clamp* (um)
V_{EOS} : *level of EOS protection*
$V_{h,j}$: *holding/clamping voltage*
$I_{max,j}'$: *normalized maximum current* (mA/um)
$R_{on,j}'$: *normalized on − resistance* $(Ohm.um)$

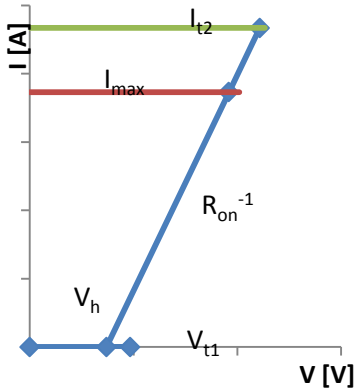

Figure 11: A simplified representation of the behaviour of the protection device under Long TLP

For each ESD clamp these parameters can be extracted as in step 2.

This formula must be applied for all the possible current paths. For each clamp the worst (largest) minimum value must be taken and the actual width for each clamp must be larger or equal than this value.

Step 3: Iteration of the actual width

This step is necessary when you have more than 1 clamp in the EOS/ESD path (n>1).

It is important to understand that if a larger width is selected, the minimum width of all the other clamps will also have to be changed: larger devices have lower on-resistance, inducing larger peak currents. The EOS source is neither current nor voltage driven: the stress that is seen by the clamp is also influenced by the clamp itself. Each element has an impact on the parameters of the other elements.

For each clamp the minimum width must be recalculated with the widths of the other clamps, i.e. the actual chosen widths of these clamps, with the following formula

$$W_{min,i} = \frac{\left(V_{EOS} - \sum_{j=1}^{n}(V_{h,j}) - \frac{I_{max,i}'\cdot R_{on,i}'}{1000}\right)}{\frac{I_{max,i}'}{1000}\cdot\left(2 + \sum_{\substack{j=1 \\ j\neq i}}^{n}\left(\frac{R_{on,j}'}{W_j}\right)\right)} \quad (i = 1 \dots n)$$

With:

$W_{min,i}$: *minimum width for EOS/ESD clamp* (um)
W_j : *actual width for EOS/ESD clamp* (um)
V_{EOS} : *level of EOS protection*
$V_{h,j}$: *holding/clamping voltage*
I_{max}' : *normalized maximum current* (mA/um)
R_{on}' : *normalized on − resistance* $(Ohm.um)$

If this calculated minimum width is smaller or equal than the actual width, it is OK. Otherwise this clamp size must be increased.

This process must be done iteratively until all widths are confirmed: if one device structure perimeter is changed the formula must be reapplied for all current paths and EOS clamps.

Step 4: Calculate peak current through the clamp

The 4th step is to calculate the peak current through the clamps. In this stage the actual widths of the ESD clamps are used.

$$I_{peak} = \left(\frac{V_{EOS} - \sum_{j=1}^{n}(V_{h,j})}{2 + \sum_{j=1}^{n}\left(\frac{R_{on,j}'}{W_{clamp,j}}\right)}\right) + 10\%\ safety\ margin$$

With:

I_{peak} : *peak current during EOS* (A)
V_{EOS} : *level of EOS protection*
$V_{h,j}$: *holding/clamping voltage*
$R_{on,j}'$: *normalized on − resistance* $(Ohm.um)$
W_{clamp} : *the actual width of the EOS/ESD clamp*

This peak current can be used for the calculation of the required metal width:

$$W_{metal,min} = \frac{I_{peak}}{I_{max,metal}'}.1000$$

With:

$I_{max,metal}'$: *the normalized maxium current through a metal line* (mA/um)
$W_{metal,min}$ = *minimum width of the metal* (um)

Note: all parameters mentioned above are EOS parameters of the clamps. These are different from the ESD parameters.

IV. Example calculation

This section shows an example calculation to determine the optimal size of the EOS/ESD clamps for the different stress cases for the ESD protection concept shown in **Figure 12**. The EOS stress tests involve 4 cases: IO to ground (PS), Ground to IO (NS), IO to VDD (PD) and VDD to IO (ND). The conduction path is different for each stress case as shown in **Figure 13**.

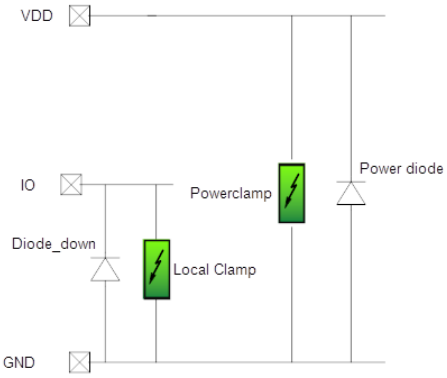

Figure 12: Example ESD protection concept for VDD/IO.

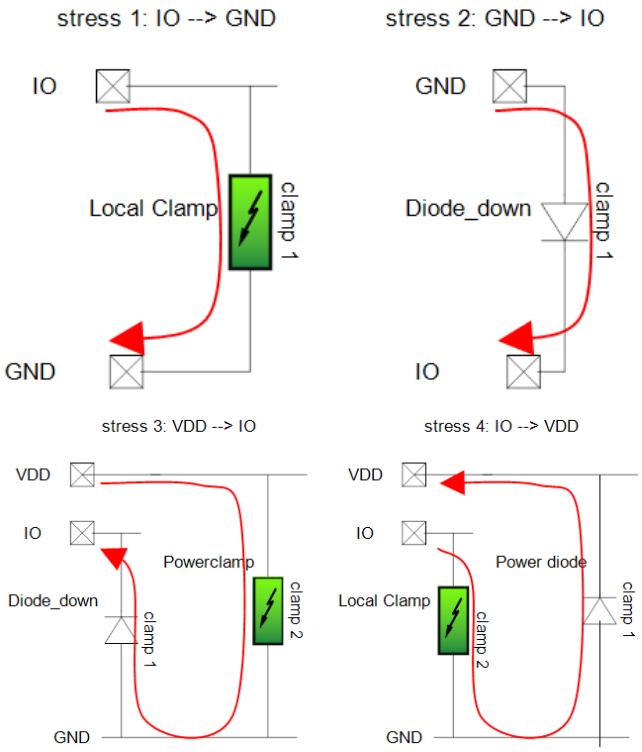

Figure 13: EOS/ESD current paths for the different stress cases.

For the stress from VDD to IO the current path consists of 2 elements: the diode from GND to IO and the power clamp (3.3V GG-SCR [5]).

$$W_{min,1} = \frac{1}{2}.\left(\frac{(V_{EOS} - V_{h,1} - V_{h,2}).1000}{{I_{max,1}}'} - R'_{on,1}.-R'_{on,2}.\frac{{I_{max,2}}'}{{I_{max,1}}'}\right)$$

$$W_{min,2} = \frac{1}{2}.\left(\frac{(V_{EOS} - V_{h,1} - V_{h,2}).1000}{{I_{max,2}}'} - R'_{on,2}.-R'_{on,1}.\frac{{I_{max,1}}'}{{I_{max,2}}'}\right)$$

The parameters are summarized:

$W_{min,1}$: *minimum width for the diode down*
$W_{min,2}$: *minimum width for the power clamp*
V_{EOS} : $17\ V$
$V_{h,1}$: $1.1\ V$
$V_{h,2}$: $4\ V$
$I'_{max,1}$: $17.25\ mA/um$
$I'_{max,2}$: $15.26\ mA/um$
$R'_{on,1}$: $55.12\ Ohm.um$
$R'_{on,2}$: $129\ Ohm.um$

This leads to a minimum width (total perimeter across multiple fingers) for the diode down of 260.31um and for the SCR based power clamp of 294.25 um.

Conclusion

With an adequate strategy the EOS performance of a product can be extended to the limits of the process. Main part in this strategy is an ESD/EOS characterization, correlation with Long TLP and finally the extraction of the parameters needed for a successful calculation. With this strategy EOS protection, up to 19V can be achieved in a 0.13um/65nm process.

References

[1] IEC 61000-4-5, Electromagnetic compatibility (EMC)
- Part 4-5: Testing and measurement techniques – Surge immunity test

[2] Jae-Hyung Kim, "A consideration on the Electrical Overstress(EOS) failure mechanism in the interconnection system of liquid crystal display(LCD) panel", IEMTC 2010

[3] http://www.kasteng.com/~ftp_kasteng/eng_board/pro_view.php?STR_CATE_SEQ=31&STR_CATE_LEVEL=1&TName=EngBoard_Product_product&TSeq=3

[4] Wunsch, D.C., and Bell, R.R., "Determination of threshold failure levels of semiconductor diodes and transistors due to pulse voltages", IEEE Trans. Nucl. Science, Vol. NS-15, 1968, pp.244-259

[5] Christian Russ et al., "GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep SubMicron CMOS Processes", EOS/ESD 2001.

About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

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Version

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Sofics BVBA
Groendreef 31
B-9880 Aalter, Belgium
(tel) +32-9-21-68-333
(fax) +32-9-37-46-846
bd@sofics.com
RPR 0472.687.037