Local I/O ESD protection for 28Gbps to 112Gbps SerDes interfaces in advanced CMOS and FinFET technology

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Abstract: Semiconductor companies are developing ever faster wireless, wired and optical interfaces to satisfy the need for higher data throughputs. They rely on BiCMOS, advanced CMOS and FinFET nodes with ESD-sensitive circuits. However, the parasitic capacitance of the traditional ESD solutions limits the signal frequency. This paper demonstrates small area and low-cap Analog I/Os used in TSMC 28nm CMOS and TSMC 16nm, 12nm, 7nm FinFET technologies for high speed SerDes (28Gbps to 112Gbps) circuits. Parasitic capacitance of the ESD solutions is reduced below 100fF and for some silicon photonics applications even below 20fF.

I. Introduction

In the connected world today, the demand to transfer data is growing every day. People increasingly consume streaming video content, at home and on the road. The increased bandwidth is needed on every level, from smartphones, PCs, at data centers and across long distance connections. This demand pushes the semiconductor industry to develop faster communication solutions for wireless, optical and wired interfaces. A few years ago, the speed limit was in the order of 10 Gbps. Recent circuits run at 56Gbps or even 112Gbps.

For such high-speed communication interfaces chip designers need to limit the parasitic capacitance of the on-chip ESD protection clamps connected to the interfaces. Because the traditional ESD approach is not good enough, they need special analog I/O circuits. This paper demonstrates silicon proven ESD solutions for TSMC 28nm CMOS and TSMC 16nm, 12nm and 7nm FinFET technology. Parasitic capacitance of the ESD solutions is reduced below 100fF and for some silicon photonics applications even below 20fF.

II. Traditional ESD approach

The traditional ESD approach for analog I/O pads is shown in Figure 1. It consists of a diode from Vss to the I/O pad, a second diode from I/O pad to Vdd and a power/rail clamp between Vdd and Vss [1-5].

IC designers like it because the 2 diodes are easy to implement, have a small silicon footprint and have reasonably low parasitic capacitance.

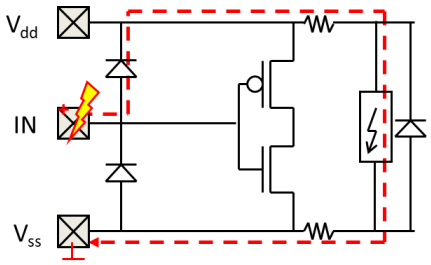

Figure 1: The traditional ESD approach for many I/O pads: A diode from Vss to I/O and another diode from I/O to Vdd. A power clamp is required for half of the stress combinations.

For sensitive nodes, IC designers add an isolation resistance from I/O to the circuit to increase the ESD design window. If the functional circuit cannot handle any ESD current, a secondary clamp is added behind the isolation resistance (Figure 2).

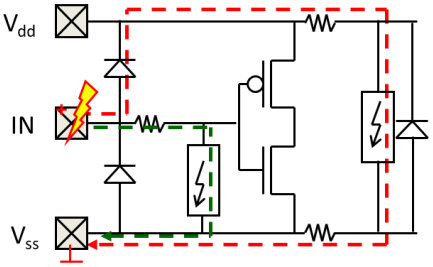

Figure 2: Sometimes IC designers add a resistance between I/O pad and the circuit and implement a small secondary clamp just before the sensitive circuit. This can increase the ESD design window.

There are several issues with this simple approach, specifically for high speed interfaces:

(1) The isolation resistance severely impacts behaviour at high speeds and adds noise.

(2) The ESD diodes may introduce excessive parasitic capacitance between the signal pad and the power lines.

(3) Some interfaces cannot tolerate a diode from I/O pad to Vdd due to matching, due to noise coupling between pad and Vdd or because the signal voltage can be higher than the reference Vdd voltage.

(4) For sensitive nodes the total voltage drop over the intended ESD current path can be above the failure voltage of the functional circuit [5].

A simple way to reduce the capacitance (issue 2) and increase the voltage tolerance (issue 3) is to use 2 or more diodes in series. However, this leads to a higher voltage drop during ESD stress, deteriorating issue 4. An alternative with a novel dual bipolar concept was presented in 2017 [6-7].

This paper discusses projects where IC designers replaced the traditional dual diode ESD approach with a local protection clamp concept, simplified in Figure 3. If the functional operation cannot tolerate a diode from 'IN' to Vdd that diode can be removed. That is typical for fail-safe, Hot-swap, open-drain outputs, cold-spare inputs or overvoltage tolerant interfaces [8].

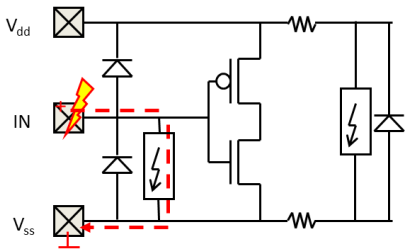

Figure 3: Simplified circuit schematic with a local clamp ESD protection approach. The diode between IN and Vdd can be removed if needed for the functional operation. In some cases, another clamp is added between Vdd and 'IN'.

The local clamp approach introduces a lot of benefits:

(1) Reduced dependence on bus resistance

(2) Strongly reduced voltage drop under ESD conditions without the need for an isolation resistance, perfect for sensitive nodes.

(3) Different options to reduce the parasitic capacitance (see case studies below)

(4) Can be optimized for each I/O pad separately. E.g. some pads may need higher ESD robustness or cannot tolerate a diode between I/O and Vdd.

III. SerDes protection case studies

Several local clamp approaches with (ultra) low parasitic capacitance are summarized in case studies below for the protection of high-speed SerDes interfaces in 28nm CMOS to 7nm FinFET. Different types of SCR-based local clamps are used in the case studies (Figure 4). The Diode triggered SCR and ESD-on-SCR were previously used to protect wireless LNA interfaces [9].

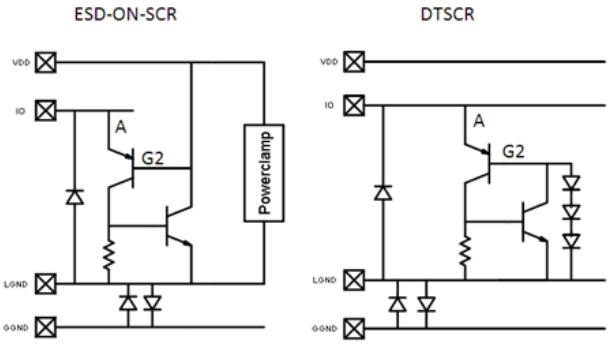

Figure 4: Two ESD protection clamps used in the case studies. The Sofics ESD-on-SCR is triggered as soon as the IO level raises 1 diode drop (Anode-G2) above the Vdd voltage. The Sofics DTSCR is turned on once the AnodeG2 and trigger diodes are forward biased.

1. FPGA 28nm, 28Gbps SerDes

For a range of advanced FPGA products in TSMC 28nm the customer required custom ESD protection cells. For the 28Gbps SerDes interface the following specifications were required.

- Parasitic capacitance well below 100fF.
- ESD rating: > 1kV HBM; >250V CDM

A scaled-down version of the Sofics DTSCR clamp was selected as the local protection for the Tx and Rx interfaces. A secondary local CDM clamp was added behind the isolation resistance to protect the thin gate oxide in the Rx case (Figure 5). The parasitic capacitance of the DTSCR, the reverse diode and the metal connections together was kept below 80fF.

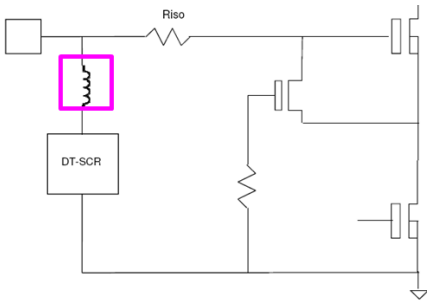

Figure 5: Schematic representation of the 28Gbps SerDes Rx (input) stage, showing the DTSCR local clamp and secondary protection stage for enhanced CDM protection.

In order to meet the S11 – Return loss specification an inductor was added in series with the DTSCR (Figure 6). All specifications were met including CDM. The FPGA part reached more than 300V with a 4.5A peak current. All the analysis results have been presented at the IEW 2011 event [10].

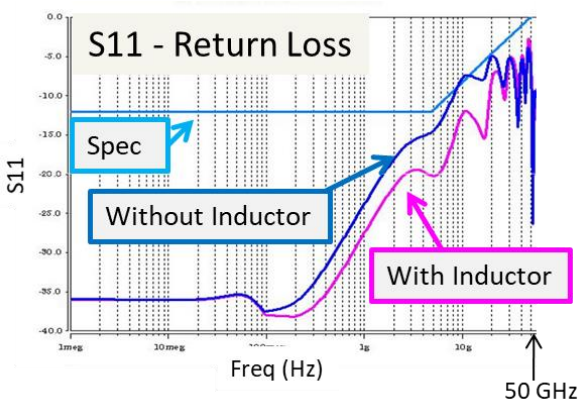

Figure 6: To meet the S11 specification an inductor was added in series with the DTSCR. The coil reduces the S11 peaks at 10 GHz and 20 GHz.

2. Generic SerDes 16nm, 28Gbps

A high speed (data center) communication chip with a 28 Gbps SerDes, produced in 16nm required a custom ESD protection approach.

The local ESD clamp must adhere to these requirements.

- Protection of sensitive thin oxide, 0.8V core transistors with failure voltage during ESD stress below 3.3V
- Low leakage ESD clamp, below 10nA at high temperature (125°C)
- Small silicon footprint to enable multiple channels on the same communication chip
- No resistance allowed
- >2kV HBM
- Maximum ESD junction capacitance of 100fF

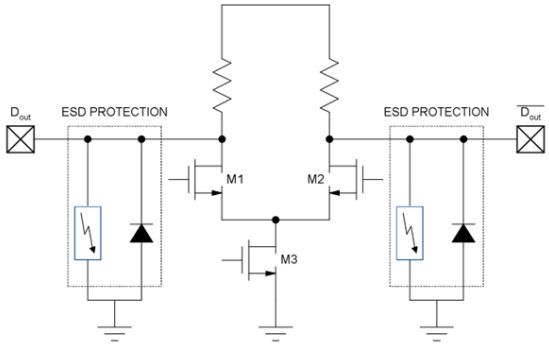

Figure 7: Schematic representation of the protection concept for the differential pair of the Tx interface. On both paths of the differential pair a local clamp and parallel reverse diode is added.

Based on an extensive test chip analysis on TSMC 16nm FinFET technology the ESD-on-SCR concept was selected as the local clamp device. The TLP data is shown on Figure 8. In an area of less than 1.000 um², it protects thin-oxide devices above 2 Ampere. Leakage at high temperature is about 1nA.

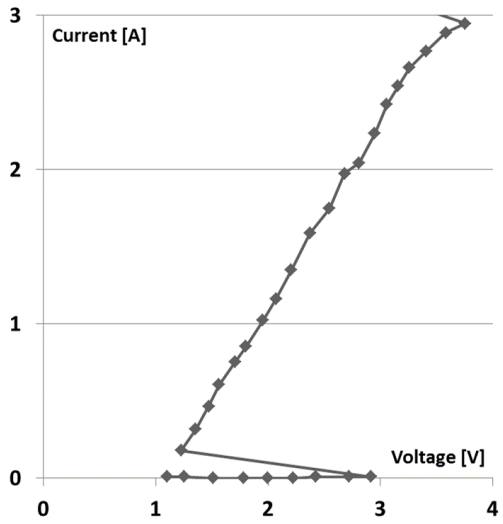

Figure 8: TLP measurement of the ESD-on-SCR device used as local clamp device. The device reaches more than 2A before the failure voltage of thin oxide transistor is reached.

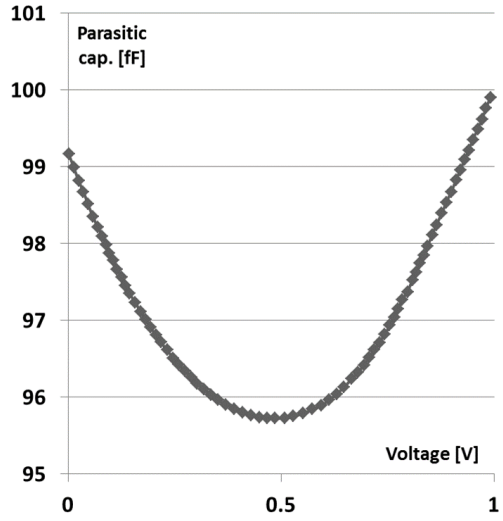

Figure 9: Capacitance simulation (Spice) for the ESD-on-SCR. The capacitance remains below the target level of 100fF across the entire voltage range of the pad.

To ensure that the ESD protection clamp does not influence the functional operation of the high speed SerDes the parasitic junction capacitance is simulated across pad voltage, shown in Figure 9. An equivalent model based on diode junctions was used to simulate the capacitive loading of the ESD cell.

3. Silicon Photonics 28nm, 28Gbps

Several companies working on new optical transceivers contacted us for support. For the regular, low speed I/Os (1.8V) the Analog/digital I/O library provided by the foundry was sufficient. The ESD requirement for those pads was 2kV HBM.

On the other hand, the analog I/Os in the foundry library introduced too much parasitic capacitance for the high-speed interfaces. The designers requested a reduced total capacitance of the ESD device below 15fF.

The 28nm CMOS SoC was co-packaged with a silicon photonic device in a shared/hybrid integrated package (Figure 10). Because this flip-chip assembly is performed in an ESD controlled environment the ESD protection level could be reduced to 200V HBM without effect on the yield.

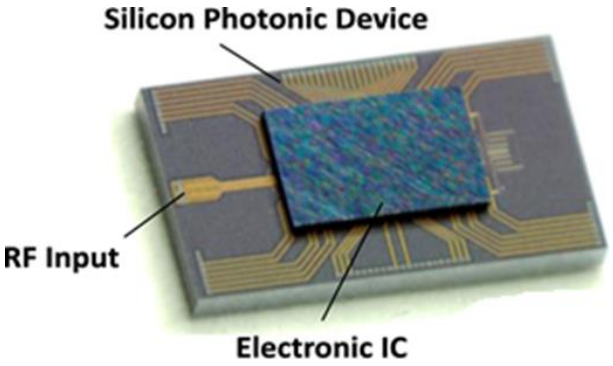

Figure 10: (Example) Packaging of an electronic IC (driver) on a silicon photonic device using a flip-chip bonding process (© IOP 2016 [11]).

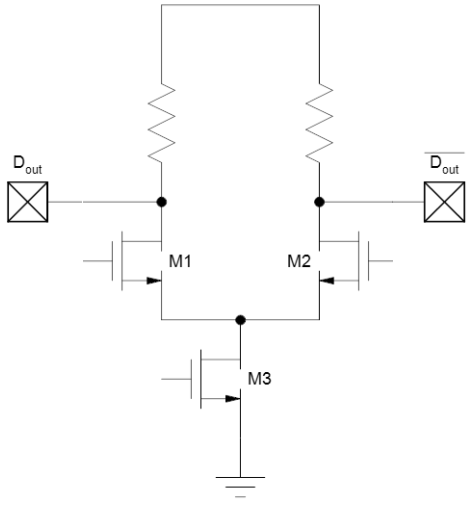

Figure 11: Simplified Tx/output circuit used in the Silicon Photonics SerDes interface.

The 28Gbps interfaces used a differential pair concept as shown in Figure 11. The 1V functional circuit is created using 0.9V core transistors to ensure the switching speed can be reached. However, these transistors reduced the available ESD design window for the Rx, Tx signals to 4V.

Other requirements for the ESD protection included low leakage operation and small silicon footprint.

The ESD protection design consists a full local protection clamp concept, shown in Figure 12. A 1V power clamp was integrated to ensure all the stress cases could be handled locally at the interface and bus resistance is taken out of the equation. The entire clamp structure was isolated from the substrate to reduce noise from the substrate that could come from digital circuits further on the die.

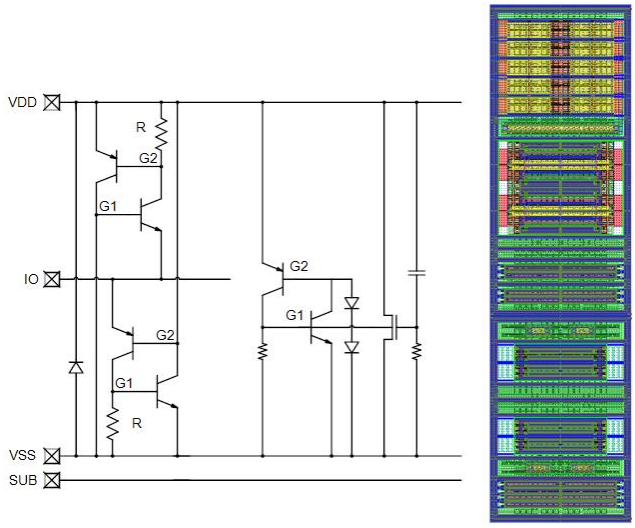

Figure 12: Schematic view (left) of the full local protection approach for the Rx and Tx nodes of the SerDes circuit. It is based on ESD-on-SCR devices. An SCR based 1V power clamp is integrated in the same layout (right). The total area for ESD is 683.75 um².

The total parasitic capacitance at the I/O pad consists of different aspects. The junction capacitance can be easily derived from the foundry provided Spice models for diodes. The metal connections of the local ESD clamps can add a significant amount of capacitance. The parasitic metal capacitance can be derived from PEX extraction. Reducing the width of the metal connections can reduce the capacitance but will also reduce the robustness of the line. The minimal metal width is derived from ESD stress performed at different metal stripes on our ESD test chip.

The metal dummies are included in the PEX extraction when customers request ESD protection with ultra-low capacitance (well below 100fF).

Through an iterative process (layout, PEX extraction) the total parasitic capacitance of the ESD clamp was reduced to less than 15fF. The presentation will show the different steps in this procedure. The plot below (Figure 13) shows the capacitance value as function of the bias voltage at the pad.

The parasitic capacitance to ground must be reduced to prevent the high-frequency signal is shunted to ground.

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C}$$

Equation 1: The capacitor reactance Xc (in Ohm) inversely proportional to the signal frequency (f) and capacitance (C)

For high frequency (>50 Ghz), the parasitic capacitance behaves as a resistance to ground. This impedance must be high enough. A 15 fF capacitance behaves as a ~200 ohm resistance at 50 GHz.

In the iterative process to reduce the contribution of the parasitic capacitance from the metal connections a number of rules are used

- Remove unnecessary via connections
- Reduce Metal 1 as much as possible, keep it on top of the connected diffusion only. Prevent running Metal 1 across junctions.
- Work vertically (up)

Even when reduced, 42% of parasitic capacitance can be linked to the metal connections.

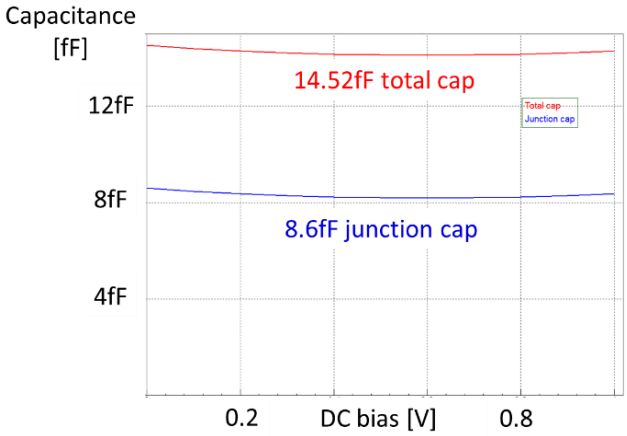

Figure 13: Parasitic capacitance (total and junction only) across the I/O voltage.

Using a transient Spice simulation of HBM ESD stress, the local clamp approach of Figure 12 is compared with 2 other concepts.

- Concept 1: Proposed local clamp
- Concept 2: Foundry provided I/O pads (dual diode and foundry proposed core power clamp)
- Concept 3: Dual diode combined with Sofics 1V core protection clamp

From Figure 14 it is clear that concept 2 and 3 create a voltage drop well above the failure voltage (4V) of the sensitive circuit based on thin oxide transistors [12].

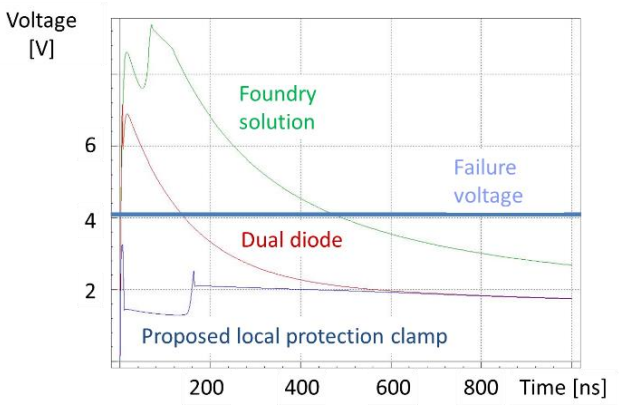

Figure 14: Transient Spice simulation under HBM stress. 3 concepts are compared to verify that the voltage drop at the sensitive node during ESD stress remains below the maximum level of 4V. Only the proposed local clamp can shunt the ESD stress below 4V. This comparison was done using 1kV HBM stress with ESD devices scaled to 1kV robustness. The snapback of the SCR local clamp was simulated using a combined NPN/PNP model.

4. Silicon Photonics 7nm FinFET

To further increase the bandwidth of the optical interconnects (beyond 56 Gbps) our customer moved to TSMC 7nm FinFET technology.

The proposed solution is similar to Figure 12. Two versions of the ESD protection are created, one with parasitic capacitance of 50fF and a smaller version with less than 15fF. During the paper presentation these case studies will be included.

Initial measurements on TSMC's 7nm FinFET process demonstrate that the ESD-on-SCR local clamp performs as expected (Figure 15).

In 7nm technology, the failure voltage of core transistors (gate to source and drain to source) is about 3V. Fortunately, in many SerDes applications there is a bit more margin due to other transistors connected in series (Figure 11). Failure voltage of those circuits is around 4-5V depending on the circuit concept.

The 7nm ESD clamps have been integrated into 2 designs for high speed interfaces. These product samples were not available at the time of paper writing so CDM data is not available yet.

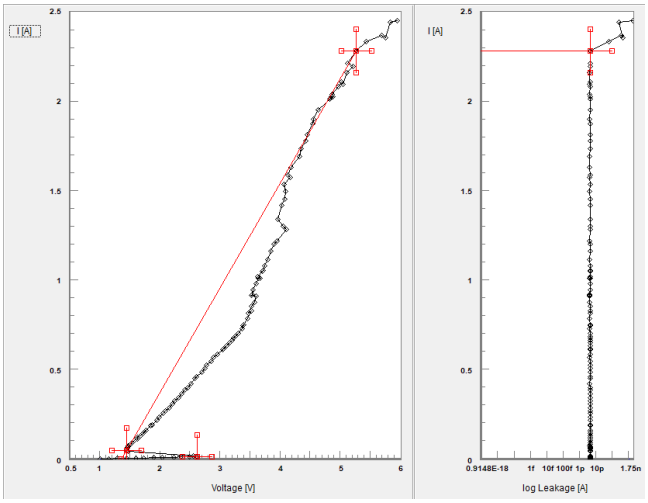

Figure 15: TLP analysis of the ESD-on-SCR concept on TSMC 7nm technology. It protects sensitive core transistors. This reference device for 2kV HBM performance is scaled down for a 15fF and 50fF version for the protection of high-speed SerDes.

Conclusions

The traditional 'dual diode' ESD protection concept for analog I/O pads runs into problems for the protection of high speed SerDes interfaces in advanced CMOS and FinFET nodes. The total voltage drop over diode, bus resistance and power clamp easily exceeds the failure voltage of core transistors. Moreover, the 'diode up' adds limitations.

This work showed several case studies where the dual diode concept was replaced with local ESD protection clamps in the I/O pad based on proprietary Diode triggered and ESD-on-SCR devices. The local clamp reduces the dependence of the bus resistance, reduces the clamping voltage and allows to optimize every analog I/O separately. Moreover, the cases show that it is possible to create ESD protection with a very low parasitic capacitance and small silicon footprint.

The data is based on dedicated ESD test chips on advanced CMOS and FinFET nodes. The analog I/Os in this work are used by more than 20 companies for the protection of high-speed SerDes interfaces in 28nm CMOS, 16nm/12nm and 7nm FinFET technology.

References

[1] M.K. Radhakrishnan et al., "ESD Reliablity Issues in RF CMOS Circuits", 2001

[2] Feng K et al., "A comparison study of ESD protection for RFICs: performance versus parasitic", 2000 IEEE RFI

[3] R.M.D.A Velghe et al, "Diode Network Used as ESD Protection in RF Applications", EOS/ESD Symposium, 2001

[4] K. Bhatia et al., "Layout Guidelines for Optimized ESD Protection Diodes", EOS/ESD Symposium, 2007

[5] G. Boselli et al., "Analysis of ESD Protection Components in 65nm CMOS: Scaling Perspective and Impact on ESD Design Window, EOS/ESD Symposium, 2005

[6] I. Backers et al, "Low Capacitive Dual Bipolar ESD protection", EOS/ESD Symposium 2017.

[7] US 8,283,698 Electrostatic Discharge Protection

[8] B. Keppens et al, "ESD relevant issues and solutions for overvoltage tolerant, hot swap, open drain, and failsafe interfaces", Taiwan ESD and Reliability conference 2011

[9] B. Keppens et al, "SCR based on-chip ESD protection for LNA's in 90nm and 40nm CMOS", Taiwan ESD and Reliability Conference 2010

[10] C. Chu, "High Speed Transceiver ESD protection", International ESD workshop 2011, lake Tahoe.

[11] Roadmap on silicon photonics, David Thomson e.a., Journal of Optics, volume 18, nr 7, 2016

[12] J. Van der Borght et al, "Protecting Photonics Where Diodes Fail: ESD Protection for 28 to 56 Gbps Interfaces in 28nm CMOS", International ESD Workshop 2018, Belgium