On-chip ESD protection for 16nm FF+

ON-CHIP PROTECTION

for electrostatic discharge (ESD) and electrical overstress (EOS)

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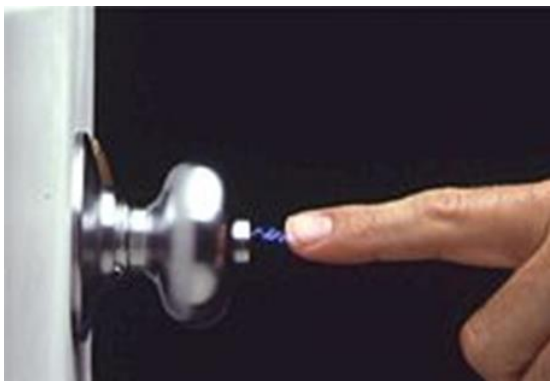
Despite the rising cost for IC development, EDA tools and mask sets, many fabless design companies continue to use the most advanced CMOS technology. Benefits like lower power dissipation, increased gate density, higher speed and lower manufacturing cost per gate compensate the higher design cost.

Due to the use of sensitive elements (such as ultra-thin oxide transistors, FinFET transistors, ultra-shallow junctions, narrow and thin metal layers), increased complexity through multiple voltage domains and the mix of IP blocks from various vendors, a comprehensive ESD (Electrostatic Discharge) protection strategy becomes more important at every node and certainly for FinFET technology.

This document shows ESD relevant analysis of 16nm FF+ technology and provides information about state-of-the-art ESD clamps that provide competitive advantage due to ultra-low leakage, reduced silicon footprint and low parasitic capacitance. With the right ESD approach advanced applications (high speed SerDes, IoT, wireless, computing) are within reach.

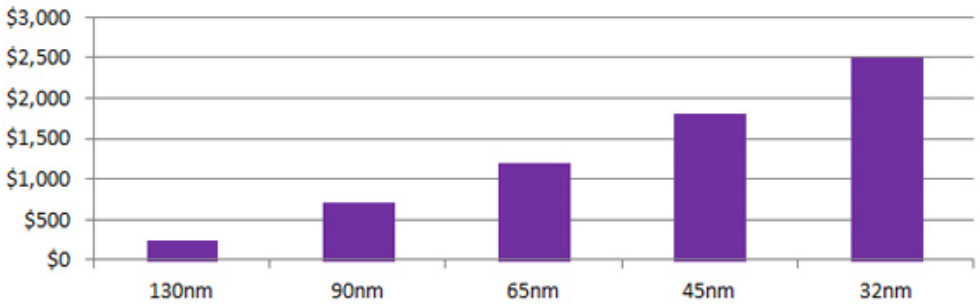
1. Introduction – on-chip ESD protection?

Electrostatic Discharge (ESD) remains an important reliability issue for semiconductor companies. ESD events can happen during several stages in the development, assembly and actual use of the ICs.



Because the mask cost is very high for the most advanced technologies, IC design firms do not want to risk updating 1 or more masks after an ESD failure is found. Therefore they use silicon proven IP.

Approximate Mask Cost ($k) per node

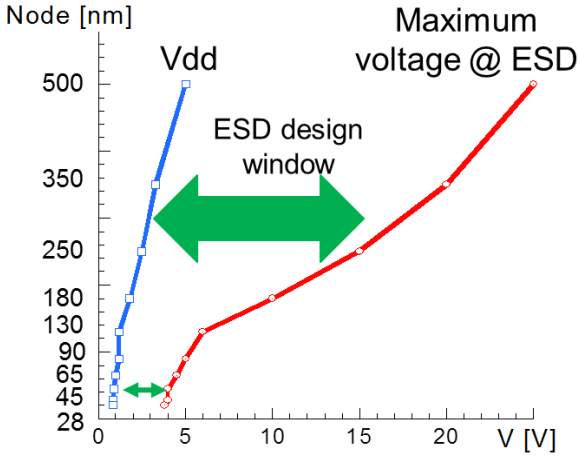


2. ESD relevant analysis of FinFET technology

Sofics recently had the opportunity to characterize the TSMC 16nm FF+ technology through cooperation with one of its customers. We analyzed the technology related to ESD. The following subsections summarize the challenges for on-chip ESD protection.

Advanced circuits fail easily during ESD stress

The maximum allowed voltage on core circuits continues to drop. This is summarized in the graph showing the ESD design window reduction for more advanced technologies.



The maximum voltage during ESD conditions across sensitive circuits based on core devices is around 3V. Simple gate oxide, junction or core victim circuits were used to extract the maximum allowed voltage.

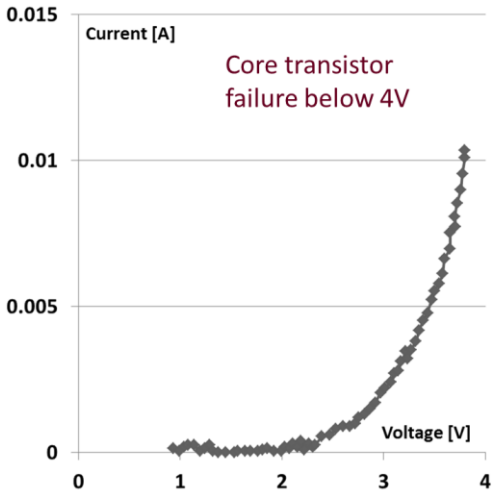
16nm FF+ 0.8V	Gate oxide	Junction	Core
Vmax	3.3 V	3 V	3V

Traditional ESD solutions run out of steam

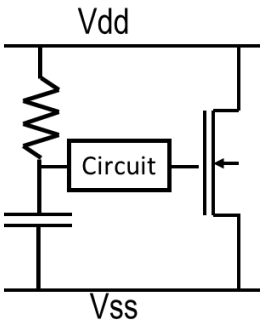
In mature and mainstream technology nodes ESD protection is rather straightforward. Several options exist for core and local protection.

We analyzed the NMOS and PMOS devices in 16nm FF+. **Both for core and I/O domains the MOS transistors do not survive snapback.** This means that it is not possible to use those devices for power or local protection. In the I/O domain (1.8V transistors) we noticed junction failure around 4.5V without snapback operation. It is thus not possible to create self-protective output drivers.

In the 1.8V I/O domain it is possible to restore the snapback operation by adding silicide block combined with an extended drain-to-gate contact spacing.



Many IC designers rely on so-called **BIGfet circuits or rail clamps** where a large NMOS is actively biased only during ESD events. We designed a MOS transistor with several fingers and a total perimeter of 2800um. Several detection and gate-bias-circuits were compared.



Thanks to the transistor scaling the total silicon footprint is reasonably small: around 1800um². **The main problem with this approach is the excessive leakage current**. At 0.8V and 85°C, the leakage is higher than 0.5uA.

We also analyzed **Nwell and Pwell diodes**. Diodes in advanced technology show a reduced ESD performance and higher resistivity compared to mainstream technology. The achievable level in 16nm is about the same as in 28nm CMOS.

- 35mA/um in 65nm
- 25mA/um in 40nm
- 20mA/um in 28nm and 16nm

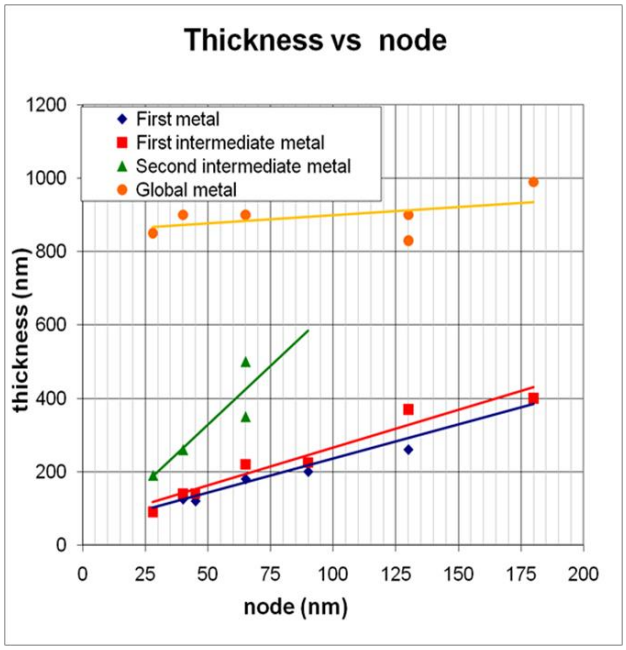
This means that diodes must be drawn with a larger perimeter compared to 65nm to compensate for the reduced performance and higher resistivity. Unfortunately this means that the capacitive loading also increases. A rail clamp approach is not feasible for 0.8V interfaces because the voltage drop across the diode, bus resistance and power clamp more than exceeds the available ESD design window of 3V.

Though metallization constraints

Typical advanced CMOS nodes provide 2 or 3 distinct groups of metallization. The local metals are getting thinner at every new node to allow narrower transistor pitch. **The thickness has been reduced by a factor 4 compared to 180nm CMOS.** This means that the

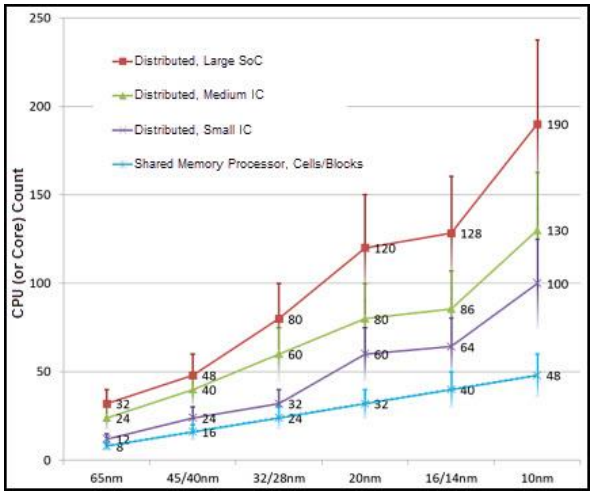
connections to the power bus are more difficult. Also the connections inside the ESD clamp need extra attention.

Fortunately, the top metal thickness remains roughly the same. So it is still possible to design an ESD robust power bus.



Increased design complexity

There is a significant increase in the number of design rules in FinFET technology. Several EDA vendors already pointed out that verifying FinFET-based circuits requires a computer system with several CPU-cores and a lot of DRAM memory[1]. Additional verifications are related to multi-pattern checks and fin-grid checks.



We also noticed a **strong increase in ESD design complexity**. Creating a custom ESD clamp layout for core protection required only a day in 28nm, but easily took about 2 weeks in 16nm technology.

[1] According to Mentor Graphics, 16nm design requires 40-100 CPU cores and 500Gb of DRAM memory

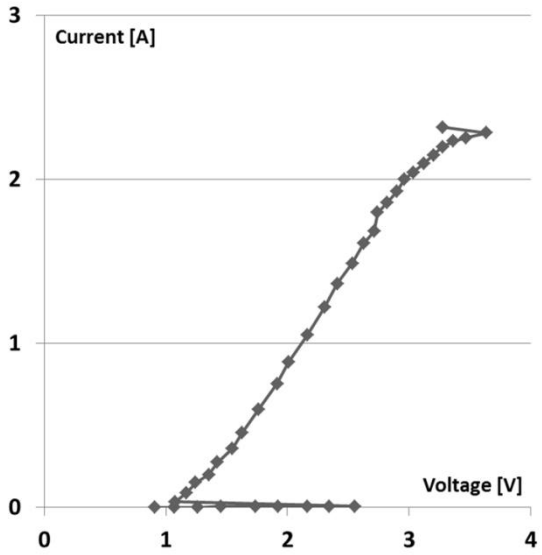
3. ESD clamp solutions in 16nm FinFET+

Sofics verified ESD solutions for different core (0.8V, 1.2V and 1.5V) and I/O domains (1.8V, 2.5V and 3.3V). Because we noticed many requests for 5V compatibility in 28nm and 40nm CMOS we have also included test structures for 5V.

ESD protection clamp for core domains

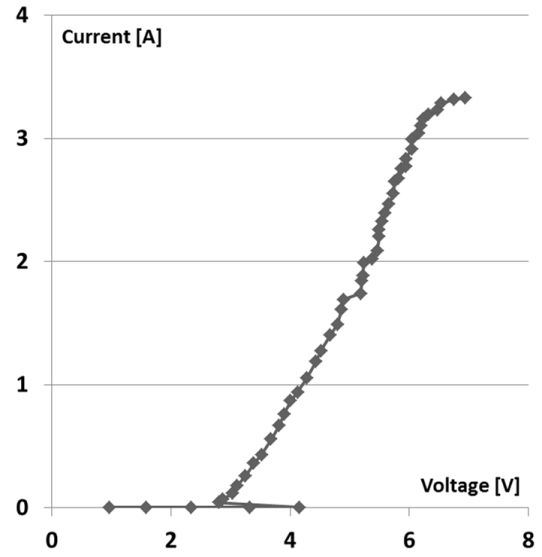
The core domain has an extremely narrow ESD design window so an efficient power protection clamp is required that shunts ESD below 3V.

The best verified solution consists of a Sofics proprietary SCR-based (Silicon Controlled Rectifier) clamp triggered with an RC based detection circuit. Within an area of 1000um² the clamp reached 2A of TLP current. The leakage remains below 10nA at 125°C. The clamping voltage, also checked at 125°C, is 0.9V, high enough to ensure there is no latch-up concern.



ESD protection for 1.8V I/O interfaces

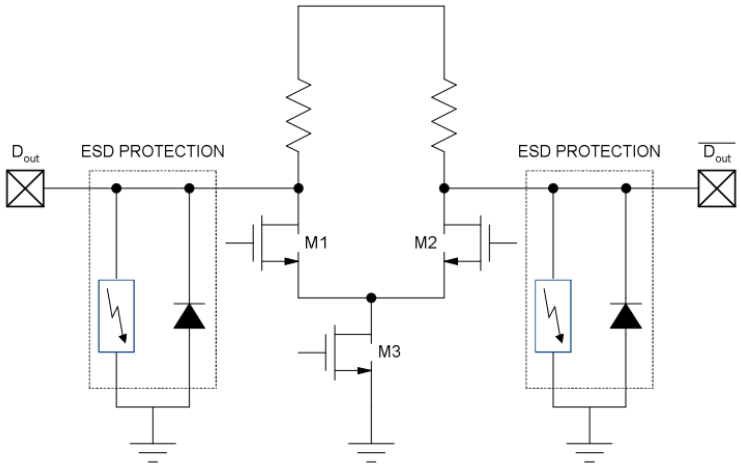
Because it is not possible to create self-protective output drivers, Sofics proposes to use a local protection device. We verified our patented Diode triggered Silicon Controlled Rectifier (DT-SCR). Within an area of less than 1000m² the clamp reached more than 2A of TLP current.



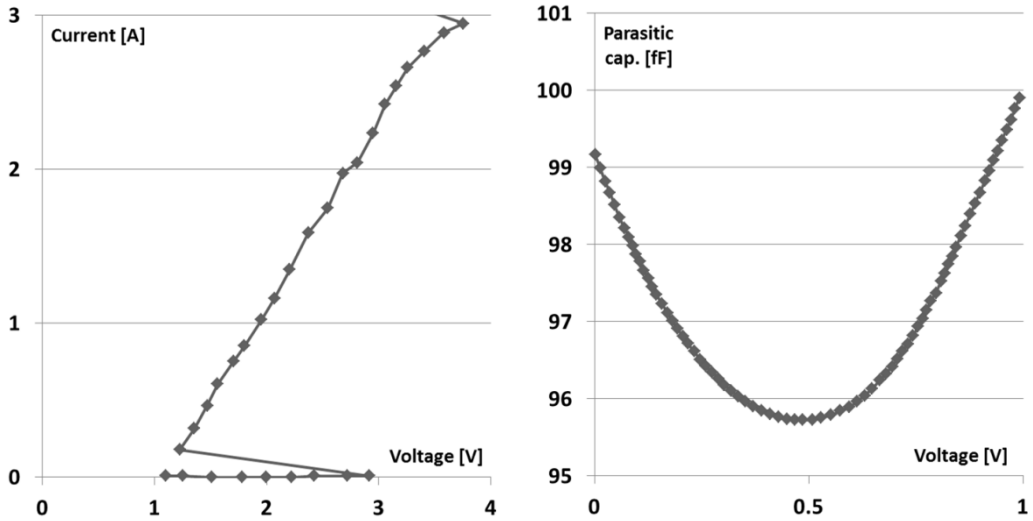
ESD protection for high speed interfaces

Sometimes it is required to use thin oxide, core transistors for high speed interfaces. E.g. designers that want to create a 30Gbps SerDes interfaces will need to use the 0.8V devices. Of course these devices are extremely sensitive and need adequate protection during ESD stress.

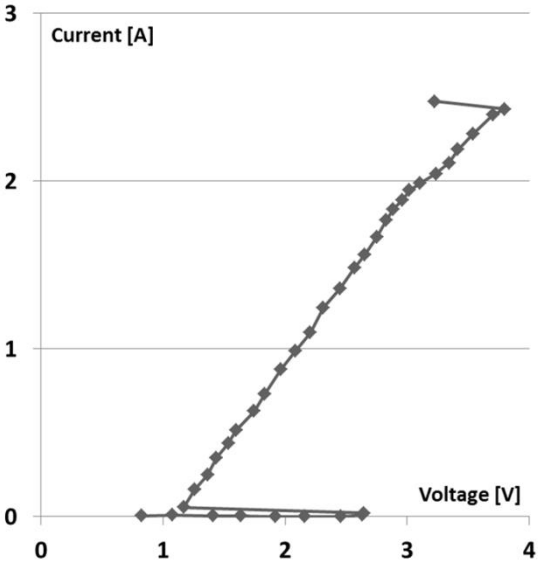
- Due to the high speed it is not possible to include a resistor in the pad to use a so-called secondary protection concept.
- In mature processes it was possible to create self-protective drivers but as shown in part 2, the core devices do not survive ESD stress.
- The other typical approach, dual diode and rail clamp, is not possible because the ESD design window is only 3V. The voltage across diode, bus and power clamp easily exceeds that.
- A feasible solution is to use a local protection clamp between pad and ground like shown below for a differential HDMI TMDS output.



A first silicon verified clamp uses the Sofics' ESD-on-SCR device. Within an area of less than 1000um² more than 2A TLP is reached. The leakage is about 1nA at 125°C! When a full local protection concept is used the total capacitive loading is about 100fF. This allows to create 30Gbps interfaces.



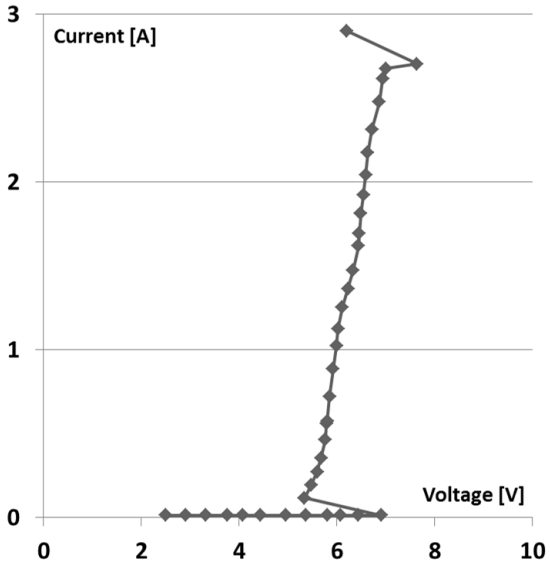
Another example uses the Sofics 'Always-on-SCR' concept with similar results.



5V interfaces

We recently received a lot of requests for 5V compatible interfaces in 40nm and 28nm CMOS. There are several reasons for such 5V pins like legacy interface compatibility, battery supply, sensor interfaces, hot swap or fail safe interfaces. A simple dual diode based protection with 1.8 or 3.3V supply reference is not possible in those cases.

Therefore we included a number of 5V capable concepts on the 16nm FinFET+ tape out. The example below is based on our N-SMOS concept and reaches 2.4A of TLP current. It is latch-up safe with a DC holding voltage above 5.5V. The leakage is about 30nA at 5V at 25°C.

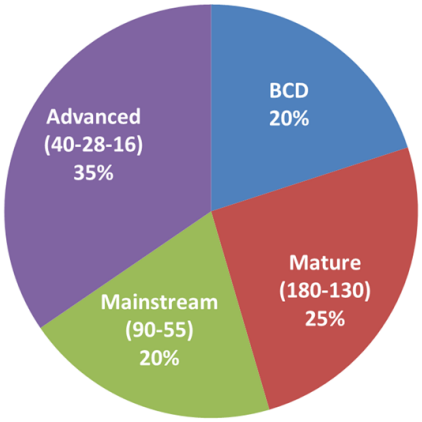


4. Sofics

Sofics joined the Design Center Alliance of TSMC already in 2008 based on positive feedback from several of TSMC's customers. In 2010 Sofics joined the IP alliance partnership when TSMC licensed the Sofics PowerQubic ESD clamps for 0.25um BCD technology.

Sofics currently supports more than 40 TSMC customers, across many different nodes, applications.

Percentage of projects on TSMC technology nodes



Node	Voltage domains
350nm HV	3.3V 15V
250nm BCD, gen. I and II	12V 24V 40V 60V
180nm BCD, gen. I and II	18V 24V 32V 40V 60V
180nm CMOS	1.8V 3.3V 5V
130nm CMOS	1.0V 1.2V 3.3V 5V 7V
90nm CMOS	1.2V 1.8V 3.3V
65nm CMOS	1.0V 1.2V 1.8V 2.5V 3.3V 5V
40nm CMOS	0.9V 1.2V 1.8V 3.3V 5V
28nm CMOS	0.85V 0.9V 1.8V 3.3V 5V 5.5V 12V
16nm FF+	0.8V 1.2V 1.5V 1.8V 2.5V 3.3V 5V

5. Conclusion

On-chip ESD protection of 16nm FinFET circuits is not easy due to the sensitive transistors and the increased design complexity. Many of the traditional ESD solutions are no longer suitable.

Sofics has silicon proven ESD clamp solutions for all the different voltage domains

- Core protection below 3V (narrow design window)
- Several options for interface protection even for 0.8V I/O's
- Competitive advantages: Optimized silicon footprint, ultra-low leakage and low parasitic capacitance.
- Enable the most challenging applications like 30Gbps high speed interfaces

About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than 3000 IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off the-shelf or custom-crafted solutions to protect overvoltage I/Os, other nonstandard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Contact Sofics

Contact Sofics by email: 16nmreport@sofics.com

Scan the code below or browse to http://tiny.cc/16nmESD for updated information.

Notes

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