# On-chip ESD protection for Silicon Photonics

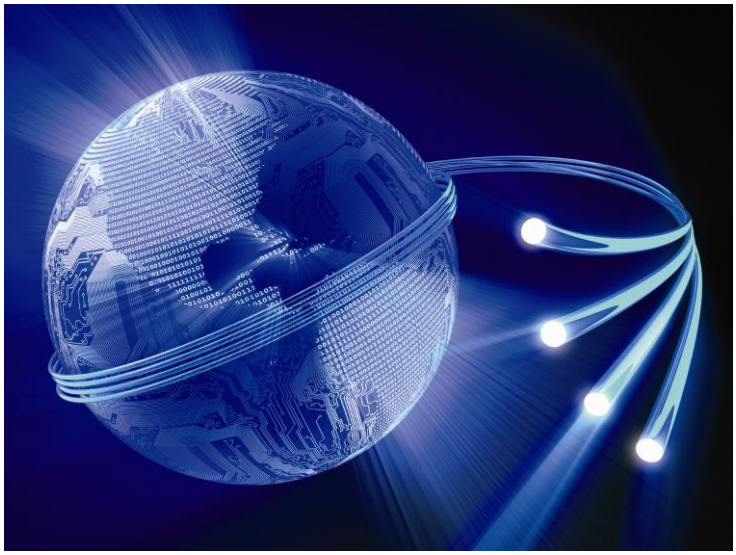
## ON-CHIP PROTECTION

*for electrostatic discharge (ESD) and electrical overstress (EOS)*

# On-chip ESD protection for Silicon Photonics

In the past, Fiber-optic communication was used only for long distance communication (50 km and beyond). Only a limited number of these high-end interface products were required worldwide. More recently, companies running large data centers (Facebook, Google, Amazon,...) like to replace the traditional cabling between server racks. The copper-based approach is considered a bottleneck for further improvements in data transfer capacity. Optical fiber can dramatically increase the bandwidth between servers and reduce complexity.

Thus, the optical interconnect suppliers now need to produce a large number of their products. To reduce the cost, they separate the optical parts (laser diodes, photo detectors) from the digital controller circuits. That allows to rely on advanced, standard CMOS technology for those controller circuits, enabling a cost-effective high-volume production. Both elements are combined within a single IC package using advanced packing techniques.



*Fiber-optic communication ensures that consumers worldwide can connect to all of the digital social and media services.*

The 25-56Gbps interfaces consist of SerDes-type circuits and are integrated into advanced CMOS technology like 28nm CMOS. To create such high-speed differential I/O circuits, designers utilize the thin oxide transistors. However, those transistors are very sensitive and can be easily damaged during transient events like electrostatic discharge (ESD).

Despite the fact that the sensitive pads are not connected outside of the package, they could still receive ESD stress during assembly. Therefore, adequate protection clamps need to be inserted at the bond pads. On the other hand, for signal integrity, it is important to limit the capacitance between the interface pads and the supply lines.

Sofics has worked with several companies developing these optical interconnect interfaces. Sofics developed ESD protection with parasitic capacitance below 15fF, ten times lower than the typical low-cap ESD protection devices in TSMC 28nm CMOS.

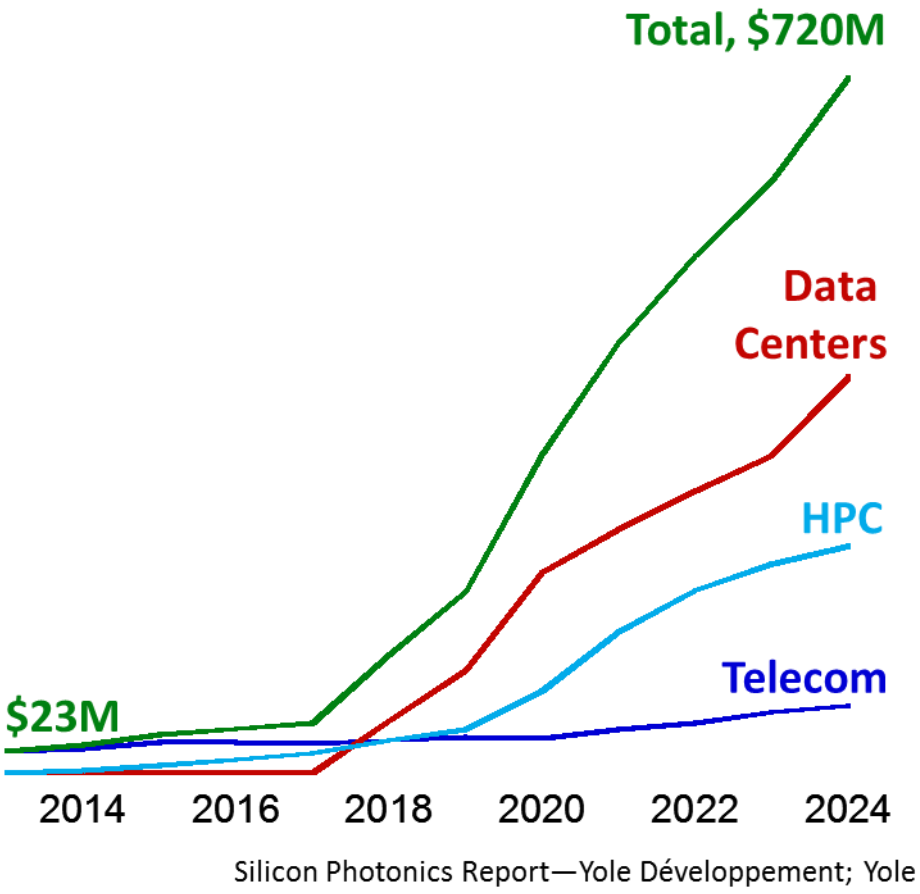
## 1. Optical communication

Already in 1880 Graham Bell used a beam of light to transmit sound with his Photophone. He called it his most important invention. In the 1970-ies the technology was developed, mainly for the telecommunications industry. The optical communication lines were used for long distance, high bandwidth connections. It has played a big role in the rise of the information age with immediate access to the worlds' data.

There are several benefits of optical communication

- Low loss communication. This allows to send information over a longer distance. The distance between amplifiers/repeaters is much higher.
- High bandwidth communication. A lot more data can be transferred over a single optical cable. So total weight is reduced.
- No cross talk from adjacent lines unlike electrical communication lines. This makes it immune to electromagnetic interference.
- Secure: it is difficult to tap the signals without disrupting them.

Several analysts predict a bright future for optical communication because there are several new application domains that require fast communication.




*Yole Développement estimates a strong increase in the use of optical communications. Specifically the communication within data centers and the High Performance Computing (HPC) sectors are expected to show the biggest growth.*

Telecommunication

In the past, Fiber-optic communication was used only for long distance communication (50 km and beyond). Only a small number of these high-end interface products were required worldwide. The suppliers could not distribute the development cost across a large volume of products. The circuits were manufactured with niche, expensive process technologies (III/V). Yole predicts a modest increase for this part.

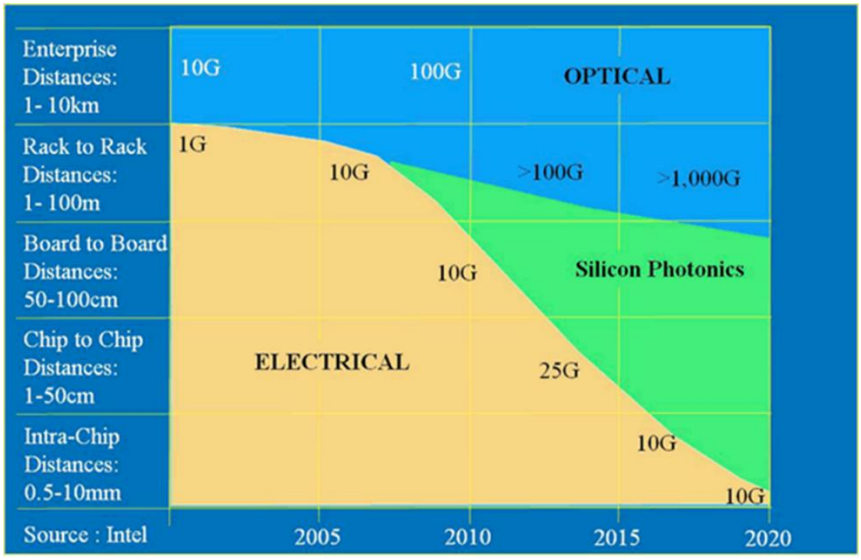
High Performance Computing (HPC)

Some applications are currently still marginal but are expected to grow quickly. To create high performance compute platforms developers use optical links between the different parts (distributed memory, distributed processing…) to speed up the data throughput. Yole predicts a strong increase in this market segment.

Data Centers

In the past optical communication is used between data centers. Today the communication between racks within data centers is being replaced by optical links. In the near future the communication between the different servers in a rack will also rely on optical communication to reduce power and increase the bandwidth.

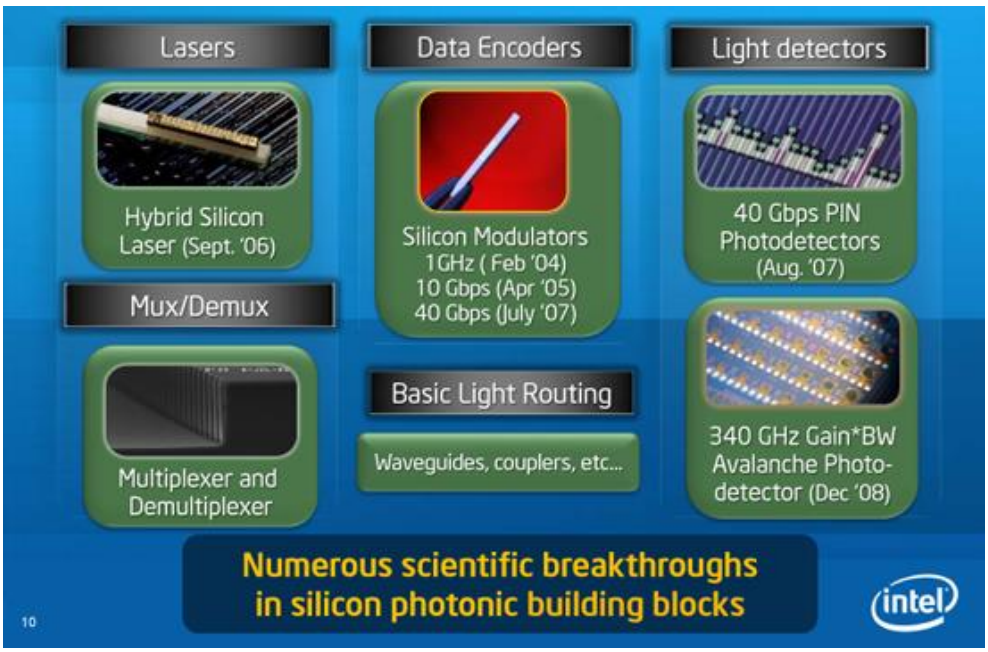
In total, Yole expects a 20-fold increase in the use of optical links over 10 years. To make this a reality new technology is required that can reduce the manufacturing and setup cost, reduce the power and increase the bandwidth. This technology is called Silicon Photonics.




*The engineers from the Intel groups working on optical communication summarized the potential for Silicon Photonics for different interface distances. The traditional optical communication will be used mainly for the long distances. Silicon photonics will replace the electrical communication for the shorter distances thanks to the combination of low power, low cost and high bandwidth opportunity.*

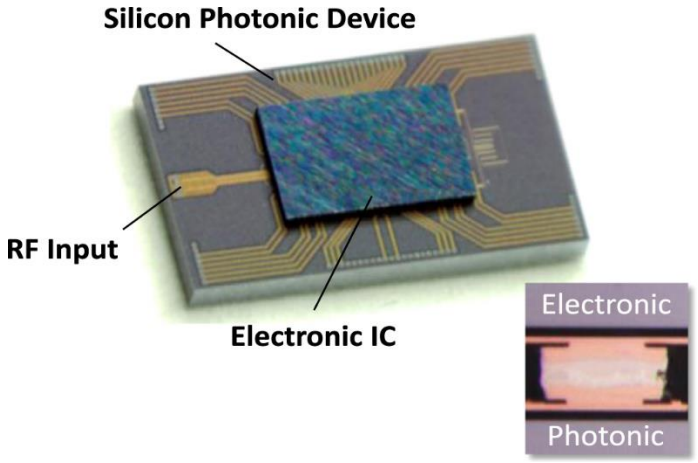
## 2. Integrated Silicon Photonics

There has been a lot of research and development to create low-cost, low power, high-bandwidth optical links that can be manufactured in great quantities. There were several breakthroughs in the last decade. Intel for instance showed an overview of the advancements where conventional CMOS processing steps can be used to create all kinds of optical components like WDM (Wavelength Division Multiplexers), lasers, detectors, waveguides…



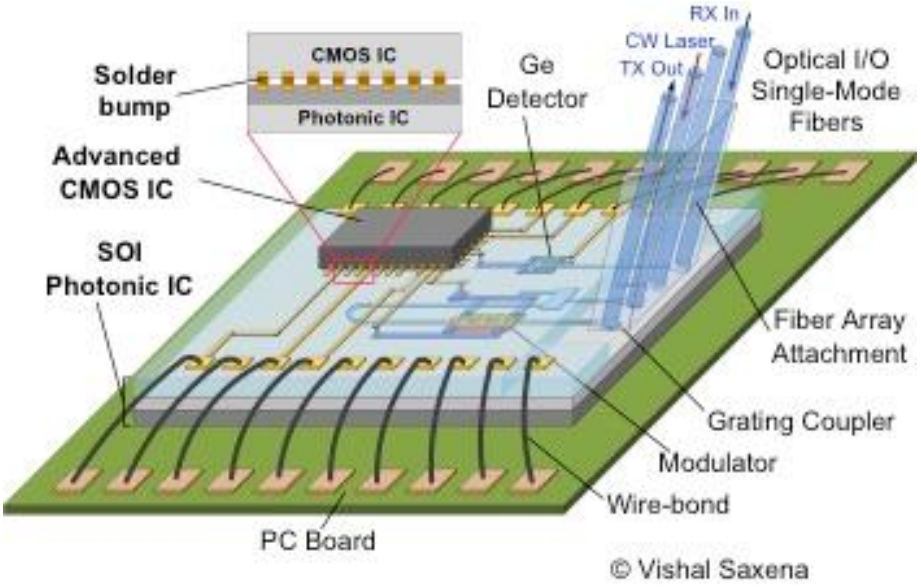

*Intel reported about some of the breakthroughs in the last decade that enabled the growth of Silicon Photonics.*

An important breakthrough is related to 2.5D (electronic interposer) and 3D (flip-chip) integration. Nowadays several integrated circuits can be assembled within one package. Both electrical and optical circuits can be combined within one package in an automated fashion.




*Packaging of an electronic IC (driver) on a silicon photonic device using a eutectic flip-chip bonding process. The inset shows a cross section of a single copper pillar to form the bond between the devices.*

The hybrid integration allows designers to select the best process option for each function. E.g. the digital functions can be integrated in high end CMOS technology with high performance and smaller size. The photonic die does not benefit from this minimum feature size and can thus be designed in a more mature SOI technology which significantly reduces the total cost.

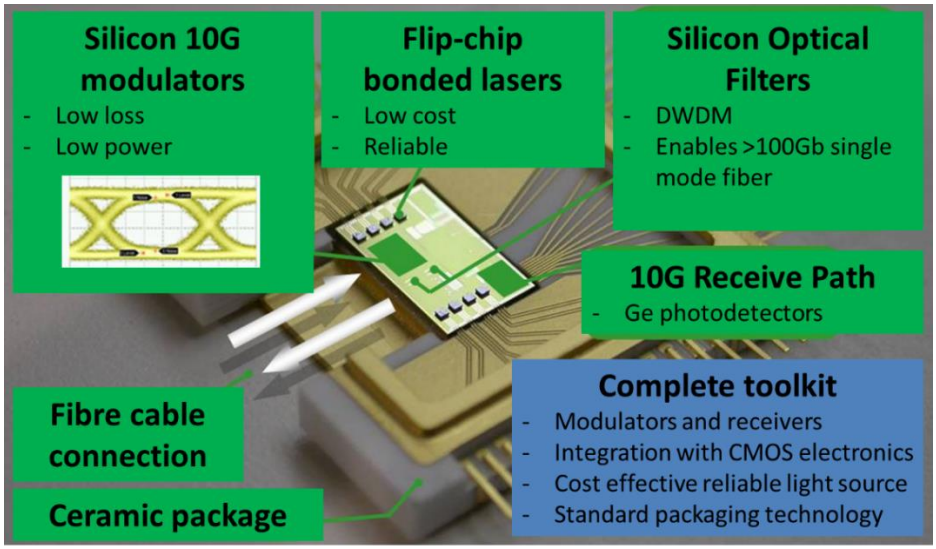



*A representation of the 3D integration of the CMOS, electrical die, on top of the photonic IC substrate.*

The CMOS (electrical IC) is connected to the SOI substrate through solder bumps. The connection distance is very short ensuring low parasitic (R, L and C) effects. That is extremely important to enable high speed interfaces and reduce power consumption of the interface. The SOI substrate includes many of the optical components like modulators, detectors.

Another option is to combine the optical die and electrical die on a shared substrate (2.5D integration).

Luxtera, the market leader in Silicon Photonics summarized their technology in an overview picture.




*Overview of the Luxtera technology (from several years ago). It shows the integration of the different elements (electrical, photonic components)*

## 3. Why optical links do need custom ESD clamps

The electrical IC that is used to control the optical parts and to process the signals before transmitting or after receiving is manufactured using advanced CMOS technology like 28nm. The interfaces consist of high speed (10Gbps, 25Gbps or even 56Gbps) SerDes-type circuits.

To create such high-speed differential circuits, designers utilize the thin oxide transistors in the I/O periphery. However, those transistors are very sensitive and can be easily damaged during transient events like electrostatic discharge (ESD). The maximum voltage that these transistors can endure during transient events is 4V or less. Despite the fact that the sensitive pads are not connected outside of the package, they could still receive ESD stress during assembly. Therefore, adequate protection clamps need to be inserted at the bond pads.

Many advanced CMOS foundries provide a set of I/O and ESD protection circuits that designers can use. However, these standard, general purpose, interface blocks are not suitable for the Silicon Photonic designs.

- The leakage from the general purpose ESD blocks is too high
- The interfaces typically operate at a voltage level below the standard I/O voltage levels (1.0V compared to 1.8V, 2.5V or 3.3V)
- The high speed SerDes circuits cannot tolerate a lot of parasitic capacitance or resistance added to the signal path. A typical analog I/O introduces 150fF of parasitic capacitance, well above what can be tolerated by the circuit.

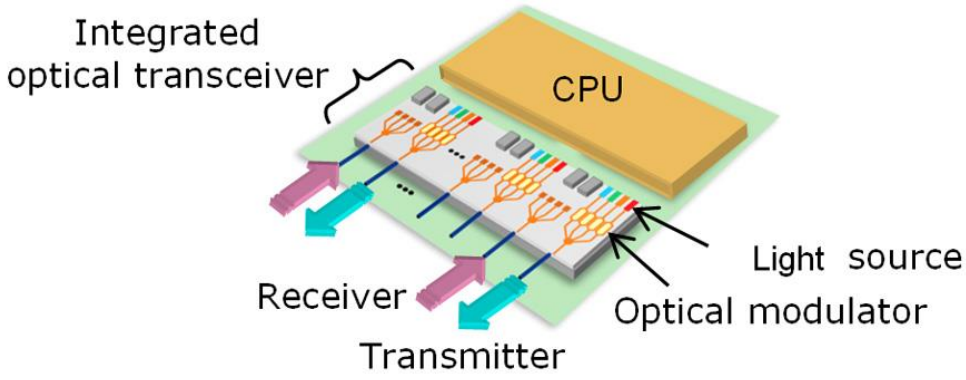
In the last 10 years, several companies that are designing products for Silicon Photonics have contacted Sofics for support. Sofics provided dedicated ESD clamps for projects in these technology nodes

- TSMC 180nm
- TSMC 130nm
- TSMC 40nm
- TSMC 28nm
- GlobalFoundries 9HP SiGe BiCMOS

In those projects Sofics engineers focused on protecting the high-speed interfaces (Tx, Rx) on the electrical die as well as protection of the low voltage power pads. In the next chapter, several case studies are summarized.

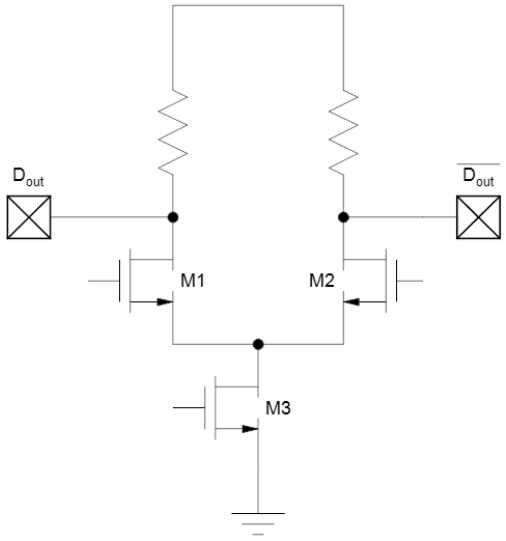
## 4. Example Sofics projects in Silicon Photonics

Over 7 recent projects Sofics supported the customer on the electrical die ('CPU'), manufactured in standard and advanced CMOS foundry technology.




*In the Sofics projects the focus has been on the protection of the high speed interfaces on the electrical component (CPU in the figure). These interfaces could be damaged during the assembly process used to combine the CPU with the optical components.*

In most cases the focus has been on the protection of the low voltage domains with sensitive thin oxide transistors and the protection of the high-speed circuits (Tx, Rx). Such interfaces are typically designed as differential, SerDes circuits. The 25-56Gbps interfaces are built with thin oxide transistors. However, those transistors are very sensitive and can be easily damaged during transient events like electrostatic discharge (ESD).



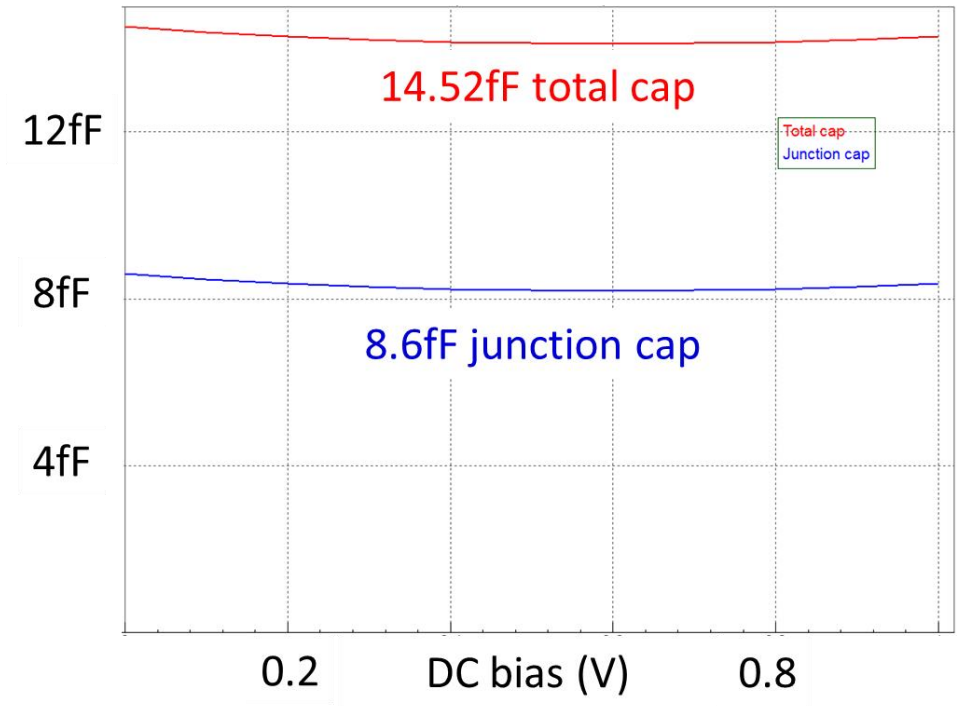

*Typical differential interface circuits used for the high speed interface circuits. Sofics provided ESD clamp circuits for each of the pads with ultra-low capacitance and leakage.*

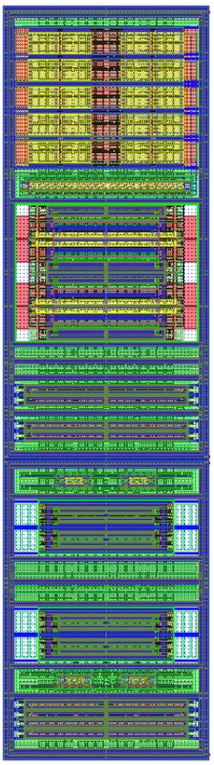
Despite the fact that the sensitive pads are not connected outside of the package, they could still receive ESD stress during assembly. Therefore, adequate protection clamps need to be inserted at the bond pads, fortunately, at a reduced ESD protection level.

To ensure that the signals are not ruined it is important that the resistance and parasitic capacitance is as low as possible. In the 4 most recent projects the parasitic capacitance for the ESD clamps at each of the bumps had to stay below 20fF.

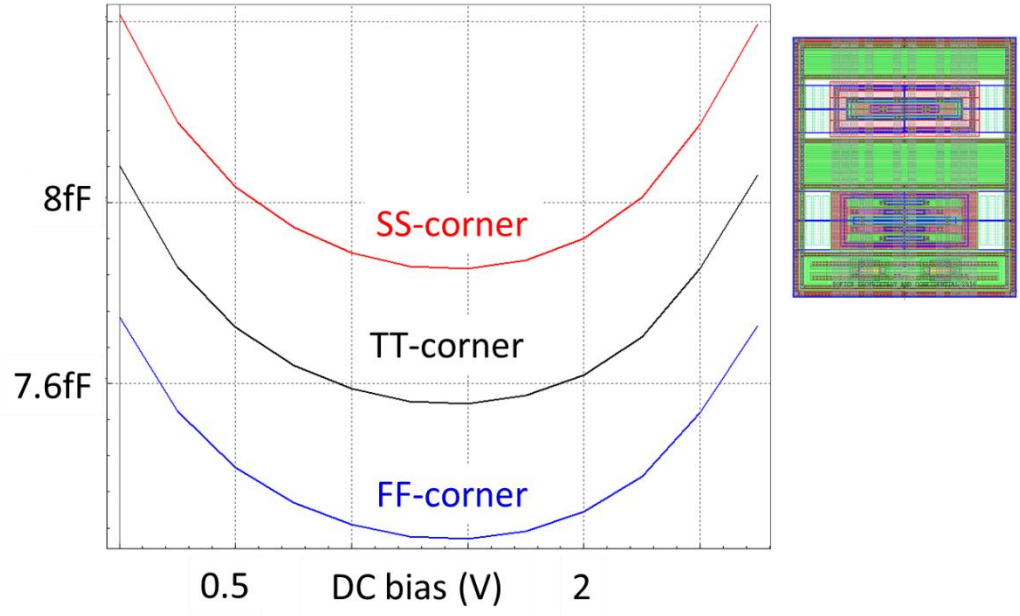
In a first project on TSMC 28nm CMOS the Sofics engineers designed a full local protection clamp concept to protect the 1V SerDes pads. A 1V power clamp was integrated to ensure all the stress cases could be handled locally at the interface. The ESD requirement was reduced to 200V HBM. The entire clamp structure was isolated from the substrate to reduce noise from the substrate that could come from digital circuits further down the die.

Through an iterative process the parasitic capacitance of the ESD clamp was reduced to less than 15fF. The plot below shows the capacitance value in function of the bias voltage at the pad. On the right side, the ESD layout is shown. The total area for the ESD protection clamp is 683.75 um².

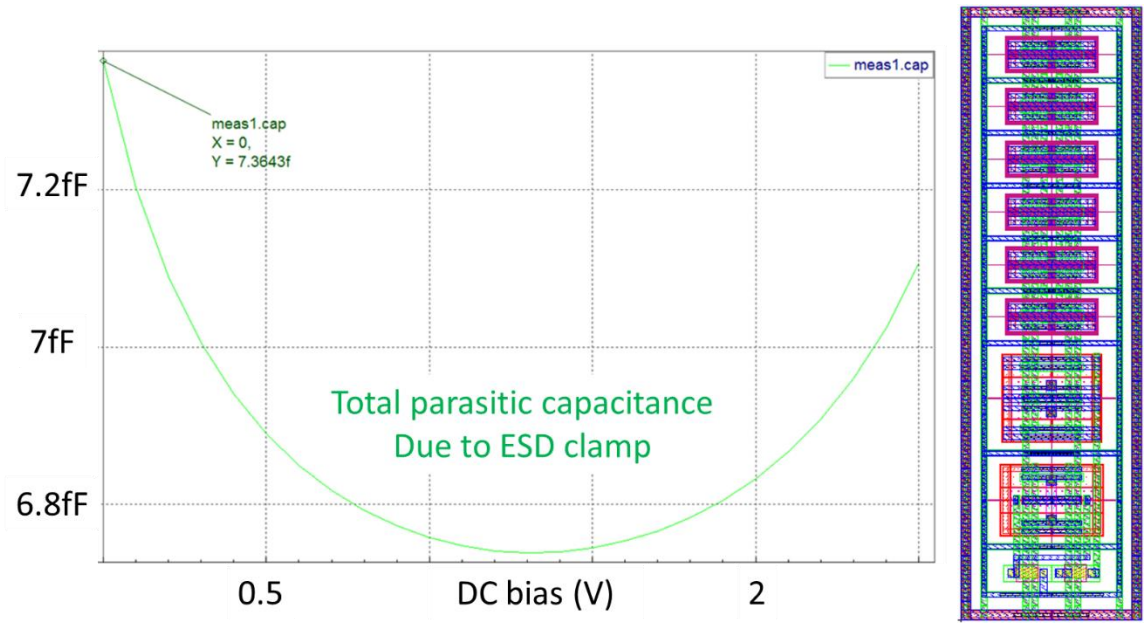


In a second case on TSMC 28nm, only the local clamp was retained at the pad. The power clamp was placed at the power pads, further away. The ESD requirement was reduced to 100V HBM to make sure that the parasitic capacitance could be further reduced. Simulations of the parasitic capacitance across different process corners are shown below. The total capacitance is in the order of 8fF. The Silicon area was reduced to 216.9 um².




The most recent project was on the IBM 9HP SiGe BiCMOS process. The customer asked help for the protection of the 2.5V high speed interface pins to 200V HBM. The total parasitic capacitance from the ESD clamps had to be below 10fF. The Sofics engineers reached a value of 8fF, within a total area of 412 um²

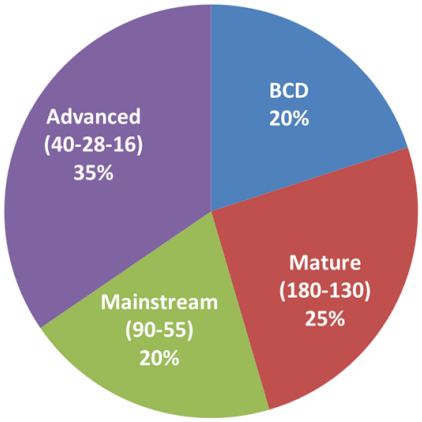


## 5. Sofics

Sofics joined the Design Center Alliance of TSMC already in 2008 based on positive feedback from several of TSMC's customers. In 2010 Sofics joined the IP alliance partnership when TSMC licensed the Sofics PowerQubic ESD clamps for 0.25um BCD technology.

Sofics currently supports more than 40 TSMC customers, across many different nodes, applications.

**Percentage of projects on TSMC technology nodes**




| Node | Voltage domains |
|---|---|
| 350nm HV | 3.3V 15V |
| 250nm BCD, gen. I and II | 12V 24V 40V 60V |
| 180nm BCD, gen. I and II | 18V 24V 32V 40V 60V |
| 180nm CMOS | 1.8V 3.3V 5V |
| 130nm CMOS | 1.0V 1.2V 3.3V 5V 7V |
| 90nm CMOS | 1.2V 1.8V 3.3V |
| 65nm CMOS | 1.0V 1.2V 1.8V 2.5V 3.3V 5V |
| 40nm CMOS | 0.9V 1.2V 1.8V 3.3V 5V |
| 28nm CMOS | 0.85V 0.9V 1.8V 3.3V 5V 5.5V 12V |
| 16nm FF+ | 0.8V 1.2V 1.5V 1.8V 2.5V 3.3V 5V |

Sofics on-chip ESD protection library

- ESD clamp solutions across 10+ CMOS generations
- Verified in 10 foundries and 30+ fabs (foundry and proprietary)
- 3000+ IC designs supported since 2000
- 80+ customers worldwide
- Patent protected portfolio
- Reduce IC cost, pass any ESD/EOS/LU specification and enhance IC performance

## 6. Conclusion

Silicon Photonics can enable a strong growth of the (optical) communication market. Thanks to the mass production opportunity of both the optical and electrical dies and the availability of 2.5D and 3D hybrid integration all the requirements can be met: Llower power, lower cost, high volume, high bandwidth.

Sofics supported 7 projects for several companies on 180nm to 28nm CMOS nodes. The main focus of the projects was to reduce the total parasitic capacitance to 10fF – 15fF. That is important to reach interface speeds of 10Gbps to 56Gbps in a single SerDes block.

## About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than 3000 IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off the-shelf or custom-crafted solutions to protect overvoltage I/Os, other nonstandard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

## Contact Sofics

Contact Sofics by email: sipho@sofics.com

## Notes